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Document 4 of 6 Page 1

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FULL TEXT OF ARTICLE:

1. [Article by Olaf Skerl and Wolfram Schmidt: ''Dynamic Memories for Single Chip Microcomputers U 8820 and U8840'']

2. [Text] From the Division for Technical Electronics of the **Wilhelm Pieck University** in Rostock

3. This article describes a circuit for the single chip microcomputers U 8820 and U 8840 which makes it possible to operate these microcomputers in conjunction with dynamic memories without taking up time for refresh functions. The circuit also avoids any time conflicts between the refresh process and time-sensitive interrupt operations. The principle used and the refresh hardware circuit will be explained.

4. Single chip microcomputers are frequently used in measuring technology since their integrated peripheral functions allow a simple set up of computers used for measuring purposes. Some applications require larger memory capacities which can be implemented by using DRAMs. However, DRAMs have the disadvantage that the information

stored has to be refreshed at short intervals.

5. The CPU U 880 provides a hardware support for the refresh function. However, the single chip microcomputers of the U 8810 and U 8820 series require a complicated DRAM refresh procedure since no refresh function has been implemented and refreshing must therefore be done via software. During one refresh period of approximately 2 ms [1] all memory cells must be refreshed at least once. This process takes up at least 20 percent of the computing time of the single chip microcomputer. In addition, during time sensitive interrupt operations there may be conflicts between the refresh function and the interrupts. To relieve the single chip microcomputer and, more importantly, to avoid conflicts during interrupt operations, a simple circuit was designed which allows the refreshing of DRAMs using the control signals of the single chip microcomputer.

6. Operating Principle

7. The DRAMs are refreshed in the background of command call cycles. This requires a division of the single chip microcomputer memory space into data and program segments, i.e. the signal /DM at P34 must be enabled. Therefore, for a command call the single chip microcomputer accesses the program segment only. During this time, the data segment can be accessed simultaneously without affecting the computer's operation as long as the data segment is kept separate from the single chip microcomputer. This principle is used for refreshing the data memory.

8. Signals /RAS and /CAS which are used to drive the DRAMs are generated by control signals /AS, /DS, /MDS. Since enabling of these control signals is inconsistent in some machine cycles (e.g. during the interrupt accept cycle, the LDE commands and Reset), the control signal /SYNC of the single chip microcomputer must be included in the refresh logic. The rising edge of /SYNC is always followed by a regular command call cycle [2].

9. For this reason, the memories are always refreshed during the machine cycle directly following the /SYNC signal, i.e. there is always exactly one refresh cycle for each command. With an external clock frequency of 8 MHz, all 128 columns are refreshed within 200 s on an average without using computing time of the single chip microcomputer.

10. The refresh hardware consists of an 8 bit refresh counter, an address multiplexer to provide the refresh address and a refresh logic which generates the required control signals (figure 1). Since the basic circuit shown in figure 1 uses the signals /SYNC and /MDS of the single chip microcomputer it can only be used for the

development versions U 882 and U 884, which are the only ones to provide the control signals mentioned.

11. *** GRAPHICS est0073 *** Figure 1. Block Diagram of the Refresh Hardware Key:--1.Data and Address Lines of the Single Chip Microcomputer--2.Address Multiplexer--3.RAM Control Signals--4.8 Bit Refresh Counter--5.Memory and Refresh Logic--6.Control Signals of the Single Chip Microprocessor *** GRAPHICS est0073 ***

12. Circuit Description

13. Figure 2 shows the refresh hardware circuit, figure 3 the time diagram. DRAM selection follows basically the suggestion given in [2] (D<inf>6<reset>, D<inf>8<reset> to D<inf>18 <reset>).

14. *** GRAPHICS est0074 *** Figure 2. Refresh Hardware Circuit Diagram Key:--1.AD0 to AD7--2.A8 to A15--3.A0 to A7--4.D<inf>11<reset> to D <inf>18<reset> *** GRAPHICS est0074 ***

15. *** GRAPHICS est0075 *** Figure 3. Time Diagram for Memory Access and Refresh Cycles (1 Low Order Part PC, 2 Op-Code, 3 Low Order Part Memory Address, 4 Data, 5 RAS-only-Refresh) Key:--1.Op code read, 2 byte command, internal ROM--2.Data Memory Access--3.Op code read *** GRAPHICS est0075 ***

16. When the data memory is accessed, the signal /RAS is generated by D<inf>10<reset> from the rising edge of /AS. Multiplexers D<inf>8<reset> and D<inf>9<reset> switch lines AD0 to AD7 of the single chip microcomputer--where the low order address part is located at this time--to the DRAM address inputs. The /CAS signal is generated from control signal /DS by a delay in the gates of D<inf>6<reset>, and the address multiplexers apply the high order address part (A8 to A15) to the DRAM address inputs. Signal /RAS is reset with the rising edge of /DS.

17. The R/W signal of the single chip microcomputer is used for the DRAM read/write control. The runtime performance of these signals [2] causes the DRAMs to function in the early write mode [1]. This allows parallel switching of the data inputs and outputs of DRAMs D<inf>11<reset> to D<inf>18 <reset>.

18. To be able to use the same memory refresh drive circuitry for accessing the internal ROM, the signal /MDS is included in the drive logic. Using the AND operation of control signals /DS and /MDS, the /DS* signal is generated which performs the same functions as /DS. /DS* is enabled both when the external memory and the internal ROM is accessed (see figure 3).

19. Since enabling of /MDS is inconsistent in some machine cycles, the refresh process is synchronized with /SYNC. The /RFSH signal is enabled during the rising edge of /SYNC and it is disabled again during the subsequent negative edge of /DS*. The AND operation of /DM and /RFSH results in the signal /RASE (RAS enable). The /AS signal can enable the DRAM signal /RAS only when /RASE is active. Thus, /RAS can become enabled only when the single chip microcomputer accesses the data segment of the memory, or directly following /SYNC. In both cases, regular /As-/DS or AS-/MDS signal sequences are generated which prevent an incorrect memory selection.

20. The DRAM signal /CAS is switched via /DM (D<inf>6,3<reset>). The /CAS signal is enabled only when the single chip microcomputer accesses the data segment; in all other instances it remains disabled. This allows a RAS-only refresh process [1]. Following /SYNC, /RAS is enabled and /CAS is disabled (see figure 3).

21. With the negative edge of /RAS, DRAMs U 2164 accept the address at address inputs A0 to A7 as a line address into the address latch. During a write or read access, this address is the line address of the memory cell selected, during a refresh cycle it is the current refresh address.

22. The refresh address is generated by an 8 bit refresh counter (D<inf>1<reset>, D<inf>2<reset>). To make counter timing less critical, the counters are not advanced until the DRAMs have accepted the refresh address during the rising edge of /RFSH. This gives the counter outputs sufficient time to respond to the new counter status. Thus, each refresh process uses the refresh address of the preceding refresh cycle.

23. To include the refresh address the tristate outputs of the address multiplexers D<inf>8<reset> and D<inf>9<reset> and of driver D<inf>7<reset> are controlled via signals /OE1 and /OE2 which are derived from /DM. If /DM is enabled, i.e. the data memory is accessed, the address multiplexers are open (/OE1 = L), and the respective memory address reaches the memory address inputs. Drive D<inf>7<reset> is disabled (/OE2 = H). If /DM is disabled, driver D<inf>7<reset> is enabled, and the counter passes the refresh address to the DRAMs. During that time, the address multiplexers are disabled, so that the memory can be refreshed (see figure 3).

24. Summary

25. The refresh hardware described allows the use of dynamic memories in systems with single chip microcomputers without using up their computing time for refresh routines. It also avoids time conflicts between refresh processes and interrupt operations. Timing

was designed so that LS-TTL circuits can be used for the complete drive circuitry with external clock frequencies of up to 8 MHz [3]. Chip types such as the U 2164 C 25 with access times of 250 ns are sufficient for the DRAMs [1]. However, only chip types U 8820 and U 8840 can be used as single chip microcomputers since their special control signals /MDS and /SYNC are required for driving the refresh circuit. We did not study the possibility of using this hardware for single chip microcomputer types U 886 and U 8611 DC/1.

26. Bibliography

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