Chrono

DIRECTOR OF CENTRAL INTELLIGENCE

Science and Technology Advisory Panel

1 March 1982

MEMORANDUM FOR: Deputy Director of Central Intelligence

SUBJECT: Technology Transfer

1. I share many of the concerns you voiced in your AAAS speech of last month. But it is not only the academic community that should be admonished. The enclosed VHSIC Notes is an excellent example of the open publication of technical information by the Defense Department. While the VHSIC contracts are unclassified, I believe the publication in the Notes of the detailed progress in this technology, the status of various programs and planned activities, all presented in detail, provides a penetrating view of where we stand in this critical technology.

2. I also wish to call your attention to a book just published by J. Wiley:

VHSIC (Very High Speed Integrated Circuits) Technologies and Tradeoffs by Arpod Barns. I believe it is based on DoD-sponsored research but have not been able to get a copy. The local bookstores report that it has been a best seller over the last three weeks. I note that Washington is not Silicon Valley.
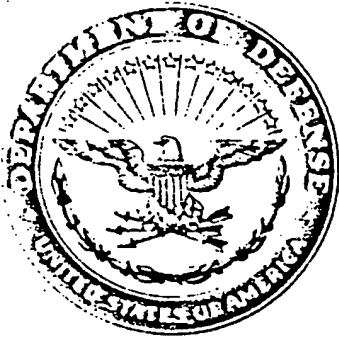
STAT

Chairman

Enclosure: a/s

cc:

STAT

VERY HIGH SPEED INTEGRATED CIRCUITS PROGRAM

VHSIC NOTES

EDITORIAL: VHSIC PROGRESS

Larry W. Sumney, OUSDRE
VHSIC Program Director

The VHSIC Program is progressing well and continues to attract widespread attention as a model for other program areas in the DoD technology base. In particular, the management structure is maturing as a cohesive entity with effective support from the three Services. Currently, program management is focusing attention on the several aspects of the program discussed below in order to assure continued progress toward the defined goals.

Design validation procedures for VHSIC chips are required at all complexity levels and are not now being addressed in sufficient depth by the Phase I contractors. Also, the various models and model parameters used in the validation procedures do not seem to be adequate in many cases. Consideration is being given to the organization of a workshop to address these issues as well as program support to a standard hardware descriptive language.

On-chip testing and fault-tolerant designs also do not appear to be receiving the attention required, although they are an important contractual requirement. Approaches being followed appear to emphasize "stuck-at" faults and non-concurrent testing which may address design and manufacturing errors adequately but not important operational testing requirements. This area will be reviewed carefully as chip designs mature.

The technology insertion efforts of the Phase I prime contractors vary considerably. In some instances, the additional chip designs resulting from the expanded number of applications could over-extend the capabilities of the available staff with a resulting degraded performance. In others, a very conservative approach has been adopted, limiting potential applications. DoD project offices have shown less initiative in VHSIC technology insertion to date but this is expected to change as a result of current information dissemination activities. Overall, this area has received considerable attention during the past several months and much progress has been made.

TABLE OF CONTENTS

It was realized that the team approach espoused by the VHSIC Program for achieving vertical integration would be difficult to implement. Thus, it is not surprising that some VHSIC contractor teams are slow in defining compatible roles for the various team members and that teaming arrangements are not yet as effective as they must be to assure successful accomplishment of the program goals. We will continue to address this problem.

A major impetus for VHSIC was and is the achievement of chip designs that can operate reliably in military operational environments. The most demanding operational specifications appear to be those related to radiation hardness. While the basic fabrication technologies appear to be capable of achieving the required hardness, there is uncertainty as to the effect of the reduced dimensions of VHSIC chips on hardness. More attention will be given to nuclear hardening techniques by the Defense Nuclear Agency in a program now being initiated in parallel with VHSIC Phase I. Other areas such as susceptibility to EMP and to microwave radiation are being studied.

Because major VHSIC chip goals are stated in terms of feature size, lithography is one of the most important technologies being addressed by the program. In parallel to VHSIC, major corporate investments in advanced lithographic technologies are being made. Optical techniques are being pushed to their limits, E-beam and X-ray machines are being developed and evaluated, and other alternatives are being investigated as well. Although direct-writing E-beam technology has been perceived as promising for VHSIC and a large investment has been made in that technology, the other options have been kept open. Now, it appears that choices can and must be made as to lithography investment strategies in the context of recent research findings, program needs,

and corporate commitments. This reappraisal should be completed in early 1982.

Over 50 Phase III contracts have been awarded. Phase III is designed to provide a broad base of research support to the Phase I and Phase II efforts. To date, however, the coupling between the research base and the mainstream efforts has not been as strong as hoped. This results from the timing of the contract awards whereby a number of Phase III efforts were underway while the Phase I efforts were still being defined and by the natural maturation of the program. For the last several months, the nature of the Phase III effort has been reexamined and steps are being taken to assure a more cohesive program and to minimize duplicative or non-contributory projects.

By direction of USDRE, a Defense Science Board Task Force is studying various aspects of the VHSIC Program. This study is chaired by Dr. W.J. Perry and is addressing such issues as progress, funding, technology insertion, report controls, and standardization. It should complete its study and make its recommendation early in 1982.

The 1981 DSB Summer Study on the technology base identified VHSIC as the technology most likely to have an order-of-magnitude impact on U.S. defense posture. This resulted from the pervasive nature of the VHSIC technology and the fact that it has a high probability of success.

While the various issues discussed above are important to the program and each must be addressed, it must be realized that none represents a crisis. Rather, each such problem is typical of the management concerns that must be continually addressed in any large complex program. As the program progresses some of these concerns will persist and others will be

resolved and replaced by new concerns. For example, it is expected that issues regarding standard versus custom chip design approaches will require much management attention as VHSIC progresses because of the resulting major implications on program directions. VHSIC NOTES will be used to apprise you of these changes as they occur.

*   *   *   *   *   *   *   *   *   *

WHAT IS TECHNOLOGY INSERTION?

R.L. Remski, AFWAL/AAD
VHSIC Program Office

Among the new concepts and technology being developed by the DoD VHSIC program is a management issue that requires increasing attention. This is the flurry of application-oriented activity known as "technology insertion." Rather than just the latest in DoD buzzwords, technology insertion is both a charge and a challenge to the VHSIC technologists and contractors to coordinate with systems users to provide more timely transition from lab demonstration to system socket utilization. Over the past several decades, technology gestation periods have ranged from as few as five or six to as many as 15 years!

In the tri-Service VHSIC program, for the first time, a large technology development program has been directed to work with systems users to develop an orderly transition procedure. This direction comes from the Under Secretary of Defense for Research and Engineering, Dr. Richard DeLauer. The shape of technology insertion activity is seen as active intra-Service marketing by the VHSIC program offices in interfacing with various levels of system developers throughout the Service commands. The technology development laboratories have estab-

lished a network of VHSIC focal points within potential user commands and are providing detailed technology and overview briefings to command level, system program offices, program managers, and engineering support operations in various application areas. They are also providing for the widest dissemination of data on chip, module, and system design permitted consistent with the VHSIC distribution limitation under the International Traffic and Arms Regulations (ITARs). Active participation in the detailed technical reviews of the Phase I contracts by consultants from the systems development operations in the Services is another tool being used to further understanding of the VHSIC program and its technology and goals.

DoD is also publishing, on a periodic basis, these VHSIC NOTES and "VHSIC Specification Design Handbooks" for use by systems designers. The Phase I programs are structured for second sourcing of the chip technology, for wide distribution of CAD capabilities, and for direct consideration of system applications in the basic statement of work. The Phase I contractors are also required to sell chips and other VHSIC technology to qualified DoD contractors through the pilot production lines to be established and running in mid-1984. Therefore, the very organization and makeup of the VHSIC program is permeated with the concept of technology transfer and insertion, to provide DoD with improved digital processing hardware and software for many applications by the late 1980s.

The Services and the six Phase I contractors are presently actively pursuing opportunities for the application of VHSIC over and above the brassboards being developed under the current Phase I contracts. Application of VHSIC technology to systems now in development and in concept is evolving at the chip, module, and brassboard levels, and in the architecture and design phases as well.

The concept of technology insertion is pervasive in that it appears in decisions affecting brassboard system partitioning, modularity, chip and chip design library candidates, and in the establishment of the CAD tools which are expected to be usable by a wide range of DoD contractors. The use of CAD tools will significantly reduce the design turnaround time for future VHSIC chips. In addition, the establishment of chip pilot production lines will provide additional copies of the chips for application in other systems as they emerge over the next few years.

The technology insertion activity in the VHSIC program is headed by Dr. Donald Burlage, OUSDRE, The Pentagon, reporting directly to Mr. Sumney. In the Army, Dr. Pete Hudson and Mr. Al Bramble (AV 995-2526/201-535-2526) of Fort Monmouth are the primary focal points for VHSIC technology insertion. The identified technology insertion focal points in the Navy are Mr. Ted Lindgren of NAVELEX (AV 222-6663/202-692-6663), Mr. Charles Caposell of NAVAIR (AV 222-2510/202-692-2510) and Mr. Dan Gordon of NAVSEA (AV 222-9760/202-692-9760). Additionally, Mr. E.C. Urban of ASN (AV 225-1444/202-695-1444) is active in Navy insertion planning. In the Air Force, the focal point is Mr. Richard Remski of the AF VHSIC Program Office at Wright-Patterson Air Force Base (AV 785-3503/513-255-3503).

Any persons or organizations interested in coupling more closely to the VHSIC Program are invited to contact the appropriate focal point in their respective Service or Command. Types of services that can be made available by the VHSIC program offices are briefings on VHSIC technology covering both chips and brassboards, distribution of reports and data pertinent to specific applications areas, and detailed technical consultation by program office and application engineers.

VHSIC HIGHLIGHTS FOR FIRST SIX MONTHS

HONEYWELL

Contract No.: F33615-81-C-1527
Program Manager: Dallas D. Burns
COTR: Mr. Robert Werner

Honeywell's Phase 1a VHSIC Program is based on the further development of a proven dielectrically isolated digital bipolar 1.25-um feature size process that is compatible with a large family of circuit technologies, including I^2L, ISL, DTL, TTL, CML, and CS^2L. This process flexibility combined with a semi-custom design approach based on the development of complex functional building blocks called "macrocells" and supported by a complete and integrated CAD system is Honeywell's solution to DoD's requirement for affordable fast turnaround ICs that will reliably provide very high performance in severe military environments. Honeywell's brassboard is the electro-optical signal processor (EOSP). Two semi-custom chips are required: a parallel programmable pipeline (PPP) chip and a controller chip. In the EOSP, two controller chips control 32 PPP chips to meet the high-throughput requirements of typical scene segmentation and target recognition algorithms -- commonly several billion operations per second. Both chips predominantly utilize ISL technology for high-density low-power logic (64,000 gates/cm^2, 30 uW/gate, 2.0-nsec delay) and CML technology for very high-speed logic (26,000 gates/cm^2, 30 uW/gate, 0.6 nsec delay). Both chips are 360 mils on a side with equivalent gate counts in excess of 20,000. Because of the flexibility of the manufacturing process, random logic, RAMs, and ROMs can be combined on a single chip for maximum on-chip data flow efficiency. The PPP and controller chips can be used in a variety of system architectures for a wide range of signal processing applications including acoustic, millimeter-wave, microwave, and optical applications. To achieve the VHSIC reliability requirement (0.006% per 1000 hours maximum failure rate), the chips have been designed with extensive self-test capabilities and the EOSP has spare PPP chips that are brought into play by self-test provisions at the subsystem level. In addition, on-chip redundancy is used to ensure the attainment of yield objectives, thus reducing manufacturing risk. Chip packaging, being developed jointly with the 3M Corporation, will be based on state-of-the-art ceramic chip carrier technology with proven high-pincount compatibility.

In VHSIC Phase 1b, Honeywell is demonstrating the feasibility of a 0.50-um feature size process (ADB-IV) based on a further extension of the 1.25-um process (ADB-III) developed in Phase 1a. The key features of both processes are summarized in Table 1.

TABLE 1. KEY PROCESS FEATURE FOR ADB-III AND AD-IV.

ADB-III

1.25-um minimum features
10:1 direct wafer stepper
All dry etched
All ion implanted
Oxide isolated
Three-layer CuAl metal

ADB-IV

0.50-um minimun features
E-beam direct write
All dry etched
All ion implanted
Groove isolated
Four-layer interconnect

Density and performance goals for 0.50-um ISL gates are 150,000 gates/cm2 at 10 uW/gate while retaining less than 2.0-nsec delay. For CML logic, these values will be 60,000 gates/cm2 at 25 uW/gate with less than 0.8-nsec delay. Thus, the ADB-IV process being developed in Phase 1b will easily surpass the VHSIC functional throughput rate requirement of 10^{13} gate-Hz/cm2. Honeywell feels that an important strength of both the ADB-III and ADB-IV processes is high inherent tolerance to radiation environments. Significant radiation testing activities have been included as a part of the Phase 1a and 1b programs.

Status of Phase 1 as of 1 November 1981

EOSP system design is proceeding as planned with initial concentration on architectural specifications, sub-system design, and chip and macrocell specifications. System requirements have been generated for segmentation, band-width compression, FFT, arithmetic operations, and histogram generation. A register transfer level description of a Sobel edge operator has been generated and documented as an example of a PPP implementation of a typical image processing algorithm. Detailed specifications for the PPP and controller chip were completed and submitted to the DoD VHSIC Program Office. Chip and system test specifications were generated along with design techniques that are consistent with non-functional test (NFT) methodology. Both procedural and nonprocedural levels of simulation using ISPS and DL languages are in progress. Functions verified to date include I/O on the PPP chip, address generation on the controller chip, floating point addition, correlation tracker functions, and a complete processing element of the PPP chip. Specifications for all the macrocells used in the two chips have been written, and functional DLS simulations have been completed for most of them. Circuit and chip

design accomplishments include the establishment of firm design rules, basic gate designs and layouts, chip floor plans, and macrocell simulation and layout. The design rules were based on processing results with test devices and include maximum current limits for electromigration resistance as well as current density limits. These design rules were applied to the basic gate designs to ensure compatibility with our simulation and testability methodology.

The controller chip contains approximately 13,000 ISL logic gates plus on-chip ISL ROM and on-chip CML RAM. The PPP chip contains a number of parallel processing elements and associated memory consisting of 17,400 ISL logic gates and CML RAM. The PPP and controller chips utilize a total of 43 different macrocells. CALMA layouts have been completed for 10 of the most complex (barrel shifter, ALU, sequencer, etc.) macrocells.

ADB-III process development is proceeding as planned with work concentrated on incorporating new process technology and optimizing process parameters to maximize yield. Baseline processes for both a reduced pressure epitaxial reactor and a high-pressure oxide growth (HIPOX) reactor have been established. The Phase 1a optical photolithography capability has been established based on a 10:1 direct wafer stepper. Baseline processes for plasma etching of silicon oxide and silicon nitride have been established with excellent uniformity. A yield model test chip to provide data on the density of yield reducing faults has been completed through design and layout. Baseline processes for both a metal deposition down-sputter system and a plasma-assisted SiO2 dielectric for threelayer metal have been established. Test chips with 1.25-um geometry have been processed and tested using automatic measurements techniques for evaluation of device parameters. Good results were obtained

with typical transistor current gains of 50-100, and collector-emitter (V_{ceo}) breakdown voltages greater than 6 V. ISL gate delays were found to be very uniform with average delays of 0.72 nsec.

The ADB-IV (0.5 um) process development is proceeding as planned with completion of initial submicrometer test chip runs and evaluation of groove refill isolation processes. This work produced functional transistors with 0.75-um emitters with typical current gains of 100-150. Development of a technology utilizing groove refill isolation is in progress. This will result in a planarized surface with reduced isolation area and lower temperature/time processes.

Samples of groove refill using several process variations were evaluated. LPCVD oxide appears to yield the best results with good planarization. Preliminary evaluation of a two-layer electron resist structure to obtain submicrometer metal interconnect showed very promising results with interconnect lines down to 0.6-um pitch demonstrated.

The packaging development has been planned in two steps. In Phase 1a, packaging will be developed for chips with up to 180 pins, and beam tape bonding will be used for high-yield high-reliability mass-bonding chip-to-package interconnect. In Phase 1b, the pin count will be extended to 240 pins, and an area tape bonding concept will be used.

In summary, Honeywell is off to a good start on the execution of its Phase 1 VHSIC contract. All program activities are proceeding as planned and virtually all results to date have reinforced our confidence in our ability to meet or exceed the original objectives of the program.

HUGHES AIRCRAFT COMPANY

Contract No.: DAAK20-81-C-0383
Program Manager: Dr. Art Chester
COTR: Dr. Pete Hudson

Introduction

The following sections provide brief discussions of the major aspects of the Hughes VHSIC program. These include: (1) the CMOS/SOS chip technology, which provides a unique combination of high speed, low power, and radiation hardness; (2) the spread-spectrum communication-system brassboard demonstration, based on three flexible VHSIC function chips; (3) the DAST activity, especially the advanced CAD system, which optimizes the combination of human creativity with machine support; and (4) the submicrometer process development, which builds on and supports the 1.25-um chip technology.

Chip Technology and Fabrication

The Hughes Phase I approach is based on CMOS/SOS technology, which provides high speed, low power, and radiation hardness. The 1.25-um version of this process is a direct development from the existing CMOS/SOS process at Hughes that is providing LSI chips for production systems. The evolutionary sequence is summarized in Table 2, which shows the basic design rules for each process. Both the SOS II and SOS III (VHSIC) processes use tantalum silicide gates and two levels of aluminum, so they are identical except for scale.

The VHSIC pilot line is being established in a new ultra-clean facility with 12000 square feet of controlled area, computer controlled diffusion furnaces, computer controlled photolithographic processing tracks and projection aligners, computer controlled wafer cleaners, central computer manufacturing control, and a full complement of plasma etchers and thin-

TABLE 2. CMOS/SOS TECHNOLOGIES.

DESIGN FEATURE	SOS I (um)	SOS II (um)	SOS III (um)
PolySi Gate	3.5	2.5	1.25
PolySi Pitch	10.0	6.5	3.0
Metal Pitch	12.0	14.0	5.0
Metal/Poly O/Lap	5.0	3.0	0.8
Contact	4 x 4	3 x 4	1.6 x 2

film equipment. Each building block of the process is based on computer modeling and supervised by the computer-aided management system.

The 1.25-um process and its design rules have been established in cooperation with two second sources, RCA and Rockwell. The second source subcontracts provide for concurrent process development, with the second sources processing both test chips and VHSIC function chips. The first pilot line test chip is in fabrication at Hughes, RCA and Rockwell. The first lot processed by Hughes using the 10:1 direct step on wafer aligner was completed in November 1981, with good initial results. A baseline oxide etch process is established, and work on etch selectivity is progressing. A silicide reactive ion etcher (RIE) is installed and operational. Metal etch to VHSIC dimensions has been demonstrated, and silicide, aluminum, oxide etch, and the double-layer metal have been shown to be compatible. Process development is moving ahead strongly, and a SOS material characterization and improvement effort has been defined and initiated.

Communication Chip Set and Brassboard Demonstration

The 1.25-um CMOS/SOS chip technology is being used to implement three reconfigurable function chips that provide key signal-processing functions common to a very broad range of secure, anti-jam communication sys-

tems. The high performance of these chips will enable them to provide cost effective communication systems into the 1990s. Their flexibility, reliability, and low power will enable them to be retrofitted into existing and developing systems with significant cost savings and improvements in reliability. Detailed technology insertion plans have been developed for the position location and reporting system (PLRS), where substantial cost and reliability improvements can be achieved in near-term production programs. In the Phase I brassboard demonstration, the three chips will provide performance enhancement of the PLRS/JTIDS hybrid for the future Army battlefield information distribution system. These three chips have been defined, and the first chip is into layout.

The three chips are a 256-stage digital correlator chip, an algebraic encoder/decoder chip, and a spread spectrum subsystem chip. These chips will operate at 25-MHz off-chip clock rates and 100-MHz on-chip clock rates. Their complexity level approaches 20,000 gates, and their full power at maximum clock rate is less than 0.7 W. The chips are designed for nominal operation at 5 V, but they are compatible with 3-V operation as well. The correlator chip has completed logic design review and is into layout. The encoder/decoder chip is almost ready for logic design review, and the spread spectrum subsystem chip is at the detailed block diagram level, with several parts of the logic defined.

The PLRS technology insertion plan covers the digital signal and message processor subsystem module of the basic user unit, a man-packable terminal. The primary impact of the VHSIC technology insertion will be to halve the size, weight, and cost of the signal and message processing module, and to double the reliability of this module. The total parts count

for the two-card module will be reduced from 280 to about 100. A preliminary estimate of the reliability improvement indicates that there will be an 18% increase in the predicted mean time between failures (MTBF) of the basic user unit as a result of changing the single module. The corresponding cost reduction is 12% of the basic user unit cost, resulting in very substantial production cost savings.

DAST and CAD System

Design technology, software tools, and chip test support are provided by the DAST segment of the Hughes VHSIC program. The CAD tools being developed provide hierarchical designs. The designer works at the symbolic level, with structured cells. Design guidelines emphasize testability and provisions for fault tolerance, while automatic test generation provides esentially complete test coverage. Full utilization of the performance potential of the chip technology is obtained by providing concurrent hierarchical simulation of performance, including the effects of interconnection parasitics. Design verification is provided by simulation at several levels, and by cross check of layout interconnections with the logical description of the chip. The set of CAD tools interacts through a common data base, using a data-base management system. The set of CAD tools is being developed for the VAX-11/780 computer, while emphasizing portability to other 32-bit virtual memory machines.

The development schedule for the VHSIC CAD system includes an operational LSI level of design capability at six months. This six-month milestone was met on schedule, providing separate CAD tools, working on a common computer. This near-term capability will be used to design the macrocells for the VHSIC function chips. The next

step is an interim VHSIC CAD capability. Work on this system has been going on in parallel with the basic system. The interim capability will be available in the second quarter of 1982, and it will be able to handle the VHSIC complexity of the three function chips. By the first quarter of 1983, these tools will be significantly enhanced and integrated to form a complete system operating under a common data base. Finally, by the end of the program, the total hierarchical capability will be incorporated into the tools and documentation will be completed, thus making the CAD system available for transfer to the VHSIC community.

The VHSIC CAD tool set is 95% defined. In addition to meeting the first major milestone of an operational LSI capability at the new VHSIC design center, a hardware and artwork description language recommendations report was prepared and delivered on schedule. Good progress is being made toward the next two major milestones; for example, a detailed information model for the common data base is 30% complete.

Submicrometer Technology

The Hughes approach in the Phase 1b development of a 0.5-um CMOS/SOS process is based on continuing evolution from the 1.25-um process. This evolution is summarized in Table 3. A key difference is the necessity to use a refractory metal for the intermediate interconnect layer in the 0.5-um process. This process will use e-beam direct write to fabricate the mask levels with the smallest resolution and tightest alignments, and the refractory metal interconnect permits annealing of e-beam induced neutral traps. The process will work with a thinned epi-layer to optimize leakage, threshold voltage stability, and carrier mobility.

TABLE 3.   EVOLUTION OF 1.25-0.5 um.

	SOS III (1.25 um)	SOS IV (0.5 um)
Technology	CMOS/SOS	CMOS/SOS (CMOS)
Lithography	DSW	E-beam (DSW)
Metalization	Two-level (Al + Al)	Two-level (Refract + Al)
Epi thickness	0.5 um	0.3 um
Channel implants	Double	Double
Gate metalization	Silicide	Silicide
Etching	Dry	Dry

The submicrometer development strategy is based on using optical lithography to determine non-lithographic issues, performing extensive process and device modeling, using existing research e-beam equipment, and utilizing results from the Phase 1a 1.25-um process development.

The first milestone, a report reviewing all equipment necessary to make the submicrometer devices, was completed and delivered on schedule. The simulation efforts started on schedule. Several test lots have been processed to evaluate different steps in the process and to confirm theoretical scaling laws.

Good progress has been in p+ implants, n+ implants, double resist processes, and anisotropic etching. Simulation results agree with observed performance, predicting 50-psec ring oscillator speed at 3-5 V for the present device design. Exposure and development studies are providing both positive and negative resists to support the e-beam lithography.

IBM

Program Manager: Dr. H. Cloud
Contract No.: N00039-81-C-0416
COTR: Eliot Cohen

This report presents progress by IBM on the VHSIC Phase 1 Contract covering the period from 1 May 1981 through 1 November 1981. IBM's Federal System Division at Manassas, VA, has the prime responsibility for the VHSIC program with support from IBM's General Technology Division, Burlington, VT and Research Division, Yorktown, NY.

Technology and Processing

The key technology requirements for the VHSIC 1.25-um program are to develop chips which have the following characteristics: densities of 10-30K gates per chip; operation with clock frquencies on the chip of at least 25 MHz; overall functional throughput rates (FTR) of at least 5×10^{11} gate-Hz/cm^2; and the capability to operate in military environments. The key program objectives for 1.25-um technology are to develop a process, practice this process for newly developed macros and chips, and integrate and test these chips in a brassboard within the three-year schedule. IBM has selected NMOS as the base technology for 1.25-um VHSIC because it is IBM's lowest risk technology in achieving the above objectives within the three-year schedule. The characteristics expected in the technology area will meet or exceed all VHSIC requirements (see Table 4). In the packaging area, IBM is developing a single-chip package for the brassboard. For the VHSIC submicrometer program, Phase 1b, IBM is examining extensions of MOS technology at IBM's Research Division.

IBM is developing the 1.25-um technology capability based on in-house development work in NMOS technology. IBM's plan for 1.25-um development is to extend the necessary process steps

TABLE 4. PHASE 1a VHSIC CHARACTERISTICS

Chip Technology
    Performance -- 25 MHz
    No. of Gates -- 30K/chip
    Power -- 3 W/Chip
    Size -- 8 x 8 mm
    FTR = 12 x 10^{11} gate-Hz/cm^2
        (approx.)

Packaging
    Single -- chip carrier
    I/O -- 240 (190 signal, 50 pwr/gnd)
    Interconnect -- decal
    Size (substrate) -- 1.5 x 2 in.
    Package (2nd lev) -- avionic

Environment
    Military

to 1.25 um from established process capability, and add the necessary radiation hardening enhancements to satisfy VHSIC requirements. IBM is currently characterizing the process and is making test sites for purposes of evaluation. Process work will continue throughout 1982 with process transfer to the VHSIC pilot line to be completed in the last quarter of 1982. Radiation-hardening work is being emphasized in the IBM approach. Plans are in place to evaluate hardening enhancements through 1982 with final techniques selected and integrated into the VHSIC pilot-line process in the 1983 time frame.

Architecture CAD and Support Software

IBM's major objective in the chip architecture area is to develop a cost-effective design capability for VHSIC which can be used for the development of unique chip configurations required in DoD weapon systems. The IBM approach complements the chip family approach in that DoD weapon systems will continue to require the development of new chips to extend the capability of already developed chips so that optimum system implementations

can be achieved in VHSIC and VHSIC-like technology. This design capability is characterized by a chip architecture called "master image" which utilizes a comprehensive set of primitive and custom macro functions stored in a computer library. The designer selects from the macro library those functions that he needs to personalize a chip design. Table 5 summarizes the initial macro list under development. Primitive macros are more simple logic structures consisting of NORs, exclusive ORs, drivers, receivers, latches, etc. Custom macros generally address more complex functions than primitives such as the 16 x 16 multiplier, multi-input adder/accumulator, interface handler, an on-chip monitor for testability, and an extendable register file for buffer storage.

Essential to the success of this approach is a set of CAD tools which facilitates the design process for macros and chips. Chips of the VHSIC complexity must be developed utilizing such a CAD system. This CAD system will provide adequate tools for simulation, design entry and checking, and documentation throughout the overall process. Products of the CAD effort will be a basic design capability which will permit custom chip design for diverse system applications.

TABLE 5. Phase Macro Library (CORE SET)

Primitive Macros	Custom Macros
NOR	16 x 16 Multiplier
Multiplexer	Three-Way Adder
Exclusive OR	Register File
On-Chip Receiver	On-Chip Monitor
On-Chip Driver	Interface
Clock Driver	
Shift-Register-Latch	
Carry-Look-Ahead Adder	
Transceiver	
Parity Generator	
Arithmetic Logic Unit	

Under the VHSIC program, IBM is addressing the support software tools for designing systems where the design assets will consist of an inventory of VHSIC and VHSIC-like components expressed in VHSIC hardware descriptive language (VHDL) and macros or subcomponents of VHSIC chips, also expressed in VHDL. An interactive system design capability is needed so that the system designer may have access to the design assets and apply various tools for analysis, simulation, checking, and documentation relative to optimizing his system design. IBM is defining the tool set and approach to support this interactive process. As a product of the process, optimized system designs composed of VHSIC technology will emerge.

Chip Development

Under the VHSIC program, IBM is developing the complex multiply accumulate chip (CMAC) as the initial chip utilizing 1.25-um technology and design capability. The CMAC is a parameter-selectable signal processor which can perform 100 million multiply and accumulate operations per second. It is intended to be used on the front end of signal-processing systems where processing demands require this type of capability. The CMAC chip executes high-performance signal processing algorithms required in the front-end data stream of many sensor processing systems. By using the IBM NMOS VHSIC technology, a very high multiply rate is achieved with significantly fewer watts and in a much smaller volume than has been achieved with current technologies. This high performance is accomplished with a very simple data flow that uses a number of multipliers connected in a linear array. The simple-structure concept extends to the control of the chip where a parameter selectable rather than programmable approach is used. The algorithms executed are highly repetitive, simplifying the control task. Flexibility is obtained by loading a

parameter, during initialization, from an external controller to configure the data flow for the desired algorithm. The CMAC chip has two basic classes of operation: (1) complex multiplication of a number of four parallel channels by a set of preloaded weights and summation of the products and (2) any of a number of delay, multiplication, and summation operations on a single channel by using cascaded sections of identical hardware. The CMAC operates with parallel stages of multiplication and accumulation, each stage operating with a basic clock frequency of 25 MHz. Current technology sizings indicate a chip density in excess of 30K gates for the chip.

Testability

IBM is placing significant emphasis on testability within the chip to provide built-in logic for manufacturing test and sufficient on-chip logic capabilities for supporting system level availability and fault tolerance. The basic approach requires, as part of the design process, added logic on the chip to implement two major testability features: level sensitive scan design (LSSD) and the on-chip monitor (OCM) macro. LSSD is a design discipline, whereby the function of the chip can be subdivided into combinatorial elements, and each element tested by inserting test patterns with the measured response compared against predetermined results. For a relatively small overhead, fault detection or coverage of greater than 96% of the gates on the chip can be expected. Furthermore, the LSSD discipline allows the test patterns to be generated automatically by the computer. The OCM is a testability macro whose function is to control and manage the testability of the chip. It also serves as the standard chip interface for testability to the overall system testability architecture which is defined as the availability management system (AMS). AMS consists of a

TABLE 6. EXPECTED BRASSBOARD SYSTEM CHARACTERISTICS.

o FUNCTION
- High-performance acoustic preprocessor

o PROBLEM ADDRESSED
- Increased detection
- Potential for increased system capability

o BRASSBOARD CONFIGURATION
- Expand capability of AN/UYS-1
- Upgrade to input signal conditioner

o SYSTEM APPLICATION
- P3, S3, AN/BQQ-5, LAMPS
- Preprocessing for AN/UYS-1 Navy standard processor

---

software-based executive or controller which ties into all of the OCMs in the system. Availability management at the system level is the primary role of AMS and will provide error detection, error logging, fault isolation, and system recovery. These attributes are essential to achieving fault-tolerant systems of the future. The architecture attributes of testability will be built into the chips and demonstrated in the brassboard.

Brassboard Development

The brassboard under VHSIC Phase 1a development is a high-performance acoustic preprocessor (see Table 6). The capability being furnished will provide for increased target detection in anti-submarine warfare (ASW) systems. Requirements in ASW have been evolving and growing for many years due to more sophisticated and quieter threats. Significant advancements have been made in signal processing which have lead to very demanding system requirements for the Navy ASW platforms. These requirements are by no means satisfied with today's tech-

nology due to space, weight, and cost considerations. VHSIC technology is an ideal match for addressing the acoustic problem in that the signal-processing capabilities needed for keeping pace with the threat can be realized. The brassboard configuration specifically addresses an upgrade to the input signal conditioner (ISC) of the AN/UYS-1. Expanded digital processing will be added to the ISC, permitting more functions to be addressed by the overall configuration without the need for redesigning the hardware and software of the AN/UYS-1. This "front-end" improvement will provide for increased processing capability and will facilitate technology insertion for those platforms currently employing the AN/UYS-1.

TEXAS INSTRUMENTS

Contract No.: DAAK20-81-C-0382
Program Manager: Dr. Dean Toombs
COTR: Dr. Pete Hudson

The Texas Instruments VHSIC-1 Program is based on a small set of multipurpose programmable system components implemented in commercially aligned semiconductor technologies; a multi-mode fire and forget (M^2F^2) missile subsystem demonstration brassboard and a comprehensive set of software/hardware design tools to support subsystem design with the basic chip set.

Eight chips have been defined and are currently under development. A high-performance NMOS memory and seven logic-oriented components that will be implemented in Schottky transistor logic (STL). NMOS was selected for the memory because of the high density, low power, and low cost intrinsic to the technology. STL was selected for the logic components because of inherent reliability and tolerance for the military environment and exceptional speed-power product characteristics.

Many of the candidate VHSIC brassboard systems shared several basic IC related requirements such as:

o Memory:
   High performance, low cost.

o Data Processing:
   Data-dependent arithmetic, logic, and control operations on unstructured data streams.

o Array Processing:
   Repetitive data-independent operations on fixed-size blocks of data.

o Limited Special-Purpose Processing and Interface:
   Some application specific requirements must be supported.

The Texas Instruments chip set and related design support tools have been architected and specified to accommodate these needs. A brief functional description of the chips as they apply to the requirements follows. The design support tools will be discussed later with the design utility system.

Memory needs are served with a single general-purpose component:

o Static Random Access Memory (SRAM):
   25 usec read/write access, on-chip parity generate/check, and 1K block write protection.

The 1750A instruction set architecture (ISA) was selected for data-processing requirements and three logic components defined as:

o 1750A Data Processor Unit (DPU):
   A full 1750A ISA with 6-MIP 16-bit fixed-point throughput, multiprocessor support, and memory error detection/correction.

o Device Interface Unit (DIU):
   Implements direct memory access (DMA) operations, provides interval timing, and performs instruction I/O.

o General Buffer Unit (GBU):
   Supports multiple level bus operation, provides first-in/first-out (FIFO) buffered transfers, and performs parallel I/O.

These three chips, together with the static RAM, can be configured as an application specific or a generic data processing node.

Four logic chips have been defined to meet the array processing requirements. They consist of a highly concurrent 16-bit fixed-point arithmetic resource and three support chips:

o Vector Arithmetic/Logic Unit (VALU):
   75-MOP 16-bit fixed-point throughput pipelined arithmetic capability.

o Vector Address Generator (VAG):
   Two-dimensional X-Y array addressing, FET bit reverse, cycle steal I/O support, and data memory chip select decode.

o Array Controller/Sequencer (ACS):
   General purpose microcontroller with nested do-loop control, a subroutine stack, and an register file.

o Multipath Switch (MPS):
   Connects memories with ports, supports cycle steal I/O, single memory/multiprocessor broadcast, and static and dynamic state control.

As with the data processor, these four chips and the SRAM can be configured to match specific or generic array processing requirements.

The SRAM and VALU designs are to be executed as dedicated optimized IC designs. The 1750A DPU, DIU, ACS, and VAG are ROM programmable components that will each be unique programmations of a 10K-gate/52-kbit ROM base array. The GBU and the MPS will be implemented as programmations of a 4K-gate base array. This 4K-gate base array will also be available with sup-

porting software for design and implementation of special-purpose processing and interface requirements. The entire chip set is TTL I/O compatible and will be packaged in Joint Electronics Device Engineering Council (JEDEC) standard leadless chip carriers.

Chip and system level testability have been comprehended in the component functional specifications. The programmable system components (PSCs) will incorporate on-chip self-test and a standard four-pin maintenance port. This will avoid the usual test bandwidth limitations, allow at-speed chip testing, and solve controllability/observability depth problems. Compatible processor and systems level testing have been defined to support fault tolerance operation, "push to test" go/no-go verification, and breakpoint/single-step operation for system checkout.

Preliminary chip specifications have been prepared for all components, and detailed final specifications are in preparation. Actual chip design is under way for both the SRAM and VALU.

The M^2F^2 VHSIC demonstration brassboard will be based on a passive rf, anti-radiation homing (ARH) sensor, and an imaging infrared (I^2R) sensor. The data and array processing modules defined and developed for the brassboard will be integrated with two existing sensors to provide the signal and control processing required for the operational function of an M^2F^2 missile subsystem. The functions to be demonstrated include control of the ARH and I2R sensor, multithreat processing of the ARH sensor data, precision queing of the I2R sensor to the radiating target selected, autonomous acquisition of the potential target from the I2R field of view and the concurrent track of the target by both sensors. The software applications for the brassboard data processor module will be

written in a higher order language (Pascal) with calling provisions to functions programmed in the array processor.

The data-processing node defined for the M^2F^2 missile subsystem brassboard is a 4-MIP 22-component configuration with 64K words of 16-bit memory. The array processor node is a 22-chip 75-MOP throughput processsor with 40K words of 16-bit memory. Missile compatible module packaging concepts have been defined that accommodate both a data and array processing node on a single 9 x 5 inch ceramic substrate. Power dissipation on the substrate will be well inside 1 W/in.^{2}.

Specification of the brassboard configuration and system performance requirements based on operational scenarios are complete. Detailed design of the system testbed and demonstration software is under way.

The design utility system (DUS) is a body of user executed software and hardware that should constitute a sufficient tool set for a subsystem designer to define a set of hardware resources and specify the PSC programmations required for a given subsystem design. The concept is analogous to the support which is currently provided for microprocessor user community. The DUS consists of four basic tool sets:

o A hardware description language and integrated simulator that is used to specify, design, and evaluate system level configurations, array and data processor nodes, and gate array programmations.

o Array processor support software that is used to specify, emulate, and design vector processor nodes. It consists of a configurable register transfer language compiler, linkage editor, and instruction level simulator.

o Data processor support software that is used to specify, evaluate, and design 1750A-based processing nodes. It consists of an HOL (Pascal) compiler, 1750A assembler, link editor, and instruction level simulator.

o A software maintenance panel that supports systems hardware/software test and diagnosis.

An integrated DUS will be delivered under the VHSIC 1 contract. It is intended to be software transportable. Detailed design is underway in each of the four areas mentioned above.

TRW

Program Manager: Dr. B. Whalen
Contract No.:   N00039-81-C-0414
Navy COTR: Eliot D. Cohen

During the first six months, TRW assigned definitized work packages, schedules, and budgets to all responsible organizations including our subcontractor/teammates, Motorola and Sperry Univac. Additional tasks for testability and fault-tolerant design were added to the Sperry Univac statement of work. Detailed schedules and budgets were computerized on the CSSR system to provide means for early identification of potential cost and/or schedule problems.

Our process development activities, which include Phase 1a and Phase 1b tasks in both 3D bipolar and CMOS, have continued as they were proposed. TRW began Phase 1 with an existing baseline 1-um process. Our Phase 1 efforts are directed toward enhancing this process with features which increase device density, increase operating speed, improve yield, and/or improve design flexibility. These enhancements include the incorporation of arsenic resistors to permit the independent optimization of collectors and resistors and thereby avoid a penalty in scaling, the use of

double-level metallization to improve both density and speed, dry etching of metal and oxide to permit reduced design rules with a resultant increase in functional throughput, incorporation of Schottky diodes in output drivers, and the use of low-temperature annealing techniques to allow ion implant activation and damage removal with minimum junction movement. Highlights of TRW's achievements included delivery of 100 flash A/D converter chips to demonstrate the stability of our baseline 1-um process.

Similarly, at the start of Phase 1, Motorola was well under way with development of a 1.25-um CMOS process having already designed a Phase 0 chip. Motorola's goal is to achieve a basic operating 1.25-um process by February 1982 and then use that process to develop enhancements such as the addition of a refractory metal shunt for the polysilicon gate material, alternative metallization to further reduce metal pitch, buried contact and polyresistor technology, and the addition of a third layer interconnect capability. Their activities during the first six months of Phase 1 consisted of producing test wafers, evaluating them, and incorporating processing changes to improve the performance of later runs. Equipment and software tool enhancements were also accomplished. Achievements included production of test device chips with reasonable yield.

Development of submicrometer processing capability is a challenging task for both 3D bipolar and CMOS technologies. During the first six months we concentrated on running experiments and gathering data that cannot be extrapolated from larger feature size work. This activity included the design of test chips. Achievements were the establishment of an operational e-beam machine at both TRW and Motorola, TRW's definition of a submicrometer process, and Motorola's production of working p- and n-channel devices with 0.5-um feature size.

In the DAST effort, we examined signal processors that require both high flexibility and substantial parallelism to achieve high volume but relatively repetitive number manipulations. Data-processing architectures tend to be more serial in nature, less synchronous, and more control intensive than signal-processing architectures. These differences lead to different requirements not only for VHSIC chips but different interconnect concepts as well. The V Bus interconnect developed by Sperry Univac allows any single pair of users to initiate, carry out, and terminate a communication with very little overhead and thereby fits the data-processing requirement. Signal processors, however, require that many short point-to-point communications occur simultaneously and these can be under program control. The DAST studies reaffirmed our Phase 0 selection of cross-bar-type switches for signal-processing applications.

Computer-aided design (CAD) and simulation activities being undertaken by Sperry Univac were started. The CAD system being developed makes use of a number of existing and evolving software programs. These programs include the logic simulators, circuit simulators, layout aids, testability aids, routing algorithms, and verification tools. A key task of the CAD and simulation efforts will be to unify these separate software tools and make them available to a designer from a common data base and using a single hierarchical system language whether he operates at the system, board, chip, macrocell or diverse level, or a combination of several levels simultaneously. One of the highlights was the interfacing of the ADLIB/SABLE mixed level simulator to the data base.

Testability received considerable emphasis during the first six months. Our testability approach is to specify a generalized test concept around a maintenance processor, a maintenance network to connect chips and boards to the maintenance processor, and a maintenance node on each chip whose purpose is only to handle communication protocol between the maintenance processor and the chip. Within this framework we are conducting a top-down look at testability to identify system requirements for testability and fault tolerance. At this time, we are specifying the testability features of the individual chips. Circuitry on each chip will perform the testability functions and convey results to the maintenance node. Software in the maintenance processor will process individual chip results. Achievements include the design of a main- tenance node for use on each VHSIC chip which meets the testability requirement.

The EW brassboard development requires an intensive first-year effort during which system requirements must be established; chip specifications produced with all functional, testability, and interfacing requirements defined; and a demonstration plan baselined. In parallel with chip design and fabrication, all packaging design and fabrication for chips, boards, and the brassboard must be completed. Brassboard software must be developed in parallel with the chips. All software development will use hardware emulators because no hardware will be available until final integration and test. During the first six months we completed our system requirements defintion and are nearing completion of our baseline processor design. A major effort to design and specify our eight custom VHSIC chips was initiated. We completed specifications on the window addressable memory (WAM) chip and are nearing completion on the matrix switch, register arithmetic logic unit (RALU), and four-port memory.

In the quality assurance area, quality control patterns which will be used to monitor chip production line performance were defined.

WESTINGHOUSE

Contract No.: F33615-81-C-1532
Program Manager: Dr. John Walker
COTR: Mr. Robert Werner

The Westinghouse VHSIC Program is a team effort focused on the development of a multiprocessing computer capable of handling the signal-processing functions of the advanced tactical fighter environment. Included in the team are National Semiconductor, Control Data Corporation, Harris, and Carnegie Mellon Institute. The team has adopted a commonality concept which includes a chip set based on 1.25-um CMOS IC technology, a set of modular signal processors, architecture capable of adaptation to a large variety of environments, and a high-order language programming approach.

A pilot line has been established for the fabrication of VHSIC chips. Process experiments and simulations have been used to define the CMOS baseline process which will meet speed, density, and reliability requirements. A process development test vehicle has been designed and is in fabrication to verify lithography, design rules, performance, and reliability of the baseline process. Parallel experiments are also in progress to optimize the baseline process prior to fabrication of logic test vehicles during the next reporting period.

A total of 36 minicells, the basis of the hierarchical design approach, have been designed and simulated. A handbook containing design information is being prepared for use by the team members. Models are to be introduced into the computer data base for use in logic design.

During the next reporting period, a minicell test vehicle, a gate array test vehicle, a 16 x 16 multiplier, and a 64K memory test vehicle will be introduced into the pilot line as a part of the validation process. The minicell test vehicle will contain samples of the minicells and associated delay chains necessary for evaluation of minicell performance. The 16 x 16 multiplier is the first VHSIC density logic circuit to be completed using the minicell library and it exhibits a gate density of 160K gates/cm^2. The gate array test vehicle will provide test cells of the gate array to demonstrate its performance. Likewise, the memory test vehicle will demonstrate yield and operational parameters for the 64K memory design.

The package development program has identified package requirements and has resulted in development requests to four package manufacturers. The packaging study is addressing large pin count packages, 120-220 pins, with leads on 20, 16.67, and 12.5 mil centers. Close center wire bonding, approximately 5 mils, and tape bonding experiments are in progress.

The initial emphasis of the 0.5-um pilot-line technology task has centered on process definition, x-ray and e-beam lithography experimentation, submicrometer test vehicle fabrication, and resulting device physics analysis. Design of an advanced submicrometer test vehicle and device and circuit modeling development are also in progress.

Process definition problems that have been addressed include thin gate oxide development, dielectric spacer, bird's beak, shallow junctions, and contacts to shallow junctions. Submicrometer n- and p-channel devices have been fabricated. The n-channel 0.8-um devices showed punch-through voltages in excess of 3 V. P-channel devices remain to be optimized. The n-channel threshold voltages varied from 0.2 V for 0.5-um gate length to 0.35-V for 5-um gatelength devices. Devices have also been fabricated using e-beam direct write on the polygate level. Devices with gate lengths down to

0.25 um are present on these wafers and will be evaluated.

A submicrometer test vehicle with three levels of design rules is being designed. Completion of the layout is expected in the next reporting period and initial first-level design rule devices are expected to be fabricated.

Chip development is presently in the preliminary design phase, the purpose of which is to define in detail producible chips which meet system requirements. The goals of this phase are specifications, block diagrams, macropartitions, I/O requirements, critical timing, and micro-instruction sets. Of the five chips, the GP controller, 16-bit AU, and pipeline AU are complete and a preliminary design document has been issued. The extended AU and the 64K memory will be completed early in the next reporting period. Analytical models, detailed macro-design, and testability analysis will be undertaken in the next reporting period.

The module development is likewise in the preliminary design phase with the goal of providing the details of module architecture required to meet system requirements. The tasks upon which efforts have been concentrated include module specifications, gate array partitions, instructions, critical timing, and I/O requirements. Of the five modules, progress has been greatest on the complex arithmetic vector processor (CAVP) and the vector scalar processor (VSP) since their architecture is dominated by the 1750A embedded computer design. The floating point processor (FPP) is following the first two modules. The hierarchical multiprocessor system controller (HMSC) module is paced to system architecture studies currently under way. The bulk memory module (BMM) is paced by both the architecture studies and the HMSC. The preliminary design specifications for these modules will be completed and

analytical models and gate array definition will be undertaken in the next reporting period.

The system development effort has concentrated on the hierarchical multiprocessor system (HMS) architecture definition and interconnection network development. The HMS study has relied on a multidisciplined team to address scheduling algorithms, software, hardware, interconnection networks, and their interrelations. Architectures being evaluated include distributed and centralized control structures. During the next reporting period the definition of the low-speed computer bus will be completed and the high-speed bus definition begun. The baseline structure will be finalized and interconnection networks defined.

The brassboard support software task is addressing signal-processing aids, the Ada compiler, and the operating system. A structured Ada methodology for signal processing has been selected. This technique allows systems analysts to define an operational problem as a set of graphs. The nodes of the graphs are Ada tasks along with control and data transfers. To support these tasks a signal-processing instruction set has been defined.

The Ada compiler study is defining the requirements of the front end, the optimization processor, and post processor. The current plan is to employ Army/Soitech front end. However, schedule incompatibility is generating difficulty in implementing the plan. Optimization techniques are being selected. The post-processor definition is being paced by the HMS studies. The kernal and radar operating system definitions are also being paced by the HMS study.

Radar system mission analysis studies were used to identify baseline radar modes and sequences of radar modes for the ATF brassboard. These, in turn, were analyzed to determine their

algorithms, content, and nature. Likewise, the algorithms are being analyzed to determine their signal processing instruction mix. The end result of this analysis is to generate time lines and work-load descriptions to feed the brassboard simulations.

The system simulation has centered on two areas. The first of these, ECSS II, is directed toward simulating the whole brassboard system under specified workloads. A simplified two processor model has been run. A complete brassboard model aimed at simulating a real time radar input buffer is near completion. The second simulation task is to generate an ATF performance baseline on an eclipse computer. The synthetic aperture radar (SAR) mode algorithms selected for brassboard implementation are presently resident on this computer and are being further developed for use in the performance baseline. Detailed descriptions of

three major functional blocks as applied to the brassboard have been completed.

The CAD package is an integrated package centered around a data-base manager and running on a CYBER computer. The data-base manager and ASSIST simulator are in place. For high-level description and simulation, the ISPS language/simulator is to be added to the system. An automatic test pattern generator and fault simulator are to be moved onto the CYBER from a UNIVAC. A gate array router, a custom layout package, and symbolic layout package are under development.

For current design utilization, a data base translator has been written to allow team members access to common information. Training has been held for team members to allow early application of ISPS for functional simulation and design validation.