

L 49253-54

ACCESSION NR: AP5008392

mode of operation and component characteristics; (2) Dynamic features of the stable states (such as frequency of harmonic oscillations, duration or phase of a periodic pulse train) do not depend on the multistable element but rather on the external master sources and, hence, are independent of circuit parameters in a fairly wide range; (3) The availability of the various dynamic stable-state features not only permits their use for presentation of numbers but also opens up the possibility for developing a special logic for every feature. Orig. art. has: 15 figures and 8 formulas.

ASSOCIATION: none

SUBMITTED: 09Jun64

ENCL: 00

SUB CODE: EC

NO REF SOV: 004

OTHER: 001

JO  
Card 2/2

L 51371-65 EWP(k)/EWA(h)/EWT(d)/EWT(1)/EWP(h)/EWP(1)/EWP(v) Pf-4/Feb GS  
 UR/0000/64/000/000/0549/0553

ACCESSION NR: AT5011628

AUTHOR: Sitnikov, L. S.; Utyakov, L. L.

TITLE: Multifrequency triggers with magnetizable cores

SOURCE: Vsesoyuznoye soveshchaniye po magnitnym elementam avtomatiki, tele-  
mekhaniki, izmeritel'noy i vychislitel'noy tekhniki, Lvov, 1962. Magnitnyye ele-  
menty avtomatiki, telemekhaniki, izmeritel'noy i vychislitel'noy tekhniki  
 (Magnetic elements of automatic control, remote control, measurement and computer  
 engineering); trudy soveshchaniya. Kiev, Naukova dumka, 1964, 549-553

TOPIC TAGS: multifrequency trigger, magnetic core trigger, discontinuous  
 automation

ABSTRACT: Different stable states in systems with several stable states differ  
 from one another by the associated value of some physical parameter. One such  
 parameter may be the frequency (each stable state being characterized by another  
 frequency) and M. S. Neyman emphasized earlier (Radiotekhnika, 1960, no. 10) the  
 future possible uses in discontinuous automation of the shifts from one possible  
 self-excitation condition to another. In the present work, sponsored by Doctor  
 of Technical Sciences V. P. Sigorskiy, the authors discuss several approaches to

Card 1/4

L 51371-65

ACCESSION NR: AT5011628

the construction of multi-frequency triggers, One version comprising a variable frequency generator of sinusoidal oscillations is shown in Fig. 1 of the Enclosure and has  $n+1$  stable states. They also investigated square-wave starting. Another, three-transistor unit shown in Fig. 2 of the Enclosure has 6 stable states with the following properties:  $I = 2, 5, 8, 11, 15$  and  $19$  mA and  $f = 0.85, 1.2, 1.5, 1.75, 1.9$  and  $2.0$  megacycles/sec., respectively, for states No. 1 through No. 6. A further increase in the number of stable states may be attained by utilizing high-quality delay lines with low frequencies and low phase distortions. Orig. art. has: 6 formulas, 5 figures, and 3 tables.

ASSOCIATION: none

SUBMITTED: 29Sep64

NO REF SOV: 003

ENCL: 02

OTHER: 002

SUB CODE: EC, DP

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L 51371-65  
ACCESSION NR: AT5011628

ENCLOSURE: 01

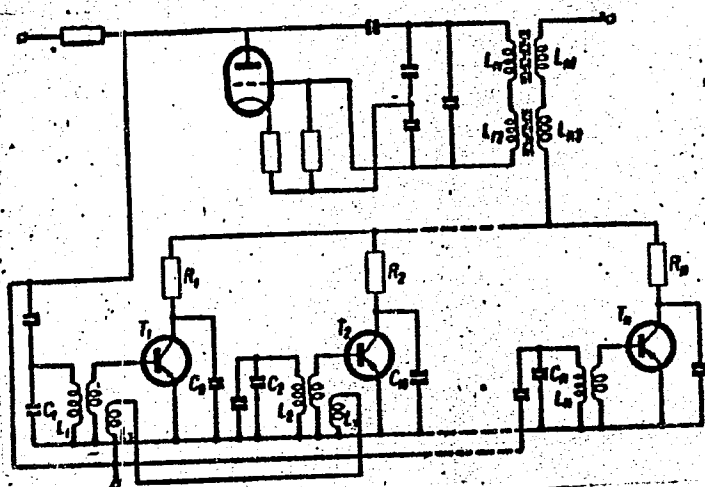


Fig. 1. Multifrequency trigger with a sinusoidal frequency generator.

Card 3/4

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ACCESSION NR: AT5011628

ENCLOSURE: 02

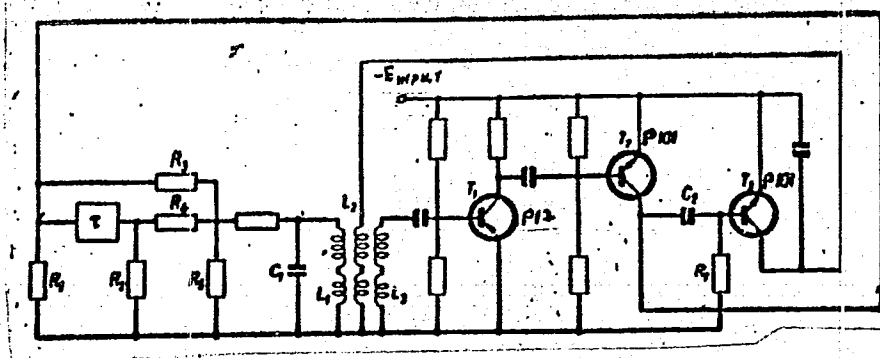


Fig. 2. Multifrequency trigger with electromagnetic LZ-0, 2-1200 lines as delay elements.

Card 4/4 MB

L 54551-65 EWT(d)/EED-2/EWP(1) Pq-4/Pg-4/Pk-4 IJP(c) BB/CG  
ACCESSION NR: AP5015526 UR/0286/65/000/008/0065/0065

AUTHORS: Sigorskiy, V. P.; Sitnikov, L. S; Utyakov, L. L.

TITLE: Pulse counter modulo n. Class 42, No. 170205

SOURCE: <sup>160</sup>Byulleten' izobreteniy i tovarnykh znakov, no. 8, 1965, 65

TOPIC TAGS: pulse counter 10

31  
B

ABSTRACT: This Author Certificate presents a pulse counter modulo n containing a multistable unit and a shift circuit. To simplify the device (using a phase-pulse multistable unit with two inputs), the counter input of each multistable unit is connected to the output of a coincidence circuit (see Fig. 1 on the Enclosure). The clock pulse inputs of all the units are connected to a clock pulse generator. The unit outputs are connected to the first input of the coincidence circuit, whose second inputs are connected to the inputs of a reference multistable unit. The coincidence circuit outputs are also connected to the input for resetting the unit to its initial state. The first multistable unit has a scaling coefficient equal to n, and that of the following units is equal to n + 1. Orig. art. has: 1 diagram.

ASSOCIATION: Institut matematiki, SO AN SSSR (Institute of Mathematics, SO AN SSSR)

Card 1/02 *submitted: 17 Feb 64*

I. 54549-65 EWT(d)/EED-2/EWP(1) Pq-4/Pg-4/Pk-4 LJP(c) BE/GG  
UR/0286/65/000/008/0066/0066

ACCESSION NR: AP5015527

AUTHORS: Piskunov, S. V.; Sigorskiy, V. P.; Sitnikov, L. S.; Utyakov, L. L.

TITLE: Summator with pulse width representation of numbers. Class 42, No. 29  
170208 16C B

SOURCE: Byulleten' izobreteniy i tovarnykh znakov, no. 8, 1965, 66

TOPIC TAGS: summator

ABSTRACT: This Author Certificate presents a summator with pulse width representation of numbers, containing multistable time-pulse units. One unit is connected through an "OR" circuit, which is connected to the transfer output of the preceding summator digit, to the first inputs of a second "OR" circuit and an "AND" circuit, whose second inputs are connected to the other unit (see Fig. 1 on the Enclosure). There are also a third "OR" circuit forming the sum modulo ten and a transfer pulse shaper section. To utilize high stability chronotrons, a shaping circuit is connected between the second and third "OR" circuits. The supply inputs of the multistable time-pulse units are connected to sources of forward and additional reference voltages. Orig. art. has: 1 diagram.

ASSOCIATION: Institut matematiki, SO AN SSSR (Institute of Mathematics, SO AN SSSR)

Card 1/2

L 54549-65

ACCESSION NR: AP5015527

SUBMITTED: 21Jan64

ENCL: 01

SUB CODE: DP <sup>0</sup>

NO REF SOV: 000

OTHER: 000

Card 2/2 2



L 54545-65 EWT(d)/EED-2/EWP(1) Pg-4/Pg-4/Pk-4 IJP(c) BB/GG

ACCESSION NR: AP5015531

UR/0286/65/000/008/0067/0067

AUTHORS: Vishnevskiy, A. P.; Koyfman, A. A.; Sigorskiy, V. P.; Sitnikov, L. S.;  
Utyakov, L. L.

TITLE: Decimal storage summator <sup>166</sup> Class 42, No. 170212

SOURCE: Byulleten' izobreteniy i tovarnykh znakov, no. 8, 1965, 67

TOPIC TAGS: summator, storage device

ABSTRACT: This Author Certificate presents a decimal storage summator containing triggers, switches, and "OR" circuits. To construct the summator of a phase-pulse unit and to decrease its cost, an "OR" circuit (connected to a source of zero reference pulses and to a pulse number detector) is connected to the dynamic input of the phase-pulse unit. The zero trigger input of a phase-to-pulse number converter is connected to the second term pulse source and the one input is connected to the zero reference pulse source. The trigger output is connected to one of the inputs of a coincidence circuit, whose other two inputs are connected to the summation solution output and to a source of clock pulses shifted by half of the high cycle. The coincidence circuit output is connected to one of the inputs of an "OR" circuit, whose other two inputs are connected to the clock pulse source

Card 1/2

L 54545-65

ACCESSION NR: AP5015531

and to the output of the transfer circuit of the preceding digit. The output of the "OR" circuit is connected to the counter input of the phase-pulse unit, whose first output is connected to the zero input of the transfer circuit trigger. The one input of the trigger is connected to a source of pulses shifted by half the period of the clock pulses relative to the zero reference pulses. The trigger output is connected to the first input of an "AND" circuit, whose second input is connected to the second output of the phase-pulse unit.

ASSOCIATION: Institut matematiki, SO AN SSSR (Institute of Mathematics, SO AN SSSR)

SUBMITTED: 10Mar64

ENCL: 00

SUB CODE: DP, EC

NO REF SOV: 000

OTHER: 000

Card <sup>1/2</sup> 2/2

L 51508-65 EWT(d)/EEC(f)/BXT/EED-2/EMP(1) Pq-4/Pg-4/Pk-4 IJP(c) BB/GG  
ACCESSION NR: AP5015339 UR/0286/65/000/009/0092/0092  
681.142 65

40  
B

AUTHOR: Vishnevskiy, A. P.; Sigorskiy, V. P.; Sitnikov, L. S.; Utyakov, L. L.

TITLE: A method for recording and retrieval of information in an N-valued memory.  
Class 42, No. 170755 160

SOURCE: Byulleten' izobreteniy i tovarnykh znakov, no. 9, 1965, 9?

TOPIC TAGS: information storage, computer memory, frequency spectrum, line spectrum

ABSTRACT: This Author's Certificate introduces a method for recording and retrieval of information in an N-valued matrix type spectrotron memory. The method makes use of selected spectrotrons only. In the initial state, the first phase supply voltage is fed to all vertical busses. This voltage has a frequency line spectrum with harmonic phases which are shifted by  $120^\circ$  with respect to the corresponding harmonics of the second phase supply spectrum. The second phase voltage is fed to all horizontal busses. During information recording, a supply spectrum with harmonic

Card 1/2

L 51508-65

ACCESSION NR: AP5015339

0

phases shifted by  $120^\circ$  with respect to the supply spectra fed to all busses in the initial state is first fed to the horizontal and vertical busses which intersect at the chosen memory element. The horizontal bus is then disconnected from the supply voltage, and the first or third phase of the  $i$ -harmonic with frequency which corresponds to the voltage information being recorded is fed to the vertical bus. After the spectrotron circuit is tuned to this frequency, there is a transition to the initial state. The spectrotron then remains tuned to the  $i$ -harmonic frequency. In reading out the information from the spectrotron, a voltage with an am frequency spectrum is first fed to the horizontal bus which is connected to the chosen spectrotron, and the vertical bus is connected to the readout amplifier. The output circuits of the readout amplifier are tuned to the upper side frequencies of the am spectrum. The device is then returned to the initial state.

ASSOCIATION: none

SUBMITTED: 14Jan63

ENCL: 00

SUB CODE: DP

NO REF SOV: 000

OTHER: 000

Card *er* 2/2

L 51111-65 EWT(d)/EED-2/EWP(1) Pq-4/Pg-4/Pk-4 IJP(c) BB/GG  
ACCESSION NR: AP5015523 UR/0286/65/000/008/0064/0064  
681.14

37  
36  
B

AUTHOR: Boyko, A. N.; Sitnikov, L. S.; Sigorskiy, V. P.; Utyakov, L. L.

TITLE: An adder. Class 42, No. 170202

SOURCE: Byulleten' <sup>160</sup> izobreteniy i tvarnykh znakov, no. 8, 1965, 64

TOPIC TAGS: logic, circuit, adder, computer

ABSTRACT: This Author's Certificate introduces an adder which contains a chronotron, pulse shift logic circuits, flip-flops, "AND" or "OR" logical elements. The device is designed for improving the reliability of adders with pulse-time number representation. The first logical shift circuit is connected to the chronotron where the first addend is stored and to the first input of the second logical shift circuit. The first input of the first logical shift circuit is connected to a source which supplies a sequence of short trigger pulses. The second input of the first logical shift circuit is connected to the carry output for the preceding digit. The second input of the second logical shift circuit is connected to the chronotron where the first addend is stored, while the output of this circuit is

Card 1/4

L 51114-65

ACCESSION NR: AP5015523

connected to the first input of the third logical shift circuit. The second input of the third logical shift circuit is connected to the chronotron where the second addend is stored, the output of the third circuit is connected to the unit input of the first flip-flop for storage of the sum, and the neutral input of this circuit is connected to the source of short trigger pulses. The chronotrons for storage of the first and second addends are connected to the first and second inputs of the "OR" gate respectively. The output of the "OR" gate is connected to the first input of the first "AND" gate. The second input of the "AND" gate is connected to a source of short pulses which are shifted with respect to the pedestal pulse sequence by an interval which corresponds to some number greater than the base of the number system minus 1 and less than the base of the number system. The output of the first "AND" gate is connected to the unit input of the first flip-flop. The neutral input of this flip-flop is connected to a source of pulses which are shifted by half a period. The flip-flop output is connected to the first input of the "AND" gate which forms the carry. The second input of this gate is connected to a source of unit duration pulses. The phase of these pulses coincides with the phase of the pedestal pulse sequence.

ASSOCIATION: Institut matematiki SO AN SSSR (Institute of Mathematics, SO AN SSSR)

Card 2/4

L 51114-65

ACCESSION NR: AP5015523

SUBMITTED: 23Dec63

NO REF SOV: 000

ENCL: 01

OTHER: 000

SUB CODE: DP

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L 51414-65  
ACCESSION NR: AP5015523

ENCLOSURE: 01

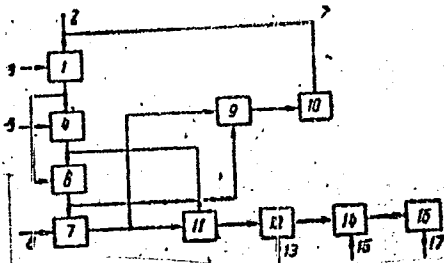


Fig. 1. 1--logical shift circuit; 2--short trigger pulse sequence; 3--carry for previous digital place; 4--chronotron where the first addend is stored; 5--input for the first addend; 6--logical shift circuit; 7--chronotron where the second addend is stored; 8--input for the second addend; 9--logical shift circuit; 10--sum flip-flop; 11--logical "OR" gate; 12--logical "AND" gate; 13--sequence of pulses which are shifted with respect to the pedestal pulses by an interval greater than  $R-1$  and less than  $R$ , where  $R$  is the base of the number system; 14--flip-flop; 15--pulses for return to the initial state which are shifted by half a period with respect to the pedestal pulses; 16--"AND" gate; 17--pulse of unit duration

Card 4/4



L 60367-65

ACCESSION NR: AP5019074

UR/0286/65/000/012/0102/0102  
681.142.642.9

15  
14

AUTHORS: Sitnikov, L. S.; Utyakov, L. L.

TITLE: Scaling circuit. Class 42, No. 172130

SOURCE: Byulleten' izobreteniy i tovarnykh znakov, no. 12, 1965, 102

TOPIC TAGS: scaling circuit

ABSTRACT: This Author Certificate presents a scaling circuit containing triggers, coincidence circuits, "OR" circuits, phase-pulse multistable units, a cadence pulse source, and a trigger pulse source. To simplify the device and to increase its reliability, the cadence pulse source is connected through a delay circuit to the first input of a coincidence circuit whose second input is connected to a trigger (see Fig. 1 on the Enclosure). The one input of the trigger is connected to the trigger pulse source, and its zero input is connected to the counter input of the scaling circuit which is connected through a shaper to the coincidence circuit input. The cadence pulse generator is connected to all the first inputs of the "OR" circuits which are connected to the inputs of the phase-pulse units. The second input of the first "OR" circuit of any following unit is connected to the inputs of the preceding. The scaling coefficient of the phase-pulse unit of

Card 1/3

L 60367-65

ACCESSION NR: AP5019074

the first digit is per unit less than the scaling coefficient of the remaining phase-pulse units. Orig. art. has: 1 diagram.

ASSOCIATION: Institut matematiki, SO AN SSSR (Institute of Mathematics, SO AN SSSR)

SUBMITTED: 04May64

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ACCESSION NR: AP5019074

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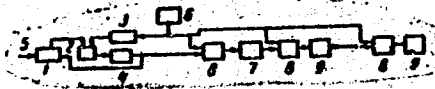


Fig. 1.

- 1- trigger; 2- "AND" circuit; 3- delay circuit; 4- shaper;
- 5- counter pulse input; 6- cadence pulse generator;
- 7- phase-pulse unit with scaling coefficient  $n = 1$ ;
- 8- two-way "OR" circuit; 9- phase-pulse multistable unit with scaling coefficient  $n$

Card 3/3 KC

L 2775-66 EWT(d)/EED-2  
ACCESSION NR: AP5022018

UR/0286/65/000/014/0087/0088

40  
38  
B

AUTHOR: Zakirzyanov, Z. Sh.; Sitnikov, L. S.; Utyakov, L. L.

TITLE: A pulse repetition frequency divider. <sup>44</sup> Class 42, No. 173032

SOURCE: Byulleten' izobreteniy i tovarnykh znakov, no. 14, 1965, 87-88

TOPIC TAGS: pulse recurrence, pulse position modulation, <sup>44</sup> frequency divider

ABSTRACT: This Author's Certificate introduces a pulse repetition frequency divider which contains multistable pulse-position elements. The device is designed for giving frequency division coefficients as high as desired and output pulse repetition frequencies as low as desired with a rather simple circuit and unified division stages. The input to each pulse-position element is connected through a two-input OR gate to the input of the preceding pulse-position element and to the input of the external pulse source. The input to the first pulse-position element is connected to the external pulse source. The outputs from the first and second elements are connected to the inputs of the first coincidence gate. The output from the first coincidence gate and that from the third pulse-position element are connected to the inputs of the second coincidence gate. The output from the k-th coincidence gate and

Card 1/3

L 2775-66

ACCESSION NR: AP5022018

from the  $(k-2)$ -th pulse-position element are connected to the  $(k-1)$ -th coincidence gate.

ASSOCIATION: Institut matematiki SO AN SSSR (Institute of Mathematics, SO AN SSSR)

SUBMITTED: 21Jul64

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SUB CODE: EC

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OTHER: 000

Card 2/3

L 2775-66

ACCESSION NR: AP5022018

ENCLOSURE: 01

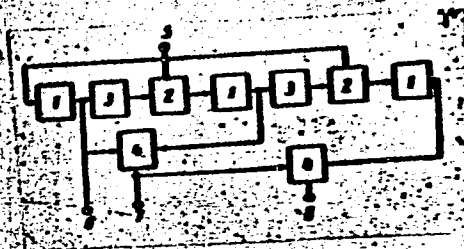


Fig. 1. 1--multistable pulse-position element; 2--OR gate; 3--delay cell; 4--coincidence gate; 5--cadence frequency pulse input; 6--first output; 7--second output; 8--third output.

Card 3/3 *hd*

SIGORSEY, Vitaliy Petrovich; SHNIKOV, Leonid Semenovich,  
STYABOV, Lev Lazarevich, BASTOVA, ... , Eds.

[Networks with multiple steady-states] Skhemy s mnogimi  
ustoychivymi sostoyaniami. Novosibirsk, Red. izd- otdei  
fizicheskogo otb-ntsa AN SSSR, 1965. 140 p.  
(MIR: 18:11)

L 7039-66 EWT(a)/NMP(1) IJF(c) BB/GG

ACC NR: AP5026810

SOURCE CODE: UR/0286/65/000/017/0092/0092

AUTHOR: Sigorskiy, V. P.; Sitnikov, L. S.; Utyakov, L. L.

43  
53

ORG: none

TITLE: A parallel cumulative decimal summation unit. Class 42, No. 174439 [announced by Institute of Mathematics, Siberian Department, AN SSSR (Institut matematiki Sibirskogo otdeleniya AN SSSR)]

SOURCE: Byulleten' izobreteniy i tovarnykh znakov, no. 17, 1965, 92

TOPIC TAGS: arithmetic unit, computer component, flip flop circuit, coincidence circuit, adder

ABSTRACT: This Author's Certificate introduces a parallel cumulative decimal summation unit which contains multistable pulse-position elements, "OR" gates, flip-flops and coincidence circuits. The circuitry of the device is simplified by connecting the input of the multistable pulse-position cell for each digit through an "OR" gate to the output of the coincidence circuit for the preceding digit, and to the output of the dynamic flip-flop for the given digit. The set terminal of this flip-flop is connected to the addend pulse source, the reset terminal is connected to the pedal pulse train source, and the cadence pulse input is connected to the cadence pulse source..

UDC: 681.142.07

Card 1/2



L 7039-66

ACC NR: AP5026810

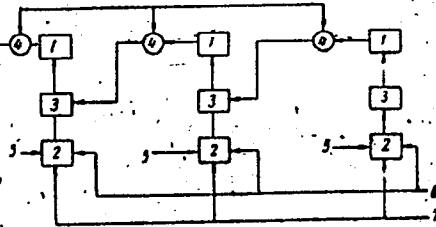


Fig. 1. 1--multistable pulse-position cell; 2--dynamic flip-flop; 3--"OR" gate; 4--nonsimultaneous coincidence circuit; 5--addend pulse input; 6--cadence pulse input; 7--pedestal pulse train input

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SUBM DATE: 03Aug64/

ORIG REF: 000/

OTH REF: 000

PC  
Card 2/2

L 20665-66 EWT(1)/EWA(h)  
 ACC NR: AP6004556 SOURCE CODE: UR/0103/66/000/001/0133/0138  
 AUTHOR: Sigorskiy, V. P. (Kiev); Sitnikov, L. S. (Kiev); Utyakov, L. L. (Kiev)  
 ORG: none

48  
 B

TITLE: <sup>25</sup> Chronotrons: time-pulsed multistable elements

SOURCE: Avtomatika i telemekhanika, no. 1, 1966, 133-138

TOPIC TAGS: pulse generator, pulse modulation, pulse rate, chronotron

ABSTRACT: It was shown earlier by the authors that a chronotron may be designed by incorporating a four-terminal network in a feedback loop. One of the common versions of such a four-terminal network is shown in Fig. 1.

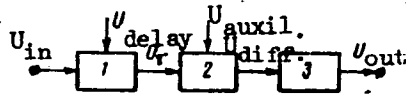


Fig. 1. An all-purpose four-terminal network.  
 1 - controlled delay; 2 - switching block;  
 3 - averaging filter.

Card 1/2

L 20665-66

ACC NR: AP6004556

The authors investigate this and other versions of multistable elements which are characterized by their d-c output voltage and the duration of the square wave pulses. The paper contains a brief outline of the theory, block diagrams of the elements, graphs of the voltages, and a circuit diagram. The control of such an element, i.e., the shift of its operation from one steady state to another is carried out by switching the circuit briefly from the univibrator output to an external source of pulses having the required duration. Orig. art. has: 6 formulas, 8 figures, and 1 table. [08]

SUB CODE: 09 / SUBM DATE: 19May65 / ORIG REF: 003/ ATD PRESS: 4223

Card 2/2 BK

L 30400-66 EWT(d)/FSS-2

ACC NR: AP6007864

SOURCE CODE: UR/0103/66/000/002/0076/0081

AUTHOR: Sigorskiy, V. P. (Kiev); Sitnikov, L. S. (Kiev); Utyakov, L. L. (Kiev)

42  
B

ORG: none

TITLE: Pulse-frequency multistable components

SOURCE: Avtomatika i telemekhanika, no. 2, 1966, 76-81

TOPIC TAGS: electronic component, stabilizer, RF pulse, frequency stability

ABSTRACT: The present article investigates the means of development and the basic characteristics of multistable components of a group the states of which are distinguished according to the value of the output voltage of the frequency sequence of the pulses generated. For the development of such components use may be made of the nonlinear four-pole component, which includes the converters of voltages into frequency sequences of pulses and frequencies into voltage. It is concluded that when a synchronized controlled relaxation generator is included in a feedback loop with an inertia link there is the possibility of creating sufficiently simple components with many unstable states, distinguished by an oscillation period of the relaxation generator and the magnitude of the control voltage at the output of the discriminator. The magnitude of the state is controlled by altering the frequency of the sequence of synchronization pulses. The advantage of the proposed device is that even with the utilization of the generator with the nonlinear control characteristic its period of oscillation in the transition of the component from any state to a neighboring state changes by a rigidly

Card 1/2

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L 30400-66

ACC NR: AP6007864

fixed constant equal to the synchronization voltage period. The utilization of the relaxation generator with linear control makes it possible to considerably increase the number of stable states and to assure a constant increment of the control voltage in the transition of one state to another. Orig. art. has: 6 figures, 7 formulas, and 3 tables. D

SUB CODE: 09 / SUBM DATE: 01Sep64 / ORIG REF: 002

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L 25652-66

ACC NR: AM6011889

Monograph

UR/

Sigorskiy, Vitaliy Petrovich; Sitnikov, Leonid Semenovich; Utyakov, Lev Lazarevich <sup>30</sup>

BT/

Circuits with many stable states. (Skhemy s mnogimi ustoychivymi sostoyaniyami) Novosibirsk, Redizdat Sib. otd. AN SSSR, 1965. 140 p. illus., biblio. (At head of title: Akademiya nauk SSSR. Sibirskoye otdeleniye) 1000 copies printed.

TOPIC TAGS: computer application, computer design, computer research, computer technology

PURPOSE AND COVERAGE: This book is intended for scientific and technical personnel concerned with computers, automation, simulation of processes in the nervous systems of living organisms, and other fields in which circuits with many stable states may find application. The book contains the main results of theoretical and experimental investigations concerned with finding new principles for developing such circuits. The possibility of developing elements with many stable states, whose quantity is determined by the operating conditions and the parameters of the circuit (independent of its complexity), is demonstrated. A method for developing such elements, based on the conversion of static and time characteristics into comb- or step-

Card 1/3

2

L 25652-66

ACC NR: AM6011889

type amplitude characteristics, is proposed. Stability is investigated, and the transients of the general block-diagram of an element with many stable states are analyzed, making it possible to evaluate various control methods from the standpoint of fast response and criticality with regard to the controlling-effect parameters. A number of specific circuits, checked under laboratory conditions, is proposed. Harmonic-frequency (spectrotron), time-pulse (chronotron), and pulse-frequency (synchrotron) circuits proved to be the most promising. In laboratory specimens ten or more states of stable equilibrium were easily obtained. In addition to the authors, A. N. Boyko, A. P. Vishnevskiy, A. A. Molchanov, Yu. S. Osyagin, E. Ye. Bartlemanov, V. A. Yelkin, Ya. Sh. Zakirzyanov and A. R. Turuk participated in the research.

TABLE OF CONTENTS:

Introduction -- 3

Ch. I. General Principles for Developing Elements With Many Stable States -- 5

1. Survey of elements with many states of equilibrium -- 5

Card 2/3

L 25652-66

ACC NR: AM6011889

- 2. Principles of the development of elements with many stable states -- 18
- 3. Dynamics of elements with many stable states -- 37
- 4. Ways of handling elements with many stable states -- 50
  
- Ch. II. Harmonic-Frequency Elements -- 59
  - 1. Basic types of harmonic-frequency elements -- 59
  - 2. Spectrotrons -- 76
  - 3. Methods of controlling spectrotrons -- 90
  
- Ch. III. Pulse Elements -- 101
  - 1. Basic types of pulse elements -- 101
  - 2. Pulse-frequency elements -- 103
  - 3. Chronotrons -- 113
  - 4. Some ways of improving chronotrons -- 124

BIBLIOGRAPHY -- 139

SUB CODE: 09/ SUBM DATE: 14Jan65/ ORIG REF: 022/ OTH REF: 009

Card 3/3 *FV*



ACC NR:AM6015099

TABLE OF CONTENTS

Foreword -- 3

Ch.I. General Principles for the Development of High-Stability Elements

1. Review and classification of elements with numerous states of equilibrium -- 9
2. High-stability elements using nonlinear two-terminal networks -- 16
3. High-stability elements using nonlinear four-terminal networks -- 21
4. Four-terminal networks with a nonlinear amplitude characteristic -- 32
5. Dynamics of high-stability elements -- 43
6. Control of high-stability elements -- 53

Ch.II. Frequency-Harmonic Elements

1. Controlled reactances and oscillators -- 63
2. Basic types of frequency-harmonic elements -- 82
3. The coordinates and quantity of stable states of a spectrotron -- 90

Card 2/4

ACC NR:AM6015099

Bibliography -- 351

SUB CODE: 09/ SUBM DATE: 21Jan66/ ORIG REF: 128/ OTH REF: 041

Card 4/4

ACC NR: AP7005660

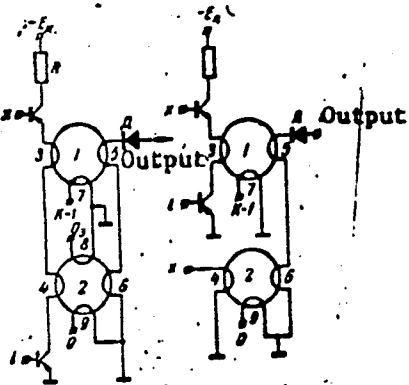


Fig. 1. Logic element

1, 2 - Ferrite cores; 3, 4 - input windings; 5, 6 - output windings; 7, 8 - read windings; 9 - restoration winding; x, i - input signals.

$$j_i(x) = \begin{cases} k-1 & \text{for } x = i \\ 0 & \text{for } x \neq i \end{cases}$$

where x and i = 0, 1, 2... k - 1, the input windings are connected in parallel and the output windings in series. Both types of winding are connected through a diode to the output terminals of the device. In order to process the characteristic function  $j_i(x)$  at i = 0, the input winding is located on a single core. Orig. art. has: 1 figure. [09]

SUB CODE: 09/ SUBM DATE: 15Oct65/ ATD PRESS: 5116

Card 2/2

SITNIKOV, M.A., inzhener; MITROFANOV, S.A.

Automatic stop for the "Piener" crane. Rats. i izobr. predl.v  
stroi. no.119:7-8 '55. (MIRA 9:7)  
(Cranes, derricks, etc.)

SITNIKOV, M.A., inzhener.

Casting precast cornices in packet forms. Rats. i izobr.predl. v stroi.  
no.123:26-27 '55. (Cornices) (MIRA 9:7)

SITNIKOV, M., inzh. (g. Minsk)

Large-panel foundations of a new type. Na stroi. Mosk. 1 no.12:27  
D '58. (MIRA 11:12)  
(Foundations) (Concrete slabs)

SITNIKOV, M., inzh.

Using lightweight glass-concrete in laying floor foundations.  
Stroitel' no.5:23 My '58.

(MIRA 11:6)

(Minsk--Floors, Concrete)

SITNIKOV, M. A. Cand Tech Sci -- (diss) "Certain problems of the industrialization of construction of foundations ~~of~~<sup>of</sup> buildings." Minsk, 1959. 24 pp with illustrations (Min of Higher and Secondary Specialized Education BSSR. Belorussian Polytechnic Inst im I. V. Stalin. Chair of Bases and Foundations), 150 copies (KL, 44-59, 127)



SITNIKOV, M.A., inzh.

New industrial foundations for buildings. Transp.stroi. 9  
no.1:33-34 Ja '59. (MIRA 12:2)  
(Foundations)

SITNIKOV, M.

Precast reinforced lightweight concrete staircases. Zhil.-kom.  
khoz. 9 no.2:22-23 '59. (MIRA 12:5)

1. Nachal'nik tekhnicheskogo otdela tresta "Beltransstroy,"  
Minsk.

(Lightweight concrete) (Staircases)

SITNIKOV, M.A., inzh.

Some problems in constructing foundations in White Russia.  
Sbor. nauch. rab. Bel. politekh. inst. no.77:67-89 '59.  
(MIRA 13:3)

(White Russia--Foundations)

SMIRNITSKIY, Yevgeniy Konstantinovich; GOLUBEVA, K.A., inzh., retsen-  
zent; MASLIY, K.Ya., zuborez, retsenzent; ZHUKOV, P.A., kand.  
ekon.nauk, red.; SITNIKOV, M.A., red. vypuska; BELYAKOV, M.N.,  
red.; ROZENBERG, I.A., kand.ekon.nauk, red.; SMIRNITSKIY, Ye. K.,  
kand.ekon.nauk, red.; SUSTAVOV, M.I., inzh., red; DUGINA, N.A.,  
tekh.n.red.

[Machinery-industry worker and technological innovations] Ra-  
bochii-mashinostroitel' i tekhnicheskii progress. Moskva,  
Mashgiz, 1960. 49 p. (Biblioteka rabocheho mashinostroitelia.  
Seria: "Osnovy konkretnoi ekonomiki," no.1) (MIRA 14:5)  
(Machinery industry--Technological innovations)

SITNIKOV, M.A. (Minsk)

Making and assembling large-panel foundations of buildings.  
Osn., fund.i mekh.grun. 2 no.4:22-24 '60. (MIRA 13:7)  
(Foundations)

SITNIKOV, M.A., kand. tekhn. nauk

Water-resistant gypsum-cement concrete products. Transp. stroi.  
ll no.7:32-34 J1 '61. (MIRA 14:7)  
(Minsk--Precast concrete)

MAKAROCHKIN, Mikhail Fedorovich, doktor tekhn.nauk; SITNIKOV,  
Mikhail Aleksandrovich, kand. tekhn. nauk; POL'SKIY, S.,  
red.; BELEN'KAYA, I., tekhn. red.

[Prefabricated foundations for buildings] Industrial'nye  
fundamenty zdaniy. Minsk, Gos.izd-vo BSSR, 1962. 300 p.  
(MIRA 16:7)

(Foundations)

SITNIKOV, M.A., kand.tekhn.nauk

Mastering the production of gypsum-cement-pozzolan articles  
for precast construction. Stroi.mat. 8 no.3:16-17 Mr '62.  
(MIRA 15:8)

(Building materials industry)



SITNIKOV, M.A., kand.tekhn.nauk

Construction of reinforced concrete stressed containers for petroleum products. Transp. stroi. 12 no.2:31-33 F '62. (MIRA 15:7)  
(Tanks) (Prestressed concrete construction)

MAKAROCHKIN, Mikhail Fedorovich, doktor tekhn. nauk; SITNIKOV,  
Mikhail Aleksandrovich, kand. tekhn. nauk; POL'SKIY, S.,  
red.; BELEN'KAYA, I., tekhn. red.

[Prefabricated foundations of buildings] Industrial'nye  
fundamenty zdani. Minsk, Gps.izd-vo BSSR. Red.nauchno-  
tekhn.lit-ry, 1962. 303 p. (MIRA 16:3)  
(Foundations)

SITNIKOV, Mikhail Aleksandrovich, **kand. tekhn. nauk**; UKRAINCHIK, M.M.,  
inzh., red.

[Precast reinforced concrete reservoirs with poststressed walls; practices of the Experimental Construction Office of the All-Union Research Institute for Water Main (VNIIST), of the "Stroidetal'" Plant and the White Russian Transportation Construction Administration of the Ministry of Transportation Construction of the U.S.S.R.] Sbornye zhelezobetonnye rezervuary s posleduiushchim napriazheniem stenok; iz opyta Eksperimental'no-konstruktorskogo biuro Vsesoiuznogo nauchno-issledovatel'skogo instituta po stroitel'stvu magistral'nykh truboprovodov (VNIIST), zavoda "Stroidetal'" i Beltransstroia Ministerstva transportnogo stroitel'stva SSSR. Moskva, Gosstroizdat, 1962. 23 p. (MIRA 17:2)

1. Nachal'nik tekhnicheskogo otdela tresta "Beltransstroy" Ministerstva transportnogo stroitel'stva SSSR (for Sitnikov).

SITNIKOV, M.A. (Minsk)

Several problems concerning the erection of pile foundations.  
Osn., fund. i mekh. grun. 5 no.5:15-16 '63. (MIRA 16:10)

SITNIKOV, M.A.

Nomogram for determining the dimensions of the base  
of a foundation. Osn., fund. i mekh.grun. 8 no.1:  
27 '66. (MIRA 19:1)

SITNIKOV, M. N.

Sitnikov, M. N. "Common pine on the artificial plantations on chernozem soils of Trans-Volga Kuybyshev Oblast." Min Higher Education USSR. Saratov Agricultural Inst. Saratov, 1956. (Dissertation for the Degree of Candidate in Agricultural Science)

So: Knizhnaya letopis', No. 27, 1956. Moscow. Pages 94-109; III.

K-4

USSR / Forest Science. Forest Cultures.

Abs Jour : Ref. Zhur - Biologiya, No 17, 1958, No. 77522

Author : Sitnikov, M. N.

Inst : AS USSR

Title : Test of Common Pine Cultivations on Chernozem Soils of  
Kuybyshevskaya Oblast

Orig Pub : Botan, sb. rabot Kuybyshevsk. otd. Vses. botan. o-va,  
M.-L., AN SSSR, 1956, 27-35

Abstract : Common pine on chernozem soils in the forest-steppe  
and steppe zones of Kuybyshevskaya Oblast is a stable and  
long-lived species and forms highly-productive stands.  
The best condition of pine plantations and their most  
successful growth are observed in the forest-steppe zone.  
In the Kuybyshevskaya Oblast, pine can be cultivated in  
pure and mixed plantations on chernozem soils. Norway  
maple, green and common ash, linden, birch and oak are

Card 1/2

28

COUNTRY : USSR  
 CATEGORY : Forestry. Forest Cultures. K  
 RES. JOUR. : RZhBiol., No. 1, 1959, No. 15513  
 AUTHOR : Dnestrovskiy, G.P.; Arsenas'iyev, S.P.; Sitnikov, M.N.  
 INST. : Kuzbassovsk. agric. Inst.  
 TITLE :  
 ORIG. PUB. : Trasn-Volga Area.  
 ABSTRACT :  
 The use of 25-year old plantations of common pine on the left bank of the Volga in mixed stands is discussed. It is stated that under the conditions of these lands a pine of class 1-2 is the best, even in the case of a high yield. The pine is distinguished by its high productivity and the pine and spruce plantations are distinguished for their

CARD: 1/2

RES. JOUR. : RZhBiol., No. 1, 1959, No. 15513  
 AUTHOR :  
 INST. :  
 TITLE :  
 ORIG. PUB. :  
 ABSTRACT :  
 higher commodity value and wood resources. It is recommended that the common pine be used in forest cultures on the chernozem soils of the left bank of the Volga.

CARD: 2/2



SIPNIKOV, M. I.

Coal-Mining Machinery

Equations of the motions of a cutting machine. Nauch. trudy Mosk. gor. inst. No. 8 1950

Monthly List of Russian Accessions Library of Congress October 1952 Unclass.

SITNIKOV, M.P.

DANCHEV, V.I.; KORNILOV, A.M.; NEYMYSHV, M.V.; OL'KHA, V.V.;  
PROSHIYAKOV, B.K.; STRELYANOV, N.P.; SITNIKOV, M.P.

Uranium mineralization in carbonate sedimentary rocks.  
Geol.rud.mestorozh. no.6:27-38 H-D '59. (MIRA 13:7)  
(Uranium ores)

SITNIKOV, N.A., kand.tekhn.nauk

Using industrial methods in constructing the foundations of  
buildings. Transp.stroi 10 no.4:34-35 Apr '60. (MIRA 13:9)  
(Foundations) (Precast concrete construction)

PETROV, I.P., kand. tekhn. nauk; SEMENTSOV, G.M., inzh.; SITNIKOV, N.B.,  
inzh.

Automatic control of cutting machines and mining cutter-loaders.  
Izv. vys. ucheb. zav.; gor. zhur. no.8:132-136 '64 (MIRA 18:1)

1. Sverdlovskiy gornyy institut imeni V.V. Vakhrushcheva. Rekomen-  
dovana kafedroy gornoy elektrotekhniki.

PETROV, I.P., dotsent; SEMENSOV, G.N., inzh.; SITNIKOV, N.B., inzh.

Regulating the power consistency of the rotary mechanism motor  
on the SBUE-150-7IV boring machine. Izv. vys. ucheb. zav.; gor.  
zhur. 7 no.10:146-151 '64. (MIRA 18:1)

1. Sverdlovskiy gornyy institut imeni V.V. Vakhrusheva. Rekomen-  
dovana kafedroy gornoy elektrotehniki.

SITNIKOV, N. K.

SOV/99-59-8-7/10

30(1)

**AUTHORS:** Sjtnikov, N.K. and Shpil'berg, Yu.I., Engineers

**TITLE:** Grounds of Canal High Embankments in Operation

**PERIODICAL:** Gidrotekhnika i melioratsiya, 1959, Nr 8, pp 41-45 (USSR)

**ABSTRACT:** Upon decision of the Expert-Technical Department, the branch of the Yuzhgiprovodkhoz at Pyatigorsk conducted bottom research work at the large dams of the Kuban'-Yegorlyk irrigation system in 1957-58. The barrages were built in 1952-53 and the water was flowing there from 1955 till 1959, when it was interrupted because of repair works. Several diagrams (Figs.1-2) explain the nature of the bottom. The experiments which were made with samples taken from the bottom (July 1957-August 1958) are described. A table shows the results of the laboratory tests. A drainage system underneath the dams proved to be superfluous. By condensation of the ground layers of the barrages new physical-technical properties of the soil were constituted. There are 5 diagrams and 4 tables.

Card 1/1

**ASSOCIATION:** Pyatigorskiy filial Yuzhgiprovodkhoza (Pyatigorsk branch of Yuzhgiprovodkhoz)

COUNTRY : USSR J  
 CATEGORIES : Soil Science. Physical and Chemical Properties  
 ABS. JOUR. : <sup>of Soil</sup> Zhurnal; No. 4, 1959, No. 1000  
 AUTHOR : Yana, L.G.; Sitnikov, N.V.  
 TITLE : The rapid determination of total moisture by the  
 gravimetric method.  
 ORIG. PUB. : Izvestiya, 1958, No. 5, 78-80  
 ABSTRACT : It is pointed out that the reaction of the impen-  
 etration of a liquid, which does not need to be  
 dried, into soil particles. The value of liquid  
 impenetration is measured by the indicator of the  
 amount of water vapor. It was found that  
 the gravimetric method can be used to determine  
 the amount of water bound water in the soil  
 (the total and physical-chemical binding).  
 The experiment was conducted at a tempera-  
 ture of 100 degrees, the total amount of water

Cards: 1/1

KLIMENKO, K. (Minsk); SITNIKOV, O. (Minsk)

Tasks for improving the economic efficiency of production  
mechanisation. Vop. ekon. no.8:18-27 Ag '62. (MIRA 15:8)  
(Machinery industry) (Automation)



SITNIKOV, O. I.

"Some Problems in the Theory of Arc-Quenching Devices With Autoblast" (Nekotoriyye voprosy teorii dugogasyashchikh ustroysty s avtodut'yem), Elektrichestvo, No 7, 1950.

Ural Polytechnic Institute  
Dissertation for Candidate Degree

USSR/Electricity - High-Voltage Equipment Literature Apr 52

"Review of M. A. Babikov's Book, 'Modern Electrical High-Voltage Equipment,'" Docent M. M. Akodis, Cand Tech Sci, O. P. Sitnikov, Cand Tech Sci, Ural Polytech Inst

"Elektrichestvo" No 4, p 95

228766  
Favorable review of subject book, which, the article states, is basically a survey of new accomplishments in the theory and practice of high-voltage elec equipment building, with particular attention

228766

to Soviet developments. Sep chapters deal with circuit breakers, disconnecting switches, fuses and lightning arrestors, capacitors, instrument transformers, and combined equipments. Published by Gosenergoizdat, 1950, 271 pp, R 14.80.

228766

SITNIKOV, O. P.



3-58-7-31/36

AUTHORS: Sitnikov, O.P., Candidate of Technical Sciences, and Chaptsov, R.P.

TITLE: The D.C. Electronic Analyzer (Elektronnaya model' postoyannogo toka)

PERIODICAL: Vestnik vysshey shkoly, 1958, Nr 7, p 83 (USSR)

ABSTRACT: The d.c. electronic analyzer was built by students of the Kafedra apparatury avtomaticheskogo upravleniya radiotekhnicheskogo fakul'teta Ural'skogo politekhnicheskogo instituta (The Chair for Automatic Operation of Equipment of the Radio-technical Faculty of the Ural Polytechnical Institute). It was built in 1956-57 and all parts were constructed by students. There is 1 photo.

ASSOCIATION: Ural'skiy politekhnicheskii institut imeni S.M. Kirova (The Ural Polytechnical Institute imeni S.M. Kirov)

Card 1/1

8(6), 9(2)  
AUTHOR:

SOV/143-58-10-6/24  
Sitnikov, O.P., Candidate of Technical Sciences,  
Docent

TITLE:

The Extinction of an Alternating Current Arc

PERIODICAL:

Izvestiya vysshikh uchebnykh zavcdeniy, Energetika,  
1958, Nr 10, pp 40-48 (USSR)

ABSTRACT:

When developing and testing arc extinction devices of high-voltage switching gear, especially when using indirect methods, it is necessary to know the optimum conditions for arc extinction. The experience of investigating arc extinction devices of high-voltage switches showed that the two theories of extinction existing at the present time - the theory of dielectric strength recovery and the theory of power, considered separately - are inadequate for describing completely the arc extinction process. However, these two theories supplement each other, describing different phases, changing within the time of the alternating current are extinction. Actually, the power theory determines the conditions required for the transition of a

Card 1/5

The Extinction of the Alternating Current Arc SOV/143-58-10-6/24

theory of the dielectric strength recovery is justified after the termination of the self-contained discharge. The author then investigates the stability of an arc and the overvoltage when switching-off low currents. A number of papers deals with this subject. The author cites Kaufman, who took the arc impedance magnitude equal to the dynamic resistance, which is to be determined from the static volt-ampere characteristic. This calculation produces the necessary, but inadequate conditions, since only the problem of the static stability is solved thereby. G.S. Borchaninov assumes in his paper on the stability of the arc discharge that, in case of minor disturbances, the voltage at the arc will be a function of the current and the rate of current changes. This is equivalent to replacing the arc by a substitution circuit consisting of series-connected inductances and resistances. However, the character of the actual frequency characteristic of the arc in case of minor disturbances does not correspond to this equivalent circuit, which is confirmed by considering the dynamic characteristic obtained by

Card 3/5

The Extinction of an Alternating Current Arc SOV/143-58-10-6/24

applying to a dc arc sinusoidal oscillations of a low frequency. The author then investigates the arc stability mathematically. He recommends a parallel-connected, noninductive shunt for increasing the arc stability, damping the recovery voltage and reducing the current at which the arc is interrupted. The analysis method explained by the author provides new aspects for the process and the conditions for the transition of an impulse discharge into an arc discharge. The probability of such a transition depends essentially on the circuit parameters in the immediate vicinity of the impulse puncturing area. In circuits where the degree of arc stability is greater, the transition of the impulse discharge to a power arc is more probable, if the other conditions are equal. There are 5 Soviet references.

Card 4/5

The Extinction of an Alternating Current Arc SOV/143-58-10-6/24

- ASSOCIATION: Ural'skiy politekhnicheskii institut imeni S.M. Kirova  
(Ural Polytechnic Institute imeni S.M. Kirov) Kafedra  
apparatury avtomaticheskogo regulirovaniya (Chair of  
Automatic Control Equipment)

SUBMITTED: June 5, 1958

Card 5/5



9(6)

S/146/59/002/06/004/016  
D002/D006

AUTHORS: Sitnikov, O.P., Perminov, Yu.A., Gubin, V.A.

TITLE: A Device for Measuring the Errors of Automatic Control Systems <sup>q</sup>

PERIODICAL: Izvestiya vysshikh uchebnykh zavedeniy. Priborostroyeniye, 1959, Nr 6, pp 23-28 (USSR)

ABSTRACT: Detailed information is given on a device (Figure 1 and 2) for measuring the errors of automatic control systems. It is a decoupling lowfrequency amplifier with a relatively wide dynamic range and has a double triode whose grid receives the voltage from the integration chains serving as the error signal input. The signal causes a disbalance of the triode currents, which is recorded by an indicating instrument. The device measuring the mean square error value consists of a preamplifier, a detector, a squaring de-



Card 1/2

L 44286-65 EWT(1)/EEC(b)-2/EWA(h) Feb/Pl-4 GS

UR/0000/64/000/000/0442/6446

24  
B+1

ACCESSION NR: AT5011616

AUTHOR: Sitnikov, O. P., Vinogradova, N. B.

TITLE: New parametron-based logical units

SOURCE: Vsesoyuznoye soveshchaniye po magnitnym elementam avtomatiki, telemekhaniki izmeritel'noy i vychislitel'noy tekhniki. Lvov, 1962. Magnitnyye elementy avtomatiki, telemekhaniki, izmeritel'noy i vychislitel'noy tekhniki (Magnetic elements of automatic control, remote control, measurement and computer engineering); trudy soveshchaniya. Kiev, Naukova dumka, 1964, 442-446

TOPIC TAGS: parametron, logical circuit, simplified parametron, parametron unit operation, constant power parametron, computer design

ABSTRACT: The road to still faster and more reliable computers does not lie along the use of the vacuum-tube and transistorized circuits known so far. In many cases, it seems advisable to use logical elements based on parametric autogenerators with variable inductances or capacitances. These so-called parametrons are extremely reliable and their operating lifetime is infinite. They do not change their operating characteristics even under mechanical loads reaching hundreds of g, can operate within the -70 to +80C range

Card 1/3

L 44286-65

ACCESSION NR: a AT5011616

(see A. I. Vishnevetskiy, I. S. Sergiyenko, Parametron, Izd-vo MO SSSR, 1961), and are small in size. However, they require 1) a complex power supply, 2) a significant operating power, and 3) they are comparatively slow. The present paper offers circuit designs which eliminate or alleviate all three deficiencies. The circuit shown in Fig. 1 of the Enclosure is proven to be most economical. The power consumed by the loaded cell differs little from the power consumed during idling, and this, in turn, simplifies the tuning of the logical circuits and further improves their reliability. One parametron can control a large number of units, bringing about a significant decrease in size of the entire computer. Orig. art. has: 1 formula and 6 figures.

ASSOCIATION: None

SUBMITTED: 29Sep64

ENCL: 01

SUB CODE: DP

NO REF SOV: 001

OTHER: 001

Card 2/3

L 44288-65 EWT(1)/EFC(b)-2/EWA(h) Feb/Pl-4 GS

ACCESSION NR: AT5011617

UR/0000/64/000/000/0447/0451

AUTHOR: Sitnikov, O.P., Vinogradova, N. V., Smirnov, A. I.

TITLE: Parametron dynamics

SOURCE: <sup>75</sup> Vsesoyuznoye soveshchaniye po magnitnym elementam avtomatiki, telemekhaniki, izmeritel'noy i vychislitel'noy tekhniki. Lvov, 1962. Magnitnyye elementy avtomatiki, telemekhaniki, izmeritel'noy i vychislitel'noy tekhniki (Magnetic elements of automatic control, remote control, measurement and computer engineering); trudy soveshchaniya. Kiev, Naukova dumka, 1964, 447-451

TOPIC TAGS: parametron dynamics, parametron transient process, monotone parametron transient, nonlinear oscillation, computer design

ABSTRACT: A successful design of computers based on parametric elements requires the elucidation of parametron dynamics. The time intervals needed for the growth and decay of parametric oscillations fixes the limiting frequency of the cycling pulse and, consequently, the operating speed of the logical units. Transient processes caused by small changes in loop parameters can be described by linear equations. However, it is of much greater interest to study the growth of parametric oscillations up to the establishment of the stationary operating conditions which are described by essentially nonlinear equations.

Card 1/2

L 44288-65

ACCESSION NR: AT5011617

These effects were studied using the parametron equation

$$\frac{d(L_i)}{dt} + R_i + \frac{1}{C} \int I dt = U_y \sin \omega t, \quad (1)$$

derived in an earlier paper presented at a conference on magnetic elements held in 1961 in Minsk. After numerous transformations, this equation reduced to a first order system of equations which is discussed in the present paper. A formula is derived for the calculation of the duration of the transient parametron process and recommendations are given regarding the choice of circuit parameters necessary for the attainment of a monotone transition process. All theoretical conclusions were checked and confirmed experimentally. Orig. art. has: 9 formulas and 7 figures.

ASSOCIATION: none.

SUBMITTED: 29Sep64

NO REF SOV: 000

Card *Bej* 2/2

ENCL: 00

SUB CODE: DP

OTHER: 000

L 39493-56 ENI(d)/ENI(i)/ENP(i)/ENA(a) IJP(c) IG/IR/IG/GM/IG  
ACC NR: AT6002993 SOURCE CODE: UR/0000/65/000/000/0279/0287

AUTHOR: Sitnikov, O. P.; Vinogradova, N. B.; Zhuykov, Yu. N.

17  
B+

ORG: none

TITLE: Constructing computing devices with parametrons

SOURCE: Vsesoyuznoye soveshchaniye po magnitnym elementam avtomatiki i vychislitel'noy tekhniki, 9th, Yerevan, 1963. Magnitnyye tsifrovyye elementy (Magnetic digital elements); doklady soveshchaniya. Moscow, Izd-vo Nauka, 1965, 279-287

TOPIC TAGS: parametron, parametric amplifier, computer

ABSTRACT: The article establishes tolerances for deviations from nominal parameters of a parametron and recommends methods for quality control of ferrite cores. Experimental investigation of the effect of capacitance on the parametron output amplitude brought about these conclusions: (a) 10%-tolerance capacitors are undesirable; (b) mica or styroflex capacitors can be replaced with paper-insulated; (c) automodulation happens in the lower range of the parametron resonance

Card 1/2

ACC NR: AT6002993

characteristic. The effect of circuit inductance on the amplitude of parametron oscillations was also experimentally investigated and brought about these conclusions: (a) maximum pumping current should be used consistent with the desirable power consumption; (b) no error in the number of turns of windings on magnetic cores can be tolerated; (c) large spread in magnetic characteristics of cores is inadmissible. Parametrons with 400NN-1 ferrite show poor performance at low temperatures; the 1000NM ferrite ensures good operation of parametrons at  $-50+50^{\circ}\text{C}$ . It is recommended that the parametron operating point be selected in the upper range of its resonance characteristic where the negative detuning  $\delta$  is maximum; also, that capacitors with a tolerance of  $\pm 2\%$  be used. A very simple arrangement for testing magnetic cores is suggested. Orig. art. has: 10 figures and 1 formula.

SUB CODE: 09 / SUBM DATE: 23Apr65

Card 2/2 MLP

SITNIKOV, Oleg Stepanovich; POL'SKIY, S., red.; STEFANOVA, N., tekhn.  
red.

[Multipurpose attachments with interchangeable parts used in piece  
and small-lot manufacture of machinery] Universal'no-sbornye pripo-  
sobleniia v edinichnom i melkoseriinom mashinostroenii. Minsk, Gos.  
izd-vo BSSR Red. nauchno-tekhn lit-ry, 1961. 91 p. (MIRA 14:8)  
(Interchangeable mechanisms)



Sitnikov, Oleg Stepanovich

Mekhanizatsiya i avtomatizatsiya v mashinostroyenii; ekonomicheskaya effektivnost'.  
Minsk, Izd-vo Akademii Nauk BSSR, 1963.

289 p. tables.

*1. MACHINERY - CONSTRUCTION*

SITNIKOV, Oleg Stepanovich. Primal uchastiye MOISEYENKO, I.G., inzh.;  
GOL'BIN, Ya.A., kand. ekonom.nauk, red.; STRIZHONOK, M., red.izd-  
va; SIDERKO, N., tekhn. red.

[Economic efficiency of the mechanization and automation of auxiliary  
operations in the machinery industry] Ekonomicheskaya effektivnost'  
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