IMMEDIATE

Form
3-65 160c

(13)

3 1 JAN 1983

EXECUTIVE SECRETARIAT
Routing Slip

TO:			ACTION	INFO	DATE	INITIAL
	1	DCI				
	2	DDCI				
	3	EXDIR		X		
	4	D/ICS				
	5	DDI		X		
	6	DDA		X		
	7	DDO		X		
	8	DDS&T		X		
	9	Chm/NIC				
	10	GC				
	11	IG				
	12	Compt				
	13	D/EEO				
	14	D/Pers				
	15	D/OEA				
	16	C/PAD/OEA				
	17	SA/IA				
	18	AO/DCI				
	19	C/IPD/OIS				
	(20)	D/ODP	X			
	21					
	22					
	SUSPENSE	4 Feb				
		Date				

Remarks:
Please coordinate with all Directorates
and prepare a response for EXDIR's
signature.

STAT

*Cpy sent to
C/ms, DD/ODP*

3637 (10-81)

Executive Secretary
28 January 1983
Date

STAT

UNCLASSIFIED

The Director of Central Intelligence

Washington, D.C. 20505

ODP # 83-177

Intelligence Community Staff

DCI/ICS 83-4224
26 January 1983

MEMORANDUM FOR: Director, Defense Intelligence Agency
                  Director, National Security Agency
                  Executive Director, Central Intelligence Agency

VIA: Acting Director, Intelligence Community Staff

STAT

FROM:

                  Chief, Policy & Planning Staff

SUBJECT: Supercomputers

1. The ad hoc committee on Supercomputers convened by the Office of Science & Technology Policy (O/S&TP) met on 24 January 1983 to review the many issues on this subject. The opinions and proposals presented differed dramatically; consequently, no consensus could be developed. Doug Pewitt, Assistant Director, O/S&TP, tasked the members to respond to the following questions by Monday, 7 February 1983.

   A.   Do you currently own and operate or time share a supercomputer? How many or how much usage?

   B.   Do you have firm plans to acquire the next generation supercomputer? What specs? When? How many? Approximate dollar funds per supercomputer?

   C.   Is there a difference in your requirement between a "big number cruncher" and an even bigger and more complex AI-based machine?

   D.   Have you identified a US source or sources?

   E.   What impact would a successful Japanese fifth generation and supercomputer with the approximate performance characteristics have on your agency? (See attachment)

   F.   Is there a role for the federal government in stimulating, partially funding, or actually developing the fifth generation supercomputer. One body of opinion asserts the US Government should only indicate the range of performance characteristic desired, the best estimate on quantity required and probable time frame for delivery with a tolerable price range.

   G.   Do you have an opinion on the probable success or range of performance the Japanese are likely to achieve? Basis for opinion?

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2. My assessment is that there is not now a strong commitment for US Government involvement in any aspect of the next supercomputer, nor to any concentrated reaction to the potential Japanese computer project.

3. Please provide me your comments (which may be classified if appropriate) by noon, Monday, 7 February. I will provide them to Dr. Keyworth's office and will obtain and circulate all members' comments for your individual review and comment prior to developing an Intelligence Community position.
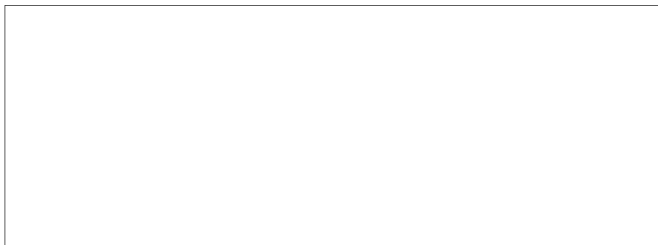
STAT

Attachment:
   Japanese Computer Specifications
     (20 Charts)

SUBJECT: Supercomputers

Distribution: (DCI/ICS 83-4224)
    1 - each addressee w/att
    1 - ER w/att
    1 - A-D/ICS w/o att
    1 - ICS Registry w/att
STAT   1 - ICS/Info Handling Committee Staff [   ] w/att
    1 - ICS/PPS Subject (Supercomputers) w/att
    1 - ICS/PPS Chrono w/o att

STAT   DCI/ICS/PPS [   ] (26 Jan 83)

JAPANESE GOALS

JAPANESE GOVERNMENT (MITI) AND COMPUTER
INDUSTRY WANT TO BE LEADERS IN SUPER
COMPUTING

THREE NATIONAL PROJECTS
- COMPONENTS
- HIGH-SPEED COMPUTER
- FIFTH GENERATION COMPUTER

NUMEROUS INDIVIDUAL COMPANY PROJECTS

COMPUTING   **Los Alamos**

JAPANESE NATIONAL
SUPER-SPEED COMPUTER PROJECT

DURATION: 1982-89

FUNDING: $200M

OBJECTIVES: 10 GIGAFLOPS
1 GIGABYTE OF MEMORY WITH
1.5 GIGABYTE BANDWIDTH
100 MEGAFLOPS IN DISTRIBUTED
PROCESSING

PARTICIPANTS: ETL
FUJITSU
HITACHI
NEC
MITSUBISHI
OKI

COMPUTING   TOSHIBA   **Los Alamos**

FIFTH GENERATION COMPUTER

STARTS APRIL 1982

OBJECTIVE: A LARGE, INTELLIGENT COMPUTER SYSTEM
FOR
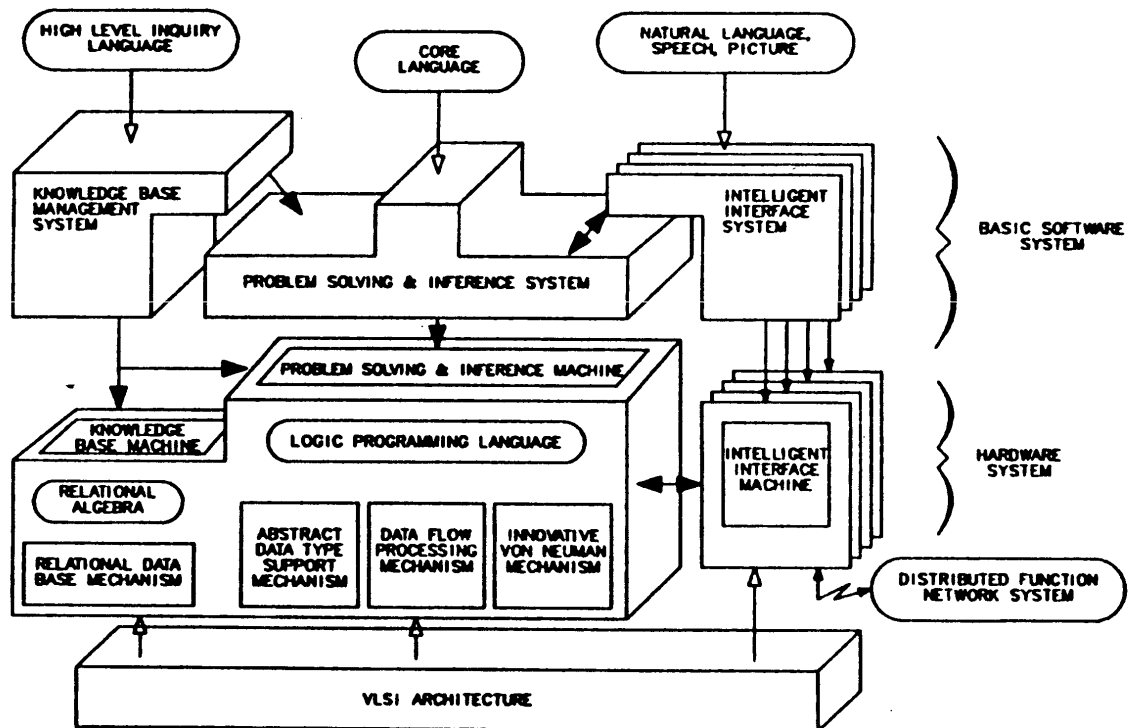- LANGUAGE PROCESSING
- SPEECH AND IMAGE PROCESSING
- EXPERT SYSTEMS

THREE PHASES
1ST - 3 YEARS - FUNCTIONAL MODULES
2ND - 4 YEARS - BUILD A PROTOTYPE
3RD - 3 YEARS - COMPLETE THE SYSTEM
AND SOFTWARE

$45M OF GOVERNMENT FUNDS FOR FIRST PHASE

COMPUTING

Los Alamos

BASIC CONFIGURATION IMAGE OF THE FIFTH GENERATION COMPUTER SYSTEM (JAPANESE)

COMPUTING

Los Alamos

5TH GENERATION COMPUTER: SPECIFICATIONS

- HIGHER PERFORMANCE LEVEL AT A LOWER COST
- "TRIPARTITE BRAIN"
    1) INTELLIGENT INTERFACE SYSTEM
        - ACCESS THROUGH NATURAL LANGUAGE AND PICTURES
    2) PROBLEM-SOLVING AND INFERENCE SYSTEM
        - HANDLE MANY MORE GENERAL PROBLEM-SOLVING TASKS THAN TODAY'S MACHINES
        - BE ABLE TO LEARN, ASSOCIATE, AND INFER
    3) KNOWLEDGE-BASED MANAGEMENT SYSTEM
        - BE ABLE TO UNDERSTAND AND USE STORED INFORMATION
        - "KNOWLEDGE BASES" RATHER THAN "DATABASES"
- EACH OF THE THREE SYSTEMS HAS OWN SPECIALIZED MACHINE WITH VLSI ARCHITECTURE
- COMPUTER SIZES TO RANGE FROM MICRO'S TO MAINFRAMES

SOURCE: TOM MANUEL, BYTE, 5/82

5TH GENERATION COMPUTER: EXAMPLE: PROJECTS AND SPECIFICATIONS

- PERSONAL WORK STATION
  - PERFORM 2 MIPS
  - HAVE .5 TO 5 MEGABYTES OF MEMORY
  - HAVE 100 MEGABYTES OF DISK STORAGE, WITH AN AVERAGE ACCESS OF
    1 MILLISECOND
- "SUPER HIGH-SPEED PROCESSOR"
  - PERFORM 1 TO 100 BILLION FLOATING POINT OPERATIONS PER SECOND (FLOPS)
  - HAVE 8 TO 160 MEGABYTES OF MEMORY
- PROBLEM — SOLVING AND INFERENCE FUNCTION
  - PERFORM 100 MILLION TO 1 BILLION LOGICAL-INFERENCE OPERATIONS PER
    SECOND
        (1 LOGICAL INFERENCE = 100 TO 1000 INSTRUCTIONS)
- NATURAL LANGUAGE PROCESSING SYSTEM
- KNOWLEDGE-BASED MANAGEMENT FUNCTION
  - RETRIEVE 1 UNIT OF KNOWLEDGE IN SEVERAL SECONDS FROM A BASE OF 100
    TO 1000 GIGABYTES

SOURCE: MANUEL, BYTE, 5/82

5TH GENERATION COMPUTER: EXAMPLE: PROJECTS AND SPECIFICATIONS

- VERY-LARGE-SCALE INTEGRATION TECHNOLOGY

  - AT FIRST, HAVE 1 MILLION TRANSISTORS PER CHIP

  - EVENTUALLY HAVE 10 MILLION TRANSISTORS PER CHIP

SOURCE: MANUEL, BYTE, 5/82

Machine translation system
- Translations among multiple languages
- Vocabulary size: 100,000 words
- Machine to guarantee 90% accuracy, with remaining 10% to be processed through intervention by man.
- System to be an integrated system where computers participate in individual stages ranging from text editing to printing and of translations.
- Total costs involved to remain at 30% or lower than for human translation.

Consultation systems
- Specimen applications
  - Medical diagnosis
  - Natural language comprehension
  - Mechanical equipment computer-aided design
  - Computer user consultation
  - Computer systems diagnosis
- Number of objects: 5,000 or more
- Inference rules: 10,000 or more
- Semi-automated knowledge acquisition
- Interfaces with system: Natural languages and speech
- Vocabulary size: 5,000 words or more

Chart Courtesy MITI

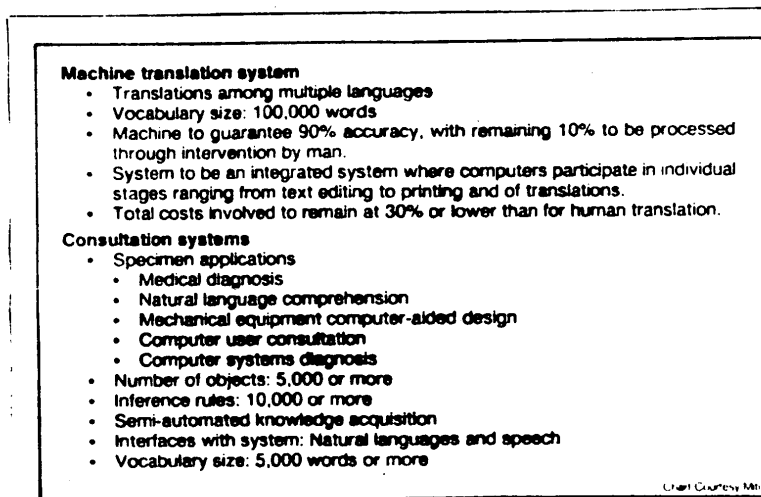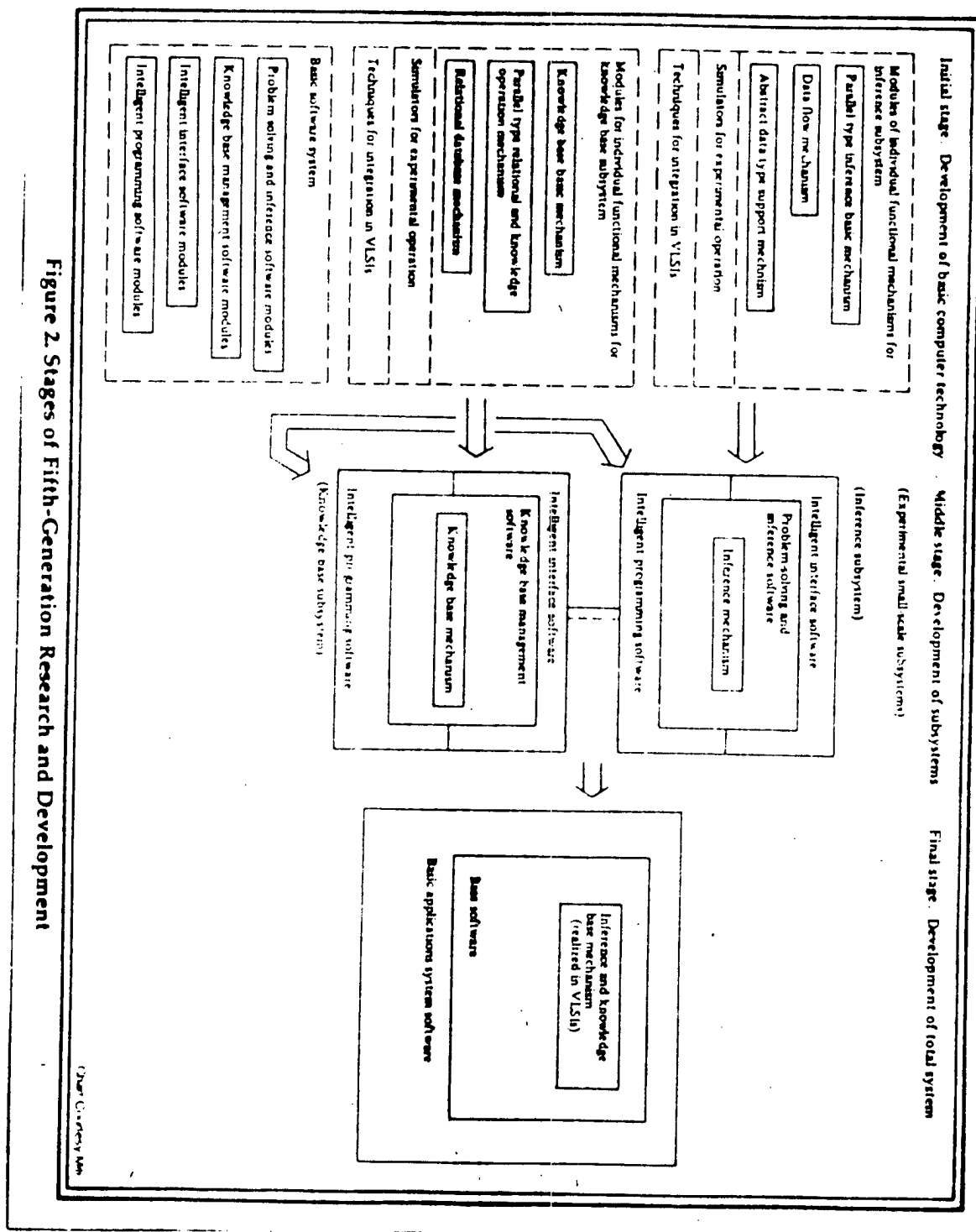**Figure 1. Subjects and 10-Year Targets for Basic Applications Systems**

SOURCE: REX MALIK, COMPUTERWORLD/EXTRA
11/17/82, P. 25

Figure 2. Stages of Fifth-Generation Research and Development

Initial stage : Development of basic computer technology

Modules of individual functional mechanisms for inference subsystem

Parallel type inference basic mechanism

Data flow mechanism

Abstract data type support mechanism

Techniques for integration in VLSIs

Simulation for experimental operation

Modules for individual functional mechanism for knowledge base subsystem

Knowledge base basic mechanism

Parallel type relational and knowledge operation mechanism

Relational database mechanism

Simulation for experimental operation

Techniques for integration in VLSIs

Basic software system

Problem solving and inference software modules

Knowledge base management software modules

Intelligent interface software modules

Intelligent programming software modules

Middle stage : Development of subsystems

(Experimental small scale subsystem)

(Inference subsystem)

Intelligent programming software

Problem solving and inference software

Inference mechanism

Intelligent interface software

Knowledge base management software

Knowledge base mechanism

(Knowledge base subsystem)

Final stage : Development of total system

Inference and knowledge base mechanism (realized in VLSIs)

Basic software

Basic applications system software

SOURCE: REX MALIK, COMPUTERWORLD/EXTRA 11/17/82, P. 25

5TH GENERATION COMPUTER: NEW TECHNOLOGIES

- NEW TECHNIQUES TO BE USED

- NEW ARCHITECTURES LIKE DATA-FLOW MACHINES

- ARTIFICIAL-INTELLIGENCE CONCEPTS

- LANGUAGES SUCH AS LISP AND PROLOG WITH MACHINES OPTIMIZED FOR THEM

- TECHNOLOGIES CURRENTLY EXCLUDED FROM PROGRAM

- EXAMPLES

  - GALLIUM ARSENIDE

  - JOSEPHSON JUNCTIONS

- RESEARCHERS FELT THESE TECHNOLOGIES WOULD NOT BE SUFFICIENTLY DEVELOPED FOR GENERAL USE BY 1990

  - THEY WILL BE INCLUDED AT SOME INTERMEDIATE STAGE IF OUTSIDE RESEARCH GAINS OCCUR

SOURCE: MANUEL, BYTE, 5/82

5TH GENERATION COMPUTER: DESIGN AUTOMATION SYSTEM

- CONSISTS OF THREE PARTS

  1) SOFTWARE FOR AUTOMATED DESIGN OF VLSI

     - PLAN TO INITIALLY IMPLEMENT HSL (HIERARCHICAL SPECIFICATION LANGUAGE)

       - HSL CONTAINS SEVERAL MODULES INTEGRATED INTO A TOTAL DESIGN SYSTEM

       - CURRENTLY BEING USED AT THE MUSASHINO ELECTRICAL COMMUNICATION LABORATORY OF NIPPON TELEGRAPH AND TELEPHONE PUBLIC CORPORATION

  2) SYSTEM 5G - THE COMPUTER SYSTEM TO RUN IT

     - PLAN TO USE CONVENTIONAL 40 MIPS GENERAL-PURPOSE COMPUTER UNTIL FIRST 5TH GENERATION COMPUTERS ARE AVAILABLE
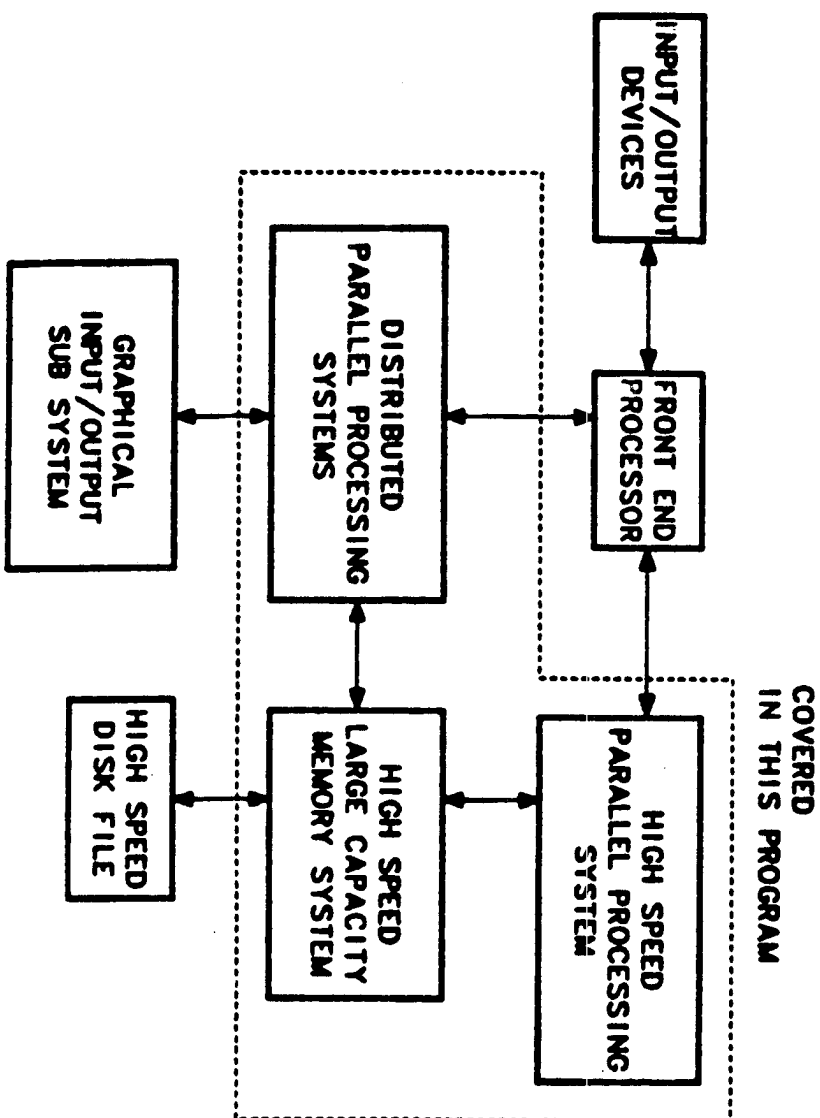
SOURCE: MANUEL, BYTE, 5/82

5TH GENERATION COMPUTER: DESIGN AUTOMATION SYSTEM (PAGE 2)

3) 5G PERSONAL COMPUTER – LOGIC-PROGRAMMING WORK STATION FOR DESIGNERS

  — REQUIRES HIGH-SPEED PROCESSING OF VOICE, GRAPHIC, AND DIGITIZED IMAGE INPUT AS WELL AS PERFORMANCE AS A PERSONAL-INTERFACE MACHINE

  — NO EXISTING PERSONAL COMPUTER MEETS THESE SPECIFICATIONS

SOURCE: MANUEL, BYTE, 5/82

COMPUTING

JAPANESE
ULTRA-HIGH-SPEED COMPUTING FACILITY

```
                    ┌──────────────┐
                    │ INPUT/OUTPUT │
                    │   DEVICES    │
                    └──────┬───────┘
                           │
  ┌──────────┐   ┌─────────────┐   ┌─────────────┐
  │GRAPHICAL │   │ DISTRIBUTED │   │  FRONT END  │
  │  INPUT/  │◄─►│  PARALLEL   │◄─►│  PROCESSOR  │
  │ OUTPUT   │   │ PROCESSING  │   │             │
  │SUB SYSTEM│   │  SYSTEMS    │   └──────┬──────┘
  └──────────┘   └──────┬──────┘          │
                        │                 │
  ┌──────────┐  ┌───────────────┐  ┌──────────────┐
  │HIGH SPEED│  │  HIGH SPEED   │  │  HIGH SPEED  │
  │DISK FILE │◄►│ LARGE CAPACITY│◄►│   PARALLEL   │
  │          │  │ MEMORY SYSTEM │  │  PROCESSING  │
  └──────────┘  └───────────────┘  │    SYSTEM    │
                                    └──────────────┘
```

COVERED
IN THIS PROGRAM

Los Alamos

31

ADVANCES ARE REQUIRED IN

COMPONENTS

ARCHITECTURE

ALGORITHMS AND LANGUAGES

COMPUTING

Los Alamos

COMPONENT OBJECTIVES

LOGIC: 3k GATES, 10 ps DELAY (JJ,HEMT)

3k GATES, 30 ps DELAY (GaAs)

MEMORY: 16k bits, 10 ns ACCESS

COMPUTING

Los Alamos

SUMMARY

JAPAN HAS LAUNCHED A NATIONAL PROGRAM TO BECOME A WORLD LEADER IN SUPERCOMPUTERS.

ALL SIX MAJOR JAPANESE VENDORS ARE PARTICIPATING.

THE PROJECT IS LIKELY TO PRODUCE A COMPUTER AND EVEN PARTIAL SUCCESS COULD HAVE FAR REACHING CONSEQUENCES.

COMPUTING

Los Alamos

5TH GENERATION COMPUTER: SOME JAPANESE EXPECTATIONS

- BENEFITS TO BE GAINED

    - RAISING PRODUCTIVITY IN LOW-PRODUCTIVITY FIELDS
    - PRESERVATION OF INTERNATIONAL COMPETITIVE CAPABILITY BY DEVELOPMENT
      OF NEW TECHNOLOGY
    - CONSERVATION OF ENERGY AND RESOURCES
    - PROMOTE UTILIZATION OF CAPACITY OF AGING CITIZENS
    - INFORMATIONALIZATION OF SOCIETY

SOURCES: SID FERNBACH, BRIEF ON THE
JAPANESE COMPUTER INDUSTRY, MAY, 1981

ZEN YAMADA, MEMORANDUM ON RECENT
PUBLISHED INFORMATION, MAY 13, 1981

5TH GENERATION COMPUTER: SOME JAPANESE EXPECTATIONS

FEATURES OF 5TH GENERATION COMPUTER

- CONSIDERABLE DIVERSITY
- EMPHASIS ON SPECIALIZATION
- NON-VON NEUMANN ARCHITECTURE
- COMPOSITE MICRO-ARCHITECTURE
- INPUT/OUTPUT OF DAILY LANGUAGES, CHARACTERS, GRAPHS WITH NO MODIFICATION
- SELF-RECOVERING FUNCTION (AUTOMATIC RECOVERY)
- SELF-PROGRAMMABLE WITH SIMPLE INSTRUCTIONS (NO REQUIREMENT FOR HUGE PROGRAMS)
- FUTURE PROBLEM SOLVING BASED ON RECORDED DATA

SOURCES: SID FERNBACH, BRIEF ON THE JAPANESE COMPUTER INDUSTRY, MAY, 1981

ZEN YAMADA, MEMORANDUM ON RECENT PUBLISHED INFORMATION, MAY 13, 1981

5TH GENERATION COMPUTER: SOME JAPANESE EXPECTATIONS

- MAJOR R&D THEMES
  - DEVICE TECHNOLOGY
  - ARCHITECTURE AND HIGH PERFORMANCE PROCESSES
  - DISTRIBUTED FUNCTIONAL SYSTEMS
  - SOFTWARE ENGINEERING
  - INTELLIGENT ROBOTS
  - HIGH RELIABILITY, SECRECY PROTECTION FUNCTION

SOURCES: SID FERNBACH, BRIEF ON THE JAPANESE COMPUTER INDUSTRY, MAY, 1981

ZEN YAMADA, MEMORANDUM ON RECENT PUBLISHED INFORMATION, MAY 13, 1981

Japanese Computer Research: Software Development

- "The Electronic Computer Basic Technology Development Association"

  - Cooperative Association to Develop Software

  - Members

    - Hitachi

    - Toshiba

    - Fujitsu

    - NEC

    - Mitsubishi

    - Oki

    - Matsushita

    - Sharp

    - NEC - Toshiba Information Systems

  - Computer Development Laboratory

- Will Spend $56 M (1981-1986)

  - MITI will provide half the funds

Source: Sid Fernbach, Brief Report on the Japanese Computer Industry, May, 1981

ROUTING AND TRANSMITTAL SLIP

Date 3 Feb. 83

TO: (Name, office symbol, room number, building, Agency/Post)

		Initials	Date
1.	C/TID		3/
2.	DD/E	2/3	
3.	D/OGI	4 FEB 1983	
4.	3. D/ODP 2D0105 Hqs.		
5.	2.	WA 4 Feb 83	4 Feb 83

Action		File		Note and Return	
Approval		For Clearance		Per Conversation	
As Requested		For Correction		Prepare Reply	
Circulate		For Your Information		See Me	
Comment		Investigate		Signature	
Coordination		Justify			

REMARKS

CP wants to Rush

(NOTE: , MS/ODP sent cys to

1 - DD/Pr
1 - DD/Ap
1 - SPS

by 2:30PM Fri. 2/4/83

STAT

STAT

NOT use this form as a RECORD of approvals, concurrences, disposals, clearances, and similar actions

M: (Name, org. symbol, Agency/Post)

OGI/TID

Room No.—Bldg.
3G22 Hqs.

Ph

102

OPTIONAL FORM 41 (Rev. 7-76)
Prescribed by GSA
FPMR (41 CFR) 101-11.206

GPO:1978-0-261-647-3354

4 FEB 1983

MEMORANDUM FOR: Director, Office of Data Processing

FROM:

Director of Global Issues

SUBJECT: Japanese Supercomputer Developments

REFERENCE: DCI/ICS 83-4224, dated 26 January 1983

     1. At the request of your Policy and Plans Group, we are providing our assessment of Japanese capabilities and plans for supercomputer developments. Specifically, the attachment responds to Question G of the reference, concerning Japanese prospects for success in developing
supercomputer systems.

     2. In addition to the attachment, we are preparing a detailed Intelligence Assessment on Japanese supercomputer systems that should be available in draft within the next few months. In addition to providing more detailed information on the Japanese supercomputers, the study will investigate Japanese marketing plans and discuss the impact of Japanese
competition on US economic and strategic interests.

     3. If you have any questions or comments please call Chief, Technology Analysis Branch,

Attachment:
  As stated

This Memorandum is classified
Upon Removal From Attachment

SECRET

Page Denied

Next 26 Page(s) In Document Denied