JPRS L/10656

14 JULY 1982

Translation

ANALOG AND DIGITAL INTEGRATED CIRCUITS

By

SERGEY VIKTOROVICH YAKUBOVSKIY ET AL.

FBIS FOREIGN BROADCAST INFORMATION SERVICE

NOTE

JPRS publications contain information primarily from foreign newspapers, periodicals and books, but also from news agency transmissions and broadcasts. Materials from foreign-language sources are translated; those from English-language sources are transcribed or reprinted, with the original phrasing and other characteristics retained.

Headlines, editorial reports, and material enclosed in brackets [] are supplied by JPRS. Processing indicators such as [Text] or [Excerpt] in the first line of each item, or following the last line of a brief, indicate how the original information was processed. Where no processing indicator is given, the information was summarized or extracted.

Unfamiliar names rendered phonetically or transliterated are enclosed in parentheses. Words or names preceded by a question mark and enclosed in parentheses were not clear in the original but have been supplied as appropriate in context. Other unattributed parenthetical notes within the body of an item originate with the source. Times within items are as given by source.

The contents of this publication in no way represent the policies, views or attitudes of the U.S. Government.

APPROVED FOR RELEASE: 2007/02/09: CIA-RDP82-00850R000500080030-5

JPRS L/10656

14 July 1982

ANALOG AND DIGITAL INTEGRATED CIRCUITS

Moscow ANALOGOVYYE I TSIFROVYYE INTEGRAL'NYYE SKHEMY in Russian 1979 (signed to press 5 Apr 79) pp 1-335

[Book by Sergey Viktorovich Yakubovskiy, Nikolay Arsen'yevich Barkanov, Boris Petrovich Kudryashov, Lev Ionovich Nissel'son, Mikhail Kikiforovich Topeshkin and Lyubov' Petrovna Chebotareva, Izdatel'stvo "Sovetskoye Radio", 68,000 copies, 336 pages, UDC 621,396]

CONTENTS

Foreword..... 1

Chapter 1: Terminology in Microelectronics and Classification of Integrated Circuits..... 5

1.1. Introduction..... 5

1.2.1. Integrated Microcircuits, Elements, Components..... 6

1.2.2. Design Elements..... 6

1.2.3. Simple and Complex IC..... 7

1.2.4. Microassemblies and Microunits..... 8

1.3. IC Classification..... 9

1.4. System of Conditional IC Designations..... 10

Chapter 2: Methods of Fabricating Integrated Circuits..... 18

2.1. Film and Hybrid Technology..... 18

2.1.1. Materials for Hybrid IC's..... 19

2.1.2. The Fabrication of the Elements of Hybrid IC's..... 21

2.1.3. Making Electrical Connections in Hybrid IC's..... 24

2.2. Semiconductor Technology..... 24

2.2.1. Materials for the Components of Semiconductor IC's and Their Manufacture..... 26

2.2.2. The Fabrication of Integrated Circuit Structures..... 29

2.2.3. Separating a Wafer Into Chips and Mounting the IC's..... 34

2.2.4. The Hermetic Sealing of IC Chips..... 36

2.2.5. The Manufacture of IC Packages..... 37

2.3. Specific Features of the Technology of IC's With a High Level of Integration..... 40

Chapter 3: Digital Integrated Circuits..... 46

3.1. Designation and Application..... 46

3.2. Logic Functions Which Can Be Realized Using Digital IC's..... 46

3.3. The Classification of Digital Integrated Circuits and Their Main Electrical Parameters..... 51

3.4. Transistor-Transistor Logic Circuits..... 55

3.4.1. The Major Electrical Parameters of TTL Integrated Circuits..... 70

3.4.2. The Functional Complement of the TTL Series..... 70

3.4.3. Some Specific Features of TTL Integrated Circuit Applications..... 72

3.5. Emitter Coupled Transistor Logic Circuits..... 85

3.5.1. Functional Composition of the ESTL Series..... 88

3.5.2. Basic Electrical Parameters and Typical Characteristics of IC Type ESTL..... 102

3.5.3. Certain Special Features in the Use of IC Type ESTL..... 106

3.6. Digital Integrated Circuits Based on MOS Structures..... 115

3.6.1. The Operational Principle of Integrated Circuits Using p-Channel MOS Transistors..... 115

3.6.2. Static Circuits Using p-Channel MOS Transistors..... 120

3.6.3. Quasistatic and Dynamic Circuits..... 122

3.6.4. The Operational Principle of Complementary MOS Transistor Integrated Circuits..... 125

3.6.5. The Major Series of Integrated Circuits Using MOS Structures..... 128

3.7. Integrated Circuits for Memories..... 136

3.7.1. Memory Elements Using Bipolar Structures..... 137

3.7.2. Memory Elements Using MOS Structures..... 140

3.7.3. Memory Elements Using CMOS Transistors..... 141

3.7.4. Storage Elements Employing MNOS Structures..... 142

3.7.5. Storage Elements Based on "Silicon on Sapphire" Structures..... 145

3.7.6. Storage Elements Based on New Materials..... 145

3.7.7. Major Series of Memory Unit Integrated Circuits and Their Functional Structure..... 147

3.8. Prospects for the Development of Digital Integrated Circuits..... 150

3.8.1. Integrated Injection Logic..... 151

3.8.2. MOS Circuits With n-Channels..... 152

3.9. Microcalculators..... 154

3.10. Microprocessors..... 158

3.10.1. Characteristics of a Microprocessor..... 160

3.10.2. Medium Operating Speed Microprocessor Configuration..... 163

3.10.3. Improved Operating Speed Microprocessor Configuration.... 169

Chapter 4: Analog Integrated Circuits..... 218

4.1. Function and Application..... 218

4.2. Operational Amplifiers..... 218

4.2.1. Operational Amplifiers With a Two Stage Structural Configuration..... 225

4.2.2. Amplifiers With Field Effect Transistors at the Input..... 233

4.2.3 Amplifiers With Super-Beta Transistors..... 234

4.2.4. The 153UD5 High Precision Operational Amplifier..... 239

4.2.5. High Speed Operational Amplifiers..... 240

4.2.6. Micropower Operational Amplifiers..... 242

4.3. Integrated Circuit Comparators..... 246

4.4. Integrated Circuit Analog Multipliers..... 250

4.5. Analog Integrated Circuits for Radio Receiving Equipment..... 263

4.5.1. The Differential Amplifier..... 263

4.5.2. Low Frequency Amplifiers (UNCh)..... 265

4.5.3. Specialized Integrated Circuits..... 270

4.5.4. IC's for the Construction of Selective Circuits..... 274

4.6. Integrated Circuits for Analog to Digital and Digital to Analog Data Conversion..... 276

4.7. Analog Switches..... 291

4.8. Integrated Circuit Voltage Regulators..... 296

Chapter 5: Providing Reliability of IC [Integrated Circuits] in the Production and Assembly Apparatus..... 312

5.1. Design-Technological Principles of High Reliability..... 312

5.2. Operational Quality Contorl..... 314

5.3. Rejection Tests..... 314

5.4. Effect of External Factors on Apparatus Production..... 323

5.5. Forming and Trimming Leadouts..... 325

5.6. Tinning and Soldering..... 331

5.7. IC Assembly on Printed Circuit Boards..... 341

5.8. IC Protection Against Electrical Effects..... 345

5.9. Dismantling..... 352

Table of Contents..... 354

[Text] The products list of the basic series of analog and digital integrated circuits produced by the electronics industry is surveyed. Methods of their fabrication, parameters and characteristics, as well as the operational principles of the basic components are treated. The developmental trends in logic circuits are indicated. Basic data is given for microprocessors as well as the specific features of their applications. Factors which influence IC reliability are covered, the specific features of IC application in the design of radioelectronic equipment are described and recommendations are made concerning the prevention of IC failures with exposure to various external loads as well as during production process operations.

The book will prove to be useful to engineers working in the field of radioelectronic equipment design and those interested in questions of selecting the IC component base and specific features of IC applications as well as for students in the appropriate specialties.

The book contains 73 tables, 186 illustrations and 64 bibliographic citations.

Foreword

In the main trends of national economic development for 1976 - 1980, set by the 25th CPSU Congress, among the major ways of improving production efficiency it calls for a "decisive improvement in the quality of all kinds of products which are produced, an expansion of the assortment, an increase in the production of new kinds of products which meet modern requirements" [1]. It is impossible to solve this problem without the further development of electronics, which provides not only for the creation of complex automated controls systems for production processes in the most diverse sectors of the national economy, but also for the development

of fundamentally new products for mass consumption. The expansion of the area of applications of electronics devices is one of the specific features of scientific and engineering progress at the present stage.

The development of electronics, starting in the 1960's, was related to the appearance and rapid improvement of integrated circuits (IC's). Integrated circuits make it possible to design modern complex electronic devices with sizes and weights acceptable in practice, as well as guarantee their high reliability. Integrated circuits have found the most widescale applications in the design of digital equipment.

The properties and characteristics of IC's are determining to an increasingly greater extent the technical characteristics of computers. Modern digital integrated circuits are complex products which realize the functions of entire blocks and assemblies of computers. It is specifically this which is responsible for the appearance of a completely new field in electronics: microprocessing design. While digital IC's were the basis for the design of third generation computers, the production mastery of microprocessors, which are IC's with increased functional complexity and universality, makes it possible to process digital signals in a new way and thus anticipate the widescale introduction of digital data processing techniques in the most diverse fields of engineering (even in those where the application of electronics had previously not had a substantial impact). Fourth generation computers are being designed around microprocessor sets (4 to 5 individual packages).

Three stages may be conditionally singled out in the development of digital IC technology and circuit design. The first was the development of the basic series of integrated circuits which execute simple logic functions (NAND, NOR, AND-OR-NOT, etc., where, as a rule, the complement of each series contained flip-flops). At this stage, IC's were designed with from 10 to 50 components.

The second stage was the development of more complex functionally complete units (counters, registers, decoders, half-adders, etc.) having from 50 to 500 components. The functional complement of the previously developed series is being constantly expanded by virtue of such new circuits.

The third stage is the development complex functional devices having an integration level of from 500 to 10,000 components on a single chip. This stage arrived at the start of the 10th Five-Year Plan. Pocket engineering calculators with broad capabilities for performing calculations based on preprogramming for the problem to be solved were designed using third stage circuits.

In the process of the development of digital integrated circuit electronics, unipolar IC's with MOS structures were developed and found wide application along with bipolar circuits: p and n-type, complementary (CMOS), MOS with nitride insulation (MNOS) and some others. It is specifically the digital circuits with MOS structures which made it possible to bring the number of elements on a chip up to 10,000 and to design such complex circuits as main memories (OZU) having a large data volume, as well as random access memory circuits and memories with long term storage of data when the power supply is turned off.

Experience with the applications of the entire diversity of technological pproaches to IC fabrication, developed during the last 10 years, has confirmed the convenience of the application and good technical characteristics of bipolar TTL and ECL circuits, as well as circuits with MOS structures. Both the Unified System of Electronic Computers (YeS EVM), created through the joint efforts of CEMA member nations, and the broad family of small computers and calculators (from the simplest school calculators with four arithmetic operations, up to universal programmable calculators which can be used in scientific research) have been built on the basis of these circuits.

The past decade also gave equipment designers a new analog component base: a large assortment of universal operational amplifiers, comparators, analog-digital and digital-analog converters, voltage regulators, switchers, as well as a set of low, intermediate and high frequency amplifiers. The application of analog IC's has made it possible to simplify the adjustment of instruments, increase their reliability and precision, and in many cases also eliminate the nececcisty of servicing.

In recent years, the design of equipment using unpackaged IC's, with overall hermetic sealing in modules, has become an independent direction. Such an approach makes it possible to obtain a high compoment density and significantly reduce the size and weight of special equipment.

The domestic electronics industry produces a large products list of modern digital and analog integrated circuits, which has become the main component base for modern radio electronics equipment (REA) for industrial purposes.

The price which must be paid for high radio electronic equipment reliability is the correction application of integrated circuits and the observance of their operational modes; violation of these conditions because of inadequate knowledge of the technical properties, electrical paramaters and operating modes is also the most frequent cause of failures.

The goal of this book is to provide basic technical characteristics of digital and analog integrated circuits, set forth the methods of manufacturing them and the functional complement of a series, as well as devote attention to the specific features of IC applications in the development of radio electronic equipment and make recommendations for the assurance of integrated circuit reliability in their production and installation in equipment.

The material presented in the book is based on the results of generalizing the experience with the development and applications of integrated circuits.

The collective of authors expresses their deep gratitude to doctor of the technical sciences, professor B.F. Vysotskiy, candidate of mathematical physics, B.N. Fayzulayev, candidates of the technical sciences Ye.I. Gal'perin, G.A. Podol'skiy, V.I. Kotikov, as well as V.L. Shilo, who took an active part in discussing the contents and structure of the book and made a number of valuable comments concerning the material content and its layout. The authors are also grateful to V.N. Bulanova and V.A. Ushibyshev for rendering assistance in the preparation and formating of the manuscript.

The authors ask that all remarks and proposals on improving the book be directed to the following address: Moscow, 101000, Main Post Office, Box 693, Izdatel'stvo "Sovetskoye Radio".

The authors

[Text] Chapter 1

Terminology in microelectronics and classification of integrated circuits

1.1. Introduction

Microelectronics is a developing field of electronics Basically, it is the creation of an integrated element base used to develop apparatus. The term integrated electronics combines the "element," as well as the "apparatus" microelectronics. Many concepts in the field have still not established themselves firmly; therefore, questions of terminology in Russian, as well as in many foreign languages are fairly complex. In 1969, the International Electrotechnical Commission (MEK) issued the second supplement to publication 147-0 (1966) [2] in which, for the first time, terminology was presented in the field of integrated circuits. The supplement included the definition of several of the most common terms such as microelectronics, microcircuit, integrated microcircuit etc.

In our country, the first attempts to regularize terms and definitions were attempted in 1967 when a norm "Integrated microcircuits. Terminology" was issued. The lack of status of this document made it impossible to recommend it as compulsory. In connection with the considerable expansion of the use of integrated circuits, the necessity arose of a government standard on terminological questions in the field of microelectronics which was developed on the basis of the above-mentioned norm and the MEK publication and, in 1971, it was approved by the USSR Gosstandart [3]. GOST 17021-71 included 16 terms and along with general terms such as integrated microcircuit, semiconductorintergrated microcircuit, there were also given single-valued definitions for parts of integrated circuits (for example, substrate, housing).

Terms whose definitions were given in the above-mentioned GOST were widely used in technical documents. However, the development of microelectronic means, the increase in the wiring density and in the number of elements on one chip had already led, in 1973, to the necessity of reworking this GOST for the purpose of correcting it and introducing new terms. In 1975, this work was completed by the approval of GOST 17021-75 [4].

Below are given the terms as per GOST 17021-75, their definitions and the synonyms of these terms which are widely used in production and in technical literature.

1.2.1. Integrated Microcircuits, Elements, Components

An integrated circuit (IC) is a microelectronic article that fulfills a certain function of converting and processing signals and has a high packing density of the electrically connected elements (or elements and components) and chips. This article is considered a single whole from the standpoint of the requirements of tests, acceptance, delivery and operation.

In abbreviated form, integrated microcircuits are called IMS. The synonym of an integrated microcircuit is the term integrated circuit or, still simpler, microcircuit. Of all the indicated terms, integrated circuit (IC) is the most frequently used. It has two subordinate terms, whose description is given by the above-mentioned GOST. These are concepts of an element of an integrated circuit (or simply element) and component of an integrated circuit (or simply component).

An element of an integrated circuit means the part of the IC that realizes the function of some simple electroradio element (for example, transistor, diode, resistor, capacitor). This part is inseparable from the IC chip (or its substrate). The element cannot be separated from the IC as an independent article; therefore, it cannot be tested, packed and operated. Examples of integrated elements are: a film resistor in a hybrid IC and an integrated transistor in an IC semiconductor.

An integrated circuit component also means a part of an IC that realizes the function of some electroradio element. However, before assembly this part was an independent article in special packing (complementing article). In principle, a component may be separated from a manufactured IC. Examples of integrated components are: a transistor without a housing or a ceramic capacitor in a hybrid IC.

1.2.2. Design Elements

In developing technical documentation for IC or in preparing descriptions of IC designs, writers of the indicated documents must frequently use such terms as housing, substrate, board, wafer, chip, as well as some special terms that determine special features of the internal structure of the IC.

The IC housing is the part of the IC structure intended to protect it from external effects and to connect it to external electrical circuits by leadouts (IC are packed in the housing). The types and sizes of the housings are also subject to government standardization (see GOST 17467-79 [4]).

The IC substrate is an intermediate product intended for elements of hybrid and film IC, interelement and (or) intercomponent connections, as well as contact pads to be applied to it.

The IC board is part of the substrate (or the entire substrate) of the hybrid (or frequently film) integrated circuit, to whose surface the film elements of the IC, the interelement and intercomponent connections and contact pads are applied.

The semiconductor wafer is an intermediate product of semiconductor material (usually it is a round thin disk) used to make IC semiconductors. It should be noted that in IC production this term is used not only for the initial intermediate product, but also for a plate with elements of semiconductor microcircuits formed on it (therefore, this term is used during the entire technological process from its beginning to the cutting of the group article into individual chips).

IC chips are the parts of the wafer obtained after it is cut (usually they form a network in the shape of equal rectangles), in the volume and on the surface of which are formed elements of the semiconductor microcircuit, interelement connections and contact pads.

A contact pad, present in any IC, no matter what its technological or functional features are, is a metallized pad on the plate or on the chip intended to connect contact leadouts and integrated circuits, as well as to monitor its electrical parameters and modes.

An integrated circuit without a housing is a term which recently acquired great importance because such circuits are used widely in microassemblies and microcircuits. While in the usual IC the housing serves to protect against external effects, the IC without a housing has no such protection of its own (at least, from mechanical effects). For connection to external electrical circuits, an IC without a housing must have its own leadouts and its full protection is provided by the housing of the device in which this IC is installed.

The leadout of an IC without a housing is a conductor connected electrically to the contact pad of the chip and mechanically to its surface. The main purpose of the leadout is to provide an electrical contact to one of the circuits of the IC without a housing when it is connected to external electrical circuits. Leadouts of the IC without a housing carry a considerable part of the heat. Leadouts of IC without a housing may be hard (round, columnar or beam-shaped). Hard leadouts may be used for mechanical fastening of an IC without a housing, without pasting it.

1.2.3. Simple and Complex IC

Until recently there was no decisive concept of the complexity of integrated circuits in literature, either abroad or domestically. When defining the term "large-scale integrated circuits" (BIS), an attempt was made to use, as the basis, the quantitative factor as well as the factor of the functional complexity of the microcircuit. In the first case, suggestions were made to define the BIS as a circuit containing 50, 100 or 10,000 circuit elements. For example, to define

a "large digital circuit" an attempt was made to use an elementary digital switch as a counting unit. In this case, it was considered that a "large" circuit must have no less than 100 digital switches. Concepts of "small," "medium" and "large" scale integration began to penetrate domestic leterature from abroad. However, deprived of numerical definitions, these concepts in each individual case, expressed only the subjective concepts of the author. In the seventies, following this tradition, in scientific literature, the terms "very large integrated circuit," "superlarge integrated circuit" and even "colossal integrated circuit" appear.

Supporters of defining BIS,depending upon its functional complexity, proposed dividing the circuits into four integration levels: elementary, circuit, subsystem level and finally, system level.

The study of all the proposals led to the idea that a quantitative factor must be used as a basis for a definition that defines precisely the quantity of the elements in the microcircuit chip or housing. GOST 17021-75 defined the term, "degree of integration of the integrated circuit," as an indicator of the degree of complexity of the IC, characterized by the number of elements and components. The degree of integration is defined here by formula K=lgN, where K is the coefficient defining the degree of automation, rounded to the nearest largest integer, while N is the number of elements and components in the IC. In accordance with this formula, an integrated circuit of the first degree of integration is called an IC containing up to 10 elements and components inclusive. An IC of the second degree of integration contains from 11 to 100 elements and components inclusive correspondingly, IC with 101 to 1000 elements and components inclusive should be called IC of the third degree of integration. Similarly IC with elements from 1001 to 10,000 or from 10,001 to 100,000 are IC of the fourth and fifth degrees of integration.

When designing electronic apparatus and selecting the elements, the so-called packing density of the elements in the integrated circuit is of great importance. By packing density is meant the ratio of the number of elements and components of the integrated circuit to its volume (without taking into account the volume of the leadouts).

1.2.4. Microassemblies and Microunits

GOST 17021-75, besides using terms with a direct relation to integrated circuits gives, in the form of reference material, a whole series of terms related to the field of application of IC. Such terms belong to the concept of microelectronics. Here it is defined as the field of electronics that spans the problems of research, design, manufacturing and the use of microelectronic products with a microelectronic product meaning an electronic device with a high degree of integration.

The term "microassembly" has several synonyms used in technical literature and documentation, but the definition of this term was not always given clearly. Thus, for example, before 1975 "microassembly" meant a microcircuit consisting of various elements and integrated circuits. The synonymsfor microassembly may be the terms used in literature such as: hybrid, integrated functional unit (GIFU), large integrated functional unit (BIFU), a large hybrid integrated circuit (BGIS) and a hybrid large integrated circuit (GBIS).

GOST 17021-75 defined the microassembly term as a microelectronic article that fulfills a certain function and consists of elements, components and integrated circuits (with and without housings), as well as other electroradio elements, in various combinations, developed and manufactured by developers of concrete radio-electronic apparatus for improving its miniaturization indicators. The GOST does not define a microassembly as an article with or without a housing, i.e., a microassembly may or may not have its own housing. Thus, a microassembly is not classified by the GOST by its complexity.

A microunit is a microelectronic article which, besides microassemblies, may contain integrated circuits and components. Finally, the miniaturization level term of a microelectronic article characterizes the quantitative measure of the effect of using the totality of technical solutions, directed to the full utilization of the advantages obtained from the reduction in volume, weight and power used by the apparatus.

Indicators of the REA [Radio-electronic apparatus] miniaturization level are: REA meeting the modern technical standard of microelectronic articles; other articles used in REA meeting the modern level of miniaturization; efficiency of comprehensive miniaturization of apparatus; technical compatibility of "nonintegrated" articles of electronic equipment, and electric equipment with integrated circuits.

1.3. IC Classification

Depending upon the manufacturing technology, integrated circuits may be semiconductor, film or hybrid. GOST 17021-75 gives the following definitions for these three varieties of IC.

A semiconductor integrated circuit is called an IC all of whose elements and interelement connections are made in the volume and on the surface of the semiconductor. The semiconductor integrated circuit may also be called a semiconductor microcircuit.

Sometimes the semiconductor integrated circuit is called a "solid" (or solid-body) circuit. This term found its way into domestic literature due to unqualified translations from the English*. GOST 17021-75 defines this term as inadmissible.

A film integrated circuit (or film circuit) whose elements and interelement connections are made in the form of films is called an IC. This film and thick film IC are variations of technical designs.

The difference between thin film and thick film IC may be quantitative and qualitative. Integrated circuits with a film thickness of up to 1 micron belong to thin film IC conditionally while integrated circuits with film thickness greater than 1 micrometer belong to thick film IC. Qualitative differences are determined

*Solid state electronics (English) -- semiconductor electronics.

by the manufacturing technology of the films. Elements of thin film IC are applied to the substrate, as a rule, by thermal-vacuum precipitation and cathode spraying, while elements of thick film IC are made primarily by silk screening with subsequent burning in.

Finally, hybrid integrated circuits (equivalent term -- hybrid microcircuits) are IC containing, besides elements, simple and complex components (for example, chips of semiconductor IC). A particular case of hybrid IC is a multichip IC (a totality of several IC without housings on one substrate).

Depending upon their functional purpose, integrated circuits are divided into two basic categories -- analog and digital.

Analog integrated circuits (analog microcircuits) are IC intended to convert and process signals that change in accordance with the continuous function law. A particular case of analog IC is an IC with a linear characteristic (linear microcircuit).

Digital integrated circuits(digital microcircuits) are IC used to convert and process signals expressed in a binary or other digital code. A variation of the digital microcircuit definition is the term logic microcircuit (operations with a binary code are described by logic algebra).

As a rule, analog and digital IC are developed and manufactured by manufacturing enterprises in the form of a series. Each series is characterized by the degree of completeness. A series contains several IC of distinctive types which, in their turn, may be divided into rated types.

According to GOST 17021-75, a series of integrated circuits contains a totality of IC which can implement various functions, but have a single design-technological form and are intended to be used in combination. As a rule, the composition of a promising series is being expanded with time.

IC that have concrete functional purposes and their conditional designations are called rated types of integrated circuits. By a type of integrated circuit is meant a totality of rated types of IC that have concrete functional purposes and their conditional designations.

1.4. System of Conditional IC Designations

The entire diversity of manufactured integrated circuits according to the adopted conditional designation system is divided into three groups: semiconductor, hybrid and others. Film IC, which are presently manufactured in a limited quantity, as well as vacuum IC and ceramic IC, are frequently referred to as the last group. The groups indicated above are assigned the following digits: 1, 5, 7 -- semiconductor IC (designation 7 is assigned to semiconductor IC without housings); 2, 4, 6, 8 -- hybrid IC; 3 -- other IC.

According to the nature of the functions implemented in radioelectronic apparatus, IC are subdivided into subgroups (for example, oscillators, modulators, triggers,

amplifiers) and types (for example, frequency, phase, duration, voltage converters). The classification of integrated circuits in accordance with their functional purpose is shown in Table 1.1.

According to the adopted system of designations, an IC must consist of 4 elements.

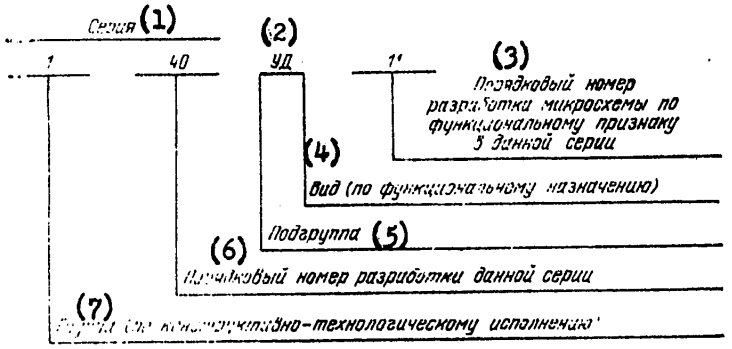
The first element -- a digit corresponding to the design-technological group.

The second element -- two-three digits assigned to a given IC series as the ordinal number of the development. Thus, in the first two elements are three-four digits that determine the total number of the IC series.

The third element -- two letters, corresponding to the subgroup and the IC type (see Table 1.1).

The fourth element -- the ordinal number of the IC development in a given series in which there may be several equal in the functional criterion of the IC. It may consist of one digit, as well as several digits. GOST 18682-73 does not limit this number.

Below is shown an example of a conditional designation of an integrated semiconductor operational amplifier with an ordinal of the series development -- 40, the ordinal number of the development of the given circuit in the series according to the functional criterion -- 11.



1. Series
2. UD
3. Ordinal number of a microcircuit development according to functional criterion in the given series
4. Type (according to functional purpose)
5. Subgroup
6. Ordinal number of given series
7. Group (according to the design-techological makeup).

Table 1.1

Functional classification of IC

Subgroup Name	Letter Designation	Type Name	Letter Designation	Letter Designation of the rated type
Oscillators	G	Harmonic signals	S	GS
		Rectangular signals (including self-excited multivibrators, blocking oscillators etc.)	G	GG
		Linearly changing signals	L	GL
		Special shape signals	F	GF
		Noise	M	GM
		Others	P	GP
Detectors	D	Amplitude	A	DA
		Pulse	I	DI
		Frequency	S	DS
		Phase	F	DF
		Others		
Switches and keys	K	Current	T	KT
		Voltage	N	KN
		Others	P	KP
Logic elements	L	Element AND-NOT	A	LA
		Element OR-NOT	Ye	LYe
		Element AND	I	LI
		Element OR	L	LL
		Element NOT	N	LN
		Element AND-OR	S	LS
		Element AND-NOT/OR-NOT	B	LB
		Element AND-OR-NOT	R	LR
		Element AND-OR-NOT/AND-OR	K	LK
		Element OR-NOT/OR	M	LM
		Expanders	D	LD
		Others	P	LP
Multifunctional circuits	Kh	Analog	A	KhA
	Digital		L	KhL
	Combined		K	KhK
	Other		P	KhP
Modulators	M	Amplitude	A	MA
		Frequency	S	MS

Table 1.1 continued

Functional Classification of IC

Subgroup		Type		Letter Designation of the rated type
Name	Letter Designation	Name	Letter Designation	
Triggers	T	Type JK	V	TV
		Type RS	R	TR
		Type D	M	TM
		Type T	T	TT
		Dynamic	D	TD
		Schmidt	L	TL
		Combined (types DT,RST etc)	K	TK
		Others	P	TP
Amplifiers	U	High frequency*	V	UV
		Intermediate frequency*	R	UR
		Low frequency*	N	UN
		Pulse signals*	I	UI
		Repeaters	Ye	UYe
		Read-out and retrieval	L	UL
		Indication	M	UM
		DC*	T	UT
		Operational and differential*	D	UD
		Others	P	UP
		*Voltage and power amplifiers (including low-noise		
Filters	F	Upper frequencies	V	FV
		Lower frequencies	N	FN
		Band	Ye	FYe
		Rejector	R	FR
		Others	P	FP
Shapers	A	Rectangular pulses (biased multivibrators, blocking oscillators, etc.	G	AG
		Special shape pulses	F	AF
		Address currents (shapers of voltages or currents)	A	AA
		Discharge currents (shapers of voltages or currents)	R	AR
		Others	P	AP

Table 1.1 continued

Functional Classification of IC

Subgroup		Type		Letter Designation of the rated type
Name	Letter Designation	Name	Letter Designation	
Modulators	M	Amplitude	A	MA
		Frequency	S	MS
		Phase	F	MF
		Pulse	I	MI
		Others	P	MP
Sets of elements	N	Diodes	D	ND
		Transistors	T	ND
		Resistors	R	NR
		Capacitors	Ye	NYe
		Combined	K	NK
		Others	P	NP
Converters	P	Frequency	S	PS
		Phase	F	PF
		Duration	D	PD
		Voltage	N	PN
		Power	M	PM
		Level	U	PU
		Code-analog	A	PA
		Analog-code	B	PA
		Code-code	R	PR
		Others	P	PP
Circuits for secondary power sources	Ye	Rectifiers	V	YeV
		Converters	M	YeM
		Voltage stabilizers	N	YeN
		Current stabilizers	T	YeT
		Others	P	YeP
Delay circuits	B	Passive	M	BM
		Active	R	BR
		Others	P	BP
Selecting and comparing circuits	S	Amplitude (signal level)	A	SA
		Time	V	SV
		Frequency	S	SS
		Phase	F	SF
		Others	P	SP

Table 1.1 continued

Functional Classification of IC

Subgroup		Type		Letter Designation of the rated type
Name	Letter Designation	Name	Letter Designation	
Memory matrices: elements	R	Storage		
		Main memories (OZU)	M	RM
		Permanent memories (PZU)	V	RV
		OZU with control circuits	U	RU
		PZU with control circuits	Ye	RYe
		PZU with control circuits and one-time programing	T	RT
		PZU with control circuits and multiple programing	R	RR
		Analog memory (AZU) with control circuits	A	RA
		Others	P	RP
Elements of arithmetic and discrete devices	I	Registers	R	IR
		Adders	M	IM
		Half-adders	L	IL
		Counters	Ye	IYe
		Coders	V	IV
		Combined	K	IK
		Others	P	IP

A letter is sometimes added to the end of the conditional designation that definesthe technological spread of the electrical parameters of the given rated type. The concrete value of the electrical parameters and the difference between the rated types is given in the tachnical documentation (for example, IC133LA1A differs from IC133LA1B).

In some series (this is also stipulated in the technical documentation), the letter at the end of the conditional designation of the IC defines the type of the housing used for the given rated type. For example, the letter P designates a plastic housing, while the letter M -- a ceramic housing. For microcircuits utilized in widely used devices, the letter K is at the beginning of the conditional designation. The designation then appears as K140UD11. If, after the letter K, there is also shown the letter M ahead of the series number, this indicates that all the given series is manufactured with a ceramic housing (for example, KM155LA1).

A series made for export(with a pitch of housing leadouts of 2.54 mm) is especially stipulated with the letter E before the letter K in the conditional designation, (for example, EK561LS2), while the series in the variation without housing, without leadouts being connected to the chip of the microcircuit -- is stipulated by the letter B ahead of the series designation (for example, KB524RP1A-4).

For IC without housings, in the shortened designation, a digit is introduced after a hyphen to characterize a corresponding design modification (for example, 703LB1-2); with flexible leadouts-1*; with ribbon leadouts, including those made with polyamide film-2; with hard leadouts-3; on a common plate (undivided)-4; separated without loss of orientation (for example, pasted on the film)-5; with contact pads without leadouts (chip)-6.

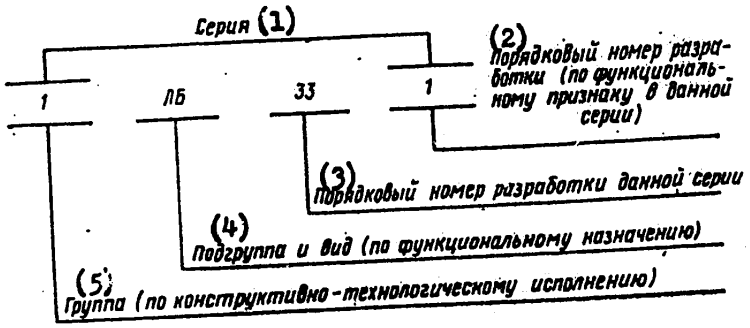
It should be noted that before the introduction of GOST 18682-73 [6] (i.e., before 1973), the assignment of conditional designations was made in accordance with the existing technical-norm documentation. After 1973, most IC received new conditional designations. However, for a certain number of IC for which no new technical documentation was issued, old conditional designations were continued.

The old and new conditional designations differ by the letter designations of subgroups and types (the latter is due to an increase in the number of types in GOST 18682-73 as compared to the previously existing documentation.

An example of the old designation of an IC type 1LB331 is shown on the next page.

---

*Modification "1" is applied to microcircuits with a number of leadouts no greater than 16.



1. Series
2. Ordinal number of development (according to functional criterion in the given series)
3. Ordinal number of development of the given series
4. Subgroup and type (according to functional purpose)
5. Group (according to design-technological makeup)

BIBLIOGRAPHY

1. Basic directions of national economy development for 1976-1980. Moscow, Politizdat, 1976.

2. Second supplement to publication MEK-147-0 (1966). Basic parameters and characteristics of semiconductor devices and general principles of measurements. General information and terminology.

3. GOST 17021-71. Microcircuits: Terms and definitions.
4. GOST 17021-75. Integrated microcircuits: Terms and definitions
5. GOST 17467-79. Integrated microcircuits: Basic sizes.
6. GOST 18682-73. Integrated microcircuits: Classifications and systems of conditional designations.

2291
CSO: 1863/209

CHAPTER TWO. METHODS OF FABRICATING INTEGRATED CIRCUITS

2.1. Film and Hybrid Technology

At the present time, film technology can be used to make passive components (resistors, capacitors, inductance foils) and also fabricate the connecting conductors, contact pads and microwave circuit components (such a stripline waveguides, attenuators, splitters). Active film elements (transistors and diodes) are as yet fabricated only under laboratory conditions for research purposes. Thus, the purely film IC's produced in the USSR and abroad are passive IC's (these are usually resistive voltage dividers, sets of resistors and capacitors, and RC networks). Film integrated circuit components are most often used in conjunction with miniature radio components, the components in hybrid IC's. Hybrid IC's, being inferior to semiconductor IC's in terms of reliability, component density, and production cost, have special circuit design advantages in a number of cases by virtue of the use of a broad products list of outboard components (transistors, micro-inductances, capacitors).

Hybrid technology is extremely flexible. It makes it possible to construct electronic devices relatively quickly which perform rather complex functions. The set of equipment for the fabrication of hybrid IC's is less expensive than for the fabrication of semiconductor IC's, while the production process itself is substantially simpler, and for this reason, the mastery of hybrid technology is accessible to practically any instrument making plant [1].

An advantage of hybrid technology is also the higher percentage yield of good IC's (60% to 80% as compared to 5 to 30% for semiconductor IC's). The rejects which occur in the manufacture of a hybrid IC can frequently be corrected. The design and planning methods for hybrid IC's do not differ from the design methods for conventional electronic circuits because of the discrete nature of the film elements and the outboard components. Because of the low parasitic capacitances and good insulation of the elements and components from each other, a hybrid IC has better electrical properties (lower induced currents and parasitic coupling) than a circuit composed of discrete, "large" radio components.

Hybrid integrated circuits are most frequently used in the design of analog equipment. It is especially convenient to use them to perform nonstandard functions, where large capacitors, high resistance, highly or precision resistors are required. The components of film and hybrid integrated circuits (resistors, capacitors, inductances) are made on the surface of the substrate in the form of films of different materials (resistive, conductive and dielectric materials).

Both thin and thick films are used in the manufacture of hybrid circuits. The choice between thick and thin films is governed by many considerations. Thick film IC's have the following advantages over thin film ones [2]. They are less expensive to develop and fabricate in the case of a small production series; lower capital outlays are required when setting up production (simpler equipment, less stringent requirements on the production rooms); they have greater mechanical strength; they have higher moisture, corrosion and thermal resistance; greater

overload capacity of the elements, as well as lower parasitic capacitances of the interconnections and lower mutual coupling of the elements.

Thin film integrated circuits have their own advantages over thick film ones: one can obtain more narrow tolerances for the nominal values of the components without trimming (resistors and capacitors); a higher layout density of the components on the substrate is achieved, where these components have lower high frequency losses and greater radiation immunity (by virtue of using a smaller products list of chemical elements with a high atomic weight).

It is preferable to use thin film hybrid circuits in very complex analog systems with strict tolerances for the elements, where extremely high stability is needed for the resistors. The scales of the proposed production of hybrid IC's also govern the choice of the type of films. If it is necessary to have a small number of products, then it is not expedient to set up production of thin film IC's, which require significantly greater capital outlays, and preference is to be given to thick film technology.

TABLE 2.1 The Parameters of Resistive Materials

Material	Specific Resistance, $\rho_{\square}$, Ohms	Temperature Coefficient of Resistance (10^{-6}/°C)	Permissible Power, W/cm^2	Nominal Tolerance, %
Chromium (on Cu with a Cr sublayer)	20--800	+180	2.0	±5
Nichrome (on Cu with a Cr sublayer)	100--300	+250	2.0	±5
Tantalum (on Au with Cr sublayer)	50--500	-400	3.0	±5
Stannic Oxide	500	±300	2.3--4.0	±2
NLT-3M alloy (on Cu with a Cr sublayer)	300--500	±200	1.0	±5
Metal ceramic on a palladium oxide base	up to 20,000	±200	up to 1.0	±10
Conducting paint on a carbon base	10,000	500--1,000	0.15--0.35	±10

2.1.1. Materials for Hybrid IC's

IC substrates are manufactured from sitall [ceramic glass, similar to pyroceram], glass or ceramic. The major requirements placed on substrates are: good

mechanical and dielectric properties, matching of the temperature coefficient of expansion to the other materials, as well as high surface purity (classes 12 to 14 in accordance with GOST 278a-73). Substrates of various sizes are used for the manufacture of hybrid integrated circuits [3]. The most widespread are rectangular substrates with the following dimensions: 6 x 15, 8 x 12, 11 x 11, 10 x 16, 12 x 12, 12 x 16, 12 x 20, 16 x 20, 24 x 30 and 48 x 60 mm (in this case, deviations from the nominal dimension amount to no more than 0.3 mm and the sides must be parallel within 0.5 mm). A number of substrate thicknesses are employed: 0.6, 1.0 and 1.6 mm (with a deviation of no more than 0.1 mm).

The substrate for thick film IC's should be heat resistant in order to stand up to annealing at several hundreds of degrees, which is necessary for fusing and securing materials from which the IC components are fabricated. In order to reduce parasitic capacitances between elements, materials are chosen having a low dielectric permittivity (if this effect is not employed as a useful one). Substrates with a high heat conductivity, for example, made of beryllium ceramic, for which the thermal conductivity is only five times worse than for copper, are used in the manufacture of high power IC's.

Regardless of the material, resistive films are characterized by the specific resistance per square surface unit area, $\rho_{\square}$. This quantity is an objective characteristic of films and depends on the specific resistance of the materials and the thickness of the film (but does not depend on the dimensions of the surface square).

Chromium, nichrome, tantalum, MLT alloy, metal ceramic, conducting paints and pastes are used for the fabrication of resistors. These materials make it possible to obtain a range of values of $\rho_{\square}$ from 20 ohms up to 20 KOhms. For better adhesion to the substrate, the resitive metal layers are placed on auxiliary metal sublayers. The parameters of some of the resistive materials are given in Table 2.1 [4].

The most suitable thickness for thin resistive films is considered to run from 0.01 to 0.2 micrometers. Having set the film thickness in this range, a material is chosen which provides the requisite specific resistance $\rho_{\square}$. In this case, one must take into account the fact that it is not always advantageous to select materials with a high resistance, since when removing them from the vacuum chamber, the thin films sometimes change their resistance by up to 50 percent as a result of oxidation in air. For thin film resistors, it is best of all to chose materials with $\rho_{\square}$ = 100 to 500 ohms, and for thick film resistors, 10 ohms to 20 KOhms.

Copper and gold with a sublayer of nichrome, aluminum or nickel are used as the materails for thin film conductors. Silicon monoxide frequently serves as the dielectric in the fabrication of film capacitors. In this case, it is best of all to use aluminum, since in terms of its electrical properties, it is quite well matched to silicon. The thickness of the conductors is chosen in a range of 0.3 to 1 micrometer (a sublayer thickness of 0.01 to 0.03 micrometers). Gold is frequently used for the fabrication of the bonding pads. The thickness of the bonding pads is usually chosen in a range of 0.5 to 4 micrometers.

Thick film conductors should have a specific resistance of no more than 0.1 ohms/ and should allow for soldering in the region of the bonding paths. Two kinds of thick film conducting materials are used: based on gold-platinum, which permit annealing at temperatures of up to 900 °C, and based on silver, which permit annealing at up to 700 °C.

Silicon monoxide, zinc sulfide, anodized tantalum, as well as chalcogenide glasses (KhG-44, IKS-24) are used as the dielectrics in the fabrication of film capacitors. The properties of silicon monoxide films depend to a great extent on the rate of vaporization and the composition of the residual gases in the vacuum chamber. Films of zinc sulfide are less critical as regards the deposition conditions. When choosing the dielectric material, its structure should be matched as best as possible to the structure of the other materials of the film circuit. The maximum thickness of dielectric films is limited by the resulting internal voltage and is on the order of 1.5 micrometers. The minimum thickness of a dielectric film is limited by the porosity of the structure and the specified working voltages (about 0.06 micrometers).

The specific capacitances, obtained when using silicon monoxide ($\varepsilon = 6$) fall in a range of 5,000 to 10,000 pF/cm^2. Anodized tantalum ($\varepsilon = 25$), titanium oxides ($\varepsilon = 80$) and barium titanate ($\varepsilon = 1{,}000$) can be used to obtain larger capacitances. The electrical strength of dielectric films depends to a considerable extent on the metal of the capacitor plate. Metals with a rather high vaporization temperature (for example, nickel and chromium) yield a greater number of short circuits, since the atoms of these metals, having a high energy, pass through the thin film of the dielectric when applying the upper plate to it. Silver and gold can also be the cause of plate short circuits, which occur because of the intense diffusion (migration) of the atoms of these metals from the plates along the grain boundaries of the film a short time following the application.

For this reason, aluminum is most often used for the plates in thin film IC's, since aluminum has a low vaporization temperature and low migration mobility because of the oxidation processes at its surface. The electrical strnegth also depends on the presence of pores in the dielectric film, since air in the pores is ionized at a lower voltage than the breakdown voltage of the solid film. The presence of microscopic pores can be related to the presence in the material being vaporized of impurities in the form of gas inclusions. Silicon monoxide and IKS-24 chalcogenide glass ($\varepsilon = 6$, $\tan\delta \leq 0.03$, a breakdown voltage of no less than $0.8 \cdot 10^6$ V/cm, a temperature coefficient of expansion of $5 \cdot 10^{-4}$ 1/°C in a temperature range of -60 °C to +125 °C) are used for the interlayer insulation.

2.1.2. The Fabrication of the Elements of Hybrid IC's

The major techniques for producing thin film components are thermal vaporization in a vacuum, cathodic and ion-plasma sputtering, and the precipitation of films from vapor and gaseous phases. Thick film components are produced on a substrate by means of silk screen printing. The choice of the specific film production

technique depends on many factors, especially on the composition of the substance being applied, the condition of the surface, the substrate temperature, the requisite thickness and the method used for monitoring it. The method of depositing thin films by means of thermal vaporization in a vacuum has become the most widespread technique in industry. The major merit of this method is its universality. One can obtain homogeneous layers of metals, alloys, semiconductors and dielectrics of various thickness in vacuum installations of the same type, and also fabricate thin films from different kinds of substances while determining the ratio of the parts for various thicknesses of each sublayer.

The process of producing films by means of thermal vaporization in a vaccum has the stages of vaporization of the material and the codensation of its vapors on the substrate. The material is heated for vaporization. Joule heating is used in this case which is liberated in conductors when an electric current is passed through them. One can also employ electron beam heating, radio frequency field heating as well as an electric arc. When heated in a vacuum, the material melts, and then goes to a vaporized state. In conventional industrial vacuum installations, a vacuum on the order of $133.322 \cdot 10^{5}$ to $133.322 \cdot 10^{-6}$ Pa [sic] is employed. However, a deeper vacuum is frequently needed to improve the structure of the films (down to $133.322 \cdot 10^{-8}$ to $133.322 \cdot 10^{-9}$ [Pa]).

The phenomenon of cathode destruction as a result of its bombardment with ionized molecules of a rarefied gas is employed to apply thin films by means of cathode sputtering. The cathode sputtering of films is accomplished at a pressure of $133.322 \cdot 10^{-1}$ -- $133.322 \cdot 10^{-3}$ Pa in a residual air atmosphere or in an inert gas (most often in argon). A high voltage of from 1 to 20 KV is applied between the cathode and anode to ignite a glow discharge.

The advantage of cathode sputtering over thermal vaporization in a vacuum consists in the fact that one can use it to obtain an increase in the surface area and uniformity of the thickness of the resulting films (the material is deposited on the substrate not from a point source, but from the flat surface of the cathode, the dimensions of which can be considerably greater than the spacing from the cathode to the substrate).

An important merit of the technique is the constant chemical composition of the material being sputtered, while in the case of thermal vaporization of the material, its components are vaporized at different rates, because of which the composition of the film can differ from the composition of the starting material. Films of difficulty fusible materials can be obtained by means of cathode sputtering.

In the case of ion-plasma sputtering, an initial pressure on the order of $133.322 \cdot 10^{-6}$ Pa is created in the chamber. Then, a thermal electron high density current (of several A/cm^2) is produced between the cathode and the anode of the installation, after which an inert gas at a pressure of up to $133.322 \cdot 10^{-3}$ to $133.322 \cdot 10^{-4}$ Pa is fed into the chamber, and a discharge is ignited by means of a high frequency transformer. The low energy ions occurring during the discharge bombard the substrate and remove the contaminants from its surface ("ion etching").

After this, a negative potential is applied to the target. The positive ions extracted from the discharge plasma bombard the target at an energy sufficient to atomize the atoms of the target material. The atoms knocked out of the target move predominantly in a direction perpendicular to the target surface [5].

The great merit of ion-plasma sputtering consists in its universality. Metals with different properties, for example, tungsten and gold, can be atomized with equal success. Such alloys as nichrome and stainless steel permalloy are atomized without the dissociation of the composition of the material being vaporized. In the case of ion-plasma sputtering, complex (alloy) films consisting of two or more metals can be fabricated by the simultaneous sputtering of several independent targets. Both pure semiconductor materials (silicon) and semiconductor compounds can be atomized.

A great advantage of the ion-plasma technique is its lack of inertia. The material is atomized only when a voltage is applied to the target; the sputtering ceases immediately after the voltage is turned off. The density of the depositing ion beam can be adjusted by changing the emission current of the tungsten cathode or the inert gas pressure. The deposition rate can be varied in a very wide range: from tenths of a nanometer up to tenths of a micron per minute. The uniformity of the film thickness with ion-plasma sputtering reaches one to two percent, which is considerably higher than in the case of cathode sputtering, where distortions are introduced in the nonconducting substrate, arranged between the cathode and the anode. Because of the high energy of the atoms impinging on the substrate, the strength of the film bond to the substrate where the film is obtained by the ion-plasma technique proves to be quite high.

The main advantage of precipitation from a gas phase consists in the ease of control of the process and its individual stages. In this case, one can comparatively easily introduce an additive into the growing film and obtain layers with properties specified beforehand. The technique is used in the fabrication of metallic, resistive and dielectric films. In this case, as a result of the decomposition of a complex chemical compound or the chemical reaction of two or more substances, the reaction product is precipitated in the form of a film on the substrate. The reaction can occur with the action of heat (pyrolytic decomposition), light (photochemical decomposition), or as the result of hydrolysis, exposure to an electrical field and other factors.

Following the application of the passive film elements to a substrate, the following components are installed on it: transistors, diodes, capacitors, transformers and semiconductor IC chips [6, 7]. Components with rigid leads are secured to the board by means of soldering or welding their leads to the contact pads of the board. Components with flexible leads are secured to the board by means of epoxy glues or are soldered. In the first case, the component is electrically insulated from the board, and in the second case, it can make electrical contact. The manner of fastening components to a board should provide for good mechanical strength of the fastening, the absence of stresses at the fastening point, chemical stability and neutrality of the materials used for the fastening, as well as their high heat conductivity, low formation temperature and high working temperature of the resulting compounds.

Epoxy glues have little shrinkage when they harden, good adhesion to various materials, do not liberate by-products and are chemically stable. Their polymerization temperature can be chosen in a wide range of values, including normal temperature, by means of selecting the hardeners. Fastening by means of soldering the chips of unpackaged semiconductor IC's, transistors and diodes is accomplished by the formation of eutectic alloys between the surface of the semiconductor and the gold layer on the board. The board is heated up to a temperature of about 370 °C, the chip is placed on the gold contact pad and pressed with a specific force. As a result, there is the mutual dissolution of the silicon and the gold with the formation of a eutectic alloy at the separation boundary.

2.1.3. Making Electrical Connections in Hybrid IC's

The leads of components which are fastened to a board are connected to contact pads, while the output contact pads are connected to the package leads. In the majority of cases, such connections are made using gold wires with diameters of from 25 to 50 micrometers by means of thermal compression, contact or ultrasonic welding.

The most widely used is thermal compression welding, in which pressure is combined with heating. The board and the gold wire are heated at the point of contact up to a temperature of 200 to 400 °C, the wire is pressed to the contact pad of the board with a force of from 0.05 to 0.5 N for a few seconds. The thermal compression technique requires careful selection and monitoring of the major parameters of the process: pressure, temperature and welding time.

Contact welding is accomplished by using a split electrode. The contact quality depends on the contact area, the specific resistance of the separation surface, and the resistance of the parts being welded. Because of this, the welding conditions are to be carefully selected for the specific conditions.

Ultrasonic welding, which is based on the simultaneous exposure to ultrasonic oscillations excited in the parts being welded and pressure in the weld region, provides for better quality of the weld joint than does thermal compression, as well as a lower welding temperature and a wider set of metals which can be welded. It also makes it possible to weld using a group technique.

2.2. Semiconductor Technology

The special features of semiconductor IC's, which determine the specific features of their fabrication technology, are as follows [8, 9]. The cost of integrated circuit elements is determined to a considerable extent by the area they occupy on the semiconductor chip. Thus, the cost of a transistor proves to be approximately equal to the cost of a diode, which in turn, approximately corresponds to the cost of a resistor with a nominal value of 4 KOhms with a tolerance of $\pm$30% or with a nominal value of 1 KOhm with a tolerance of $\pm$20%. The nominal values of elements having discrete prototypes are limited. It is not expedient in practice to use "pure" resistors with nominal values above 50 KOhm for mass produced IC's.

Capacitors having a capacitance exceeding a few hundred picofarads must be made in the form of individual outboard components. The desired nominal values of resistors cannot have small tolerances, although the ratio of the resistances of resistors of identical shape on a single chip can be maintained rather precisely (1 to 2%), where their temperature dependence will be the same. All semiconductor integrated circuit components are coupled together by means of parasitic capacitances and conductances, something which is due to the dense packing of the components and the imperfection of the methods used to insulate the components.

The advantages of semiconductor IC's over hybrid integrated circuits are as follows:

--Higher reliability because of the smaller number of contact connections, the limited number of materials which are used as well as because of the fact that a semiconductor IC can be fabricated only from a monocrystalline, ultrapure semiconductor structure;

--The great mechanical strength as a result of the smaller dimensions (approximately an order of magnitude) of the components;

--The lower production cost of semiconductor IC's because of the more efficient utilization of the advantages of group technology.

--Bipolar and unipolar (field effect) integrated circuits can be used as the active elements in semiconductor integrated circuits. Semiconductor IC's (especially digital) with bipolar transistors are distinguished by the higher pulse speed (or working frequency). Semiconductor digital IC's with field effect transistors having an MOS structure are distinguished by the maximum packing density of the components and the least production cost. Analog IC's with field effect devices have a high input impedance (more than 10^9 ohms) and can be quite economical in terms of the power consumption (microwatts). Unipolar transistor technology makes it possible to achieve better noise characteristics.

Bipolar transistors increase the operational stability of circuits in a wide range of temperatures, make it possible to realize the maximum operational speed and to design circuits with better load capabilities. Bipolar structures stand up better to electrical loads. It must be noted that the capabilities of unipolar structures are as yet far from completely uncovered (they are especially good for future radio frequency devices and operational amplifiers).

Because of the complexity of the equipment and the stringent requirements placed on the production conditions for semiconductor IC's, their manufacture becomes economically expedient only in the case of mass production (millions of pieces per year from one equipment complex). For this reason, in terms of semiconductor technology, it is expedient to fabricate the following: digital IC's and IC's for the realization of standard analog functions, as well as high reliability integrated circuits for the design of equipment with maximum component packing density.

2.2.1. Materials for the Components of Semiconductor IC's and Their Manufacture

Wafers of monocrystalline p or n type silicon are used in the majority of cases for the fabrication of semiconductor IC's, where these wafers are provided with epitaxial and so-called "hidden" layers. Compounds of boron, antimony, phosphorous, aluminum, gallium, indium, arsenic and gold are used as the doping impurities, by means of which the conductivity of the original material of the wafer is changed. Aluminum and gold are used to make interconnections and contact pads; silicon dioxide and polycrystalline silicon are used as dielectric coatings and insulation for elements. The materials used should have a very high purity: the impurity content in the majority of materials used in the manufacture of semiconductor integrated circuits should not exceed 10^{-5} to 10^{-9} parts of the base material.

By changing the doping impurity concentration in various parts of a monocrystalline semiconductor wafer in a definite manner, one can obtain a multilayer structure, which performs a specified electrical function and corresponds to a known extent to that equivalent to a discrete resistor, capacitor, diode or transistor [8].

The process of manufacturing modern semiconductor IC's is extremely complicated. It is carried out only in special hermetically sealed rooms using specialized equipment. The major production process operations for the fabrication of semiconductor circuits can be broken down into six steps.

1. The mechanical treatment of the silicon. Circular wafers with thicknesses of 250 to 400 μm are separated from a cylindrical rod of monocrystalline silicon with a diameter of 60 to 100 mm (in this operation, the thickness of the disturbed surface layer of the single crystal can exceed 80 μm). Cutting and polishing of the wafers is carried out to remove the disturbed layer, as a result of which, the thickness of this layer is reduced to 1 to 2 μm. Chemical etching is employed for the final finishing of the wafer surface.

2. Epitaxial growth. The term "epitaxy" means a process of the oriented growth of a crystalline lattice of silicon on a monocrystalline wafer through the deposition of layers. When additional impurities are introduced, it is possible to obtain epitaxial layers (films) with a specified type of conductivity (for example, one can obtain an epitaxial film with p-type conductivity on an n-type silicon wafer). The epitaxial layer, which takes the form of a monocrystalline extension of the base material, has no mechanical defects or stresses. Epitaxial growth is accomplished in special furnaces at temperatures of about 1,200 °C. The buildup rate of the film thickness is on the order of several microns per minute.

Epitaxial films 10 to 15 μm thick are the most widely used at the present time, however, to produce modern semiconductor digital IC's with a fast operating speed, the film thickness must be reduced down to a few microns.

3. The oxidation of the wafer surface. Oxidation of the wafers in an oxygen atmosphere or water vapor at temperatures of 1,000 to 1,300 °C is used to protect and mask the silicon surface during diffusion operations. The thickness of the built-up oxide is on the order of one micron.

4. Photolithography. A set of photolithographic processes is repeated several times during the production process for the manufacture of semiconductor integrated circuits (from 3 to 14 times). Each time, a thin layer (about one micrometer) of a light sensitive emulsion is applied to the oxidized silicon wafer: the photoresist, which is exposed through a negative with the image of the mask (in contrast to conventional photomagnification here, with a reduction). The requisite "windows" in the silicon oxide surface can be "opened up" in the photoresist after developing. The silicon oxide is etched away in these windows by a mixture of ammonium fluoride and hydrofluoric acid, and the silicon surface is thereby selectively exposed.

5. Diffusion. This process is carried out in special diffusion furances at a temperature of about 1,200 °C using special doping impurities. The following diffusants are used to obtain n-type conductivity: phosphorous, antimony, arsenic; boron, gallium and indium are used to obtain p-type conductivity.

6. Making interconnections. To create the "hook-up wiring" between the elements on the semiconductor IC substrate, the silicon wafer, which the elements formed on it (transistors, diodes and resistors), is coated with a layer of precipitated aluminum 0.5 to 2 μm thick, which is then etched away at the unnecessary points through the corresponding windows in the photoresist (following the final photolithography operation). In this case, the outline of the connecting aluminum conductors, having a width of about 10 μm, as well as the contact pads, remains on the semiconductor surface.

Several differents kinds of production processes, which differ primarily in the techniques used to produce the insulation between the individual integrated circuit components, are used at the present time in the electronics industry to make bipolar transistor semiconductors IC's.

Planar epitaxial technology with the insulation of the components by means of reverse biased p-n junctions is the most widely used. Drawbacks to this method of insulating structures are considered to be the increased values of parasitic capacitances and leakage currents between individual components, as well as their considerable area (taking into account the areas of the insulating regions), the relatively low breakdown voltages and the poor radiation immunity. However, structures with p-n insulation are the simplest to manufacture.

In isoplanar technology, the components are insulated by means of etching grooves between the elements with the subsequent thermal oxidation of the surface of these grooves. In this case, the layout density of the components is almost doubled, the radiation immunity is increased as well as the IC reliability, and the percentage yield of good integrated circuits is also increased.

Polyplanar technology provides for filling the gaps between the components with polycrystalline silicon, which makes it possible to increase the component

layout density even more (by a factor of three times more than in the planar process), and to reduce the parasitic capacitances between the components and increase IC realiability.

Technology utilizing anisotropic etching of the grooves (etching along the crystallographic axes) makes it possible to obtain an even greater component layout density.

The considerable diversity of technology processes (both simpler and more complex than bipolar) is used when manufacturing semiconductor IC's with MOS structures [10]. MOS structures are formed with three layers: the metal (M is the gate), the SiO_2 oxide (O is the gate insulation), and the semiconductor Si (S - the regions of the source, channel and gate). Standard technology (metal gate with single layer dielectric insulation about 100 μm thick) makes it possible to manufacture MOS transistors both with a p-channel and an n-channel (in the first case, the charge carriers are holes, and in the second, they are electrons; for this reason, n-channel MOS IC's have a faster operational speed than p-channel devices). The working frequency of digital MOS IC's, made using standard technology, does not exceed 1 to 2 MHz, while for analog devices, it is 300 to 500 MHz.

A two-layer dielectric is used in MNOS integrated circuits between the metal gate and the semiconductor: a layer of silicon dioxide about 50 μm thick and a layer of silicon nitride (N) 10 to 20 μm thick. The MNOS structures have a reduced threshold voltage as compared to standard MOS structures.

A progressive technology using silicon gates (regions of heavily doped silicon about one micrometer thick) is also used to boost the operational speed of MOS IC's. Using this approach, the speed of digital IC's has been successfully increased by a factor of three to five times, and the threshold cut-on voltage for a switch has been reduced while the component layout density has been increased by a factor of 1.5 times. The manufacture of MOS IC's on insulating substrates (sapphire or spinel with an epitaxially grown layer about one micrometer thick) makes it possible to increase the speed of such IC's at the present time up to 100 MHz (up to 250 MHz in the future).

The use of transistors with different polarities (p-channel and n-channel) as part of MOS IC's makes it possible to create digital IC's with relatively high speeds (up to 20 MHz) with a very low static power consumption (the product of the power consumption times the speed has a level of about 1 pJ). These structures are called CMOS (the letter C comes from the word complementary).

The fabrication of MOS IC's using double diffusion (first the p-channel is made, and then the n-layer in it) makes it possible to reduce the channel length down to one to two micrometers (using standard technology, a channel cannot be made with a length of less than 5 μm).

MOS transistors which oscillate at frequencies of up to 10 GHz can be manufactured based on gallium arsenide. In digital engineering, switches with a signal delay time of less than 1 nsec can be obtained using such integrated circuit transistors.

2.2.2. The Fabrication of Integrated Circuit Structures

Planar epitaxial technology is the most widely used in the production of transistors on semiconductor wafers (it is also used for the manufacture of modern discrete transistors). The difference in the characteristics of the transistors of semiconductor circuits and "conventional" transistors can be due to the properties of the insulating region, in which the transistor is located on the semiconductor circuit chip, as well as to the arrangement of the collector lead (in integrated structures, it is almost always the "top" one).

Integrated circuit diodes are easily made based on transistor structures. The emitter-base and collector-base junctions of transistor structures can be used as diodes. In some cases, the emitter-base junction can also operate as a stabilitron (Zener diode).

After forming the p-n junctions, it is necessary to make the contact pads at the requisite points and to connect the separate components of the semiconductor IC together. If the p-n junction was produced by means of diffusion, then it is necessary to apply a metal layer to the surface of the semiconductor wafer to obtain a good contact. This can be done, for example, by vacuum deposition. After fusing the metal into the semiconductor, low resistance p^+ or n-n^+ structures are formed. The external leads are secured to the metal contacts by means of thermal compression. One can avoid deposition on the metal contacts during the epitaxial growth process by introducing, where necessary, heavily doped p^+ or n^+ layers. Then the external leads can be connected directly to these layers using the same thermal compresssion.

Separate working components are connected together or to the contact pads by means of depositing aluminum in a vacuum on the semiconductor wafer surface which is oxidized beforehand, and in which windows are etched through to make contact with the semiconductor structure. The region between any pair of ohmic contacts on a semiconductor wafer can be used as a resistor. The resistance of such a resistor will depend on the length and cross-section of the region, as well as the specific resistance of the material. It can be calculated using the idfferential Ohm's Law.

Since the current in such a bulk semiconductor resistor will flow through the body of the semiconductor, the resistance of the resistors are less subject to the influnece of external conditions than the resistance of film resistors. The temperature coefficient, depending on the doping impurity concentration, can differ, however, as a rule, it is high and is positive. The resistance of three-dimensional semiconductor resistors is limited only by the dimensions of the semiconductor substrate and in practice can run up to 40 KOhms. Resistors which are made in the volume of a semiconductor chip are frequently used as thermal compensating resistors (with respect to the region where they are located in actual circuits, they are called collector resistors).

So-called "base" resistors (they are fabricated simultaneously with the base n-p-n regions of integrated circuit transistors) are more well known. This is the major type of diffusion resistor, in which the conducting channel is of p-type

conductivity. Such a channel is "bordered" by the n-region. After the supply voltages are applied to the chip, the insulating p-n junctions cut off and the current cannot overflow from the resistive channel into adjacent regions. Additionally, pinch resistors are widely used in IC's; these are nonlinear resistors which are "compressed" on the top by a cutoff p-n junction. They are high resistance devices and do not have a "conventional" equivalent" this is a field effect transistor with a small transconductance).

A three-layer p^+-i-n^+ structure can be used to create capacitors with a small fixed value of the capacitance in semiconductor integrated circuits. Two layers of such a structure are very heavily doped with the appropriate doping impurities. The middle layer is undoped material. The capacitance of the p^+-i-n^+ structures is determined by the thickness of the undoped layer and depends little on the inverse voltage level.

A reverse biased p-n junction is frequently used as a small value capacitor. The dielectric in such a capacitor is the junction region depleted of carriers. For any semiconductor, capacitance will be a function of the width of the depletion zone and the junction area. When silicon is used, one can obtain a specific capacitance of a p-n junction of up to 200,000 pFd/cm^2 for a breakdown voltage of several hundred volts. Since the width of the depletion zone depends on the applied voltage, the capacitance of the p-n junction is also a nonlinear function of the voltage.

Capacitors based on a p-n junction are polar capacitors, and for this reason they are not suitable for use in circuits with an alternating component. The latter drawback can be eliminated if two series connected p-n junctions are used. The capacitance of such a structure becomes independent of the working voltage polarity and depends little on its amplitude.

We shall treat in more detail some of the specific features of standard integrated circuit structures. The typical structure of an epitaxial diffusion transistor of a semiconductor IC is shown in Figure 2.1. Five diffusion layers are indicated in the vertical section through the structure. The emitter, base, epitaxial collector, hidden fusion n^+ layer and the chip (substrate). The specific resistance of the p-type chip is 10 Oh · cm. The epitaxial n-type layer which is 25 μm thick, and built-up on the surface of the chip, has a specific resistance of 0.5 Ohm · cm. The n^+ diffusion layer (usually arsenic) with a high concentration of doping impurities (more than 10^{19} atoms/cm^3) is placed beneath it.

The electrical insulation of the collector region from adjacent transistors (when a positive voltage will be applied to the circuit relative to the substrate) is assured through the presence of a deep separation diffusion region of p-type doping impurity through the epitaxial layer to the chip. This diffusion is accomplished first. The base is formed during the second diffusion of the p-type doping impurity into the epitaxial region of the collector (during this same time, the base and pinch resistors are made). The typical value of the resistance of the layer formed during the second diffusion (for example, with boron to a depth of 2.7 μm) amounts to 200 ohms/□ . The emitter is the n-type region which is formed during the third diffusion (for example, of phosphorous) into the base region to a depth of about 2 μm. The resistance of the emitter layer amounts to

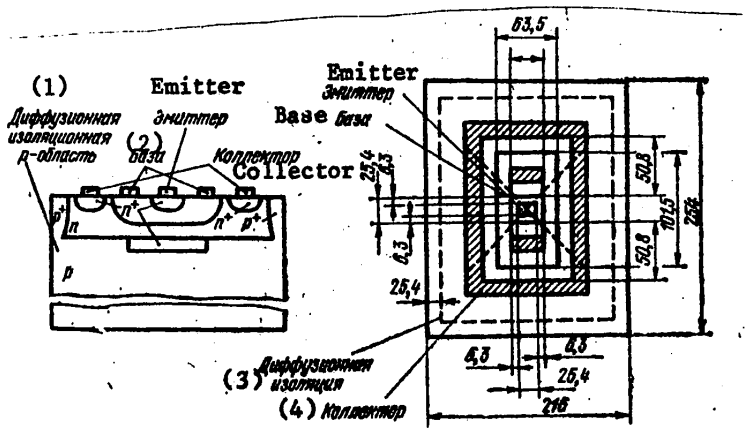


Figure 2.1. Structure of a transistor using p-n junction insulation (planar technology).

Key: 1. Diffusion insulated p-region;
2. Base;
3. Diffusion insulation;
4. Collector.

approximately 2 ohms/□. The doping depths of the junctions are: 2 μm for the emitter-base junction; 3 μm for the collector-base junction and 25 μm for the collector-chip junction. The plan view configuration of the transistor gives an idea of the dimensions of the structure on the chip surface. The emitter is the diffusion region with a rectangular shape having dimensions of 25 x 40 μm. It is formed after the diffusion of the n-doping impurity into the region of the p-base (the base area is 64 x 102 μm). The electrical contacts are made to the emitter, base and collector regions using aluminum metalization; the emitter contact is made with stripline metallization 12.5 μm wide. The contact with the base is formed by means of two strips arranged on both sides of the emitter. The contact is made to the collector with a rectangular metallized strip; it completely surrounds the diffusion collector-base junction. As can be concluded from an analysis of the topology, a considerable portion of the semiconductor surface is used for the insulation of adjacent structures from each other by the separation diffusion region, which is run to a depth of 25 μm. When the diffusion process is three-dimensional, the doping impurity atoms diffuse not only into the depth of the material, but also "leak out" in lateral directions. The distance to which doping impurities propagate in lateral directions is also approximately 25 μm. Such technology does not allow for attaining a high degree of component layout density on a chip.

The refinement of the fabrication technology for IC's with a high component layout density on a chip is more or less related to the passive insulation of the elements, i.e., to the replacement of active regions of p-n junctions, which electrically insulate active devices in conventional bipolar integrated circuits with any kind of dielectric material. One of the first developments was the technique in which electrical insulation of the elements on a chip was accomplished by a thermally grown silicon oxide. In this technique, a layer of silicon dioxide is used as the dielectric insulation instead of diffusion regions (Figure 2.2). The silicon dioxide forms the walls in the case of dielectric insulation as well as the bottom of each integrated circuit component and the structure is placed in a dielectric "pocket" (because of this the electric leakage is low). Such technology makes it possible to obtain higher voltage integrated circuit components on a chip than in the case of insulation using p-n junctions, however, the final advantage gained in terms of structure area is small.

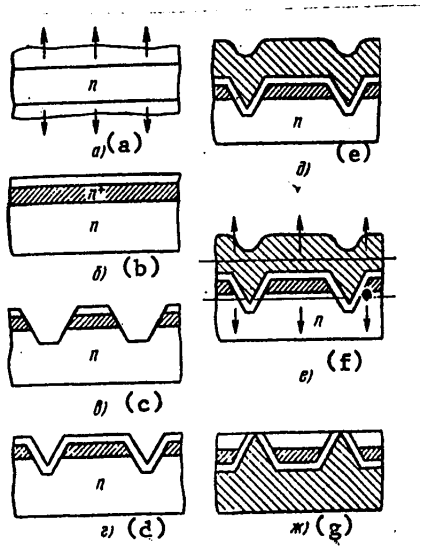


Figure 2.2. The sequence for the fabrication of a transistor structure using the dielectric insulation technique (the "epic" process):

a. Preparation of the wafer surface;
b. Deposition of the n^+ layer and the masking oxide;
c. Masking and etching of the insulating depressions;
d. Dielectric oxide build-up;
e. Deposition of the polycrystalline silicon;
f. Shaping of the wafer and polishing;
g. The final structure of the wafer.

The polyplanar process is a further development of technology using silicon dioxide insulation of the elements. In it, the surface of the insulating groove is coated with silicon dioxide, while the grooves themselves are filled with polycrystalline silicon, forming a smooth surface on the chip. The smooth chip surface makes it possible to use standard metallization, simplifies the layout of the intersection of conductors at various levels and improves the overall reliability of the IC's. The polyplanar process, just as the process using p-n junctions for insulation, starts with the selective formation of hidden diffusion n^+ type layers on p-type chip (Figure 2.3), after which an epitaxial n-type layer is grown on it. Then a layer of oxide is built up on the chip, in which, by means of standard photolithographic techniques, windows are etched out underneath the insulating

regions. Anisotropic etching of the silicon is carried out in the (100) crstallographic plane in the unprotected areas to form the insulating depressions. The depth of thd depressions is governed only by the geometric width of the hole in the masking material on the surface of the silicon.

Then a layer of silicon dioxide is grown in the resulting depressions where this layer is sufficiently thick to produce the requisite electric insulation. After this, in contrast to other processes which are based on etching the depressions, polycrystalline silicon is deposited on the surface of the chip, which completely fills the depressions. The excess silicon is then polished away as a result of which, a smooth chip surface remains. At this point in time, the side walls of the structure are completely formed and all subsequent production process operations do not differ from the standard ones adopted in planar epitaxial technology.

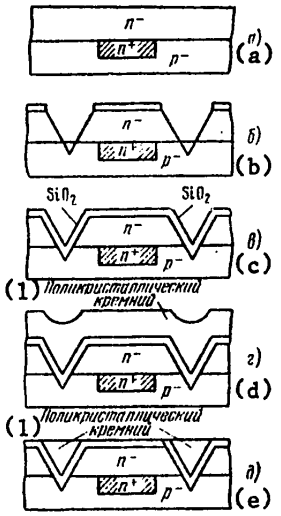


Figure 2.3. The sequence for the fabrication of a transistor structure using polycrystalline silicon insulation (polyplanar technology).

Key: a. Selective formation of the n^+ hidden diffusion layer and the build-up of the n-type epitaxial layer;
b. Masking and etching of the insulating depressions;
c. Build-up of the insulating oxide;
d. Deposition of the polycrystalline silicon;
e. Removal of excess silicon;
1. Polycrystalline silicon.

Small dimensions of the components are characteristic of polyplanar technology. The oxide grooves are separated from each other by a spacing of 10 to 15 μm. With such a technology, the area needed for creating an element is limited only by the thickness of the epitaxial layer and the minimum width of the insulating groove. Given the condition of optimization of technological process parameters, the area occupied by an element for a random access memory can amount to about 0.004 mm^2. The use of polyplanar technology has made it possible to significantly boost the layout density and reduce the sizes of chips as compared to the capabilities of standard technology. Thus, bipolar n-p-n transistors, together with the insulating region surrounding them, can have an area of about $0.3 \cdot 10^3$ μm^2. The area of the planar epitaxial diffusion transistor shown in Figure 2.1 is approximately $55 \cdot 10^3$ μm^2.

For comparison, we shall give figures which show the layout density of memory elements with insulation using p-n junctions, dielectric insulation as well as polyplanar insulation. A polyplanar matrix of memory elements with a capacity of 1,024 bits can be placed on a chip with an area of 2.6 mm^2; while for the same matrix with dielectric insulation a chip with an area of 4 mm^2 is needed and for a matrix with p-n junction insulation, an area of about 5.2 mm^2.

Standard isoplanar isoplanar technology makes it possible to obtain transistors with the smallest dimensions by virtue of the capability of producing thin base regions and small collector regions with oxide side walls [11]. The process of creating an isoplanar structure (Figure 2.4) begins with the formation of the n^+ regions in the p-type silicon wafer. Then, a thin p-type epitaxial layer is grown over the entire surface of the wafer. The built-up epitaxial layer is coated with a layer of silicon nitride from which a protective mask is formed to make the transistorsand resistors. The regions not protected by the nitride are etched away to a relatively great depth: down to almost the hidden layer. After this, long term low temperature oxidation is carried out, as a result, the deep etching regions are filled with insulating oxide, while the region coated with nitride remain unoxidized. To make contacts to the collector regions, deep n^+ diffusion is carried out. For this, the nitride is selectively etched with the corresponding areas of the silicon, which are practically untouched by the insulating oxide. The deep diffusion regions prove to be surrounded by the insulating oxide, which separates them from the base regions of the transistors. After creating the resistive regions, the nitride remaining on the wafer surface is etched away and replaced with oxide. Emitter windows are formed in the oxide in which the diffusion is carried out. Then the contacts to the base regions are opened up, the aluminum is deposited and with its etching, the formation of the structures is completed.

The further refinement of this technology will make it possible to obtain transistors with areas twice as small as compared to the original technological process through the capability of fabricating not only the base regions, but also the emitter regions directly adjacent to the oxide regions. The reduction in the area of the transistors fabricated using isoplanar technology is illustrated in Figure 2.5.

The isoplanar process provides for the creation of structures with a high layout density, since with a minimum number of technological variables, there is the capability of substantially reducing the dimensions of the insulating region. In this case, the surface resistance is quite high, which makes it possibel to obtain optimal electrical parameters for the IC's.

2.2.3. Separating a Wafer into Chips and Mounting the IC's

From several hundreds up to thousands of chips are fabricated simultaneously on a semiconductor wafer. The electrical parameters of the IC chips are measured even on the uncut wafer, and the nonoperating IC's are marked with paint [12].

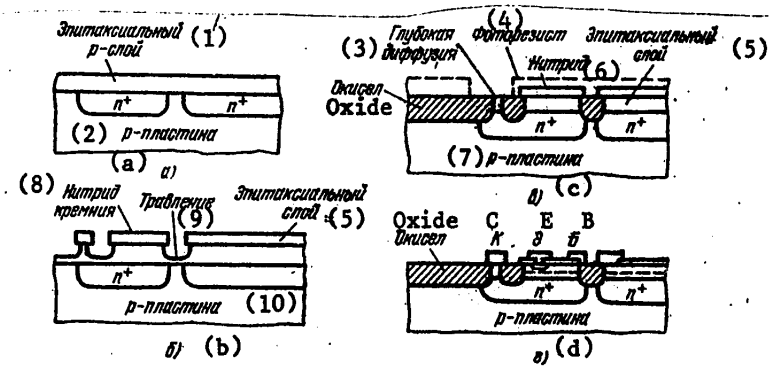


Figure 2.4. The sequence for the fabrication of a transistor structure using isoplanar technology.

Key: a. The formation of the epitaxial layer;
b. The etching of the insulating regions;
c. The formation of the insulating oxide and deep diffusion;
d. Final metallization;
1. Epitaxial p-layer;
2. p-wafer;
3. Deep diffusion;
4. Photoresist;
5. Epitaxial layer;
6. Nitride;
7. p-wafer;
8. Silicon nitride;
9. Etching;
10. p-wafer.

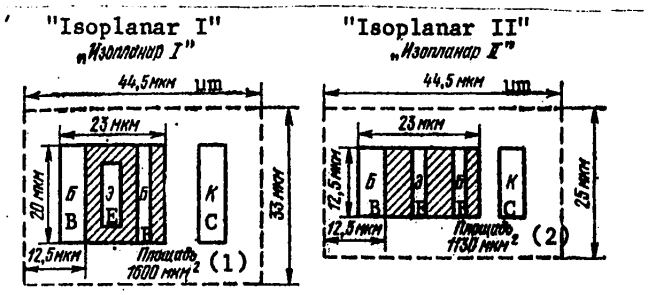


Figure 2.5. A comparison of the areas of memories made using "Isoplanar 1" and "Isoplanar 2" technologies.

Key: 1. Area of 1,600 μm^2;
2. Area of 1,130 μm^2.

Prior to breaking the wafer into chips, it is glued to a special film, which maintains the mutual positioning of the chips following the separation and prior to the operation of mounting them in a package. The separation of a wafer into individual chips can be accomplished in various ways. Scribing and breaking the wafer are accomplished by applying a grid of lines on the surface of the wafer using a diamong cutter with the subsequent breaking of the wafer along these lines with the application of bending forces (the method is similar to that of cutting glass). After separating the wafer, some of the "rectangles" can have visible chipped places, cracks and other defects. This is a frequently used and the simplest method of separating wafers. Equipment exists for making the grooves by means of a high energy laser beam with subsequent "cleaving" of the wafer.

The marked nonoperating IC's are rejected right away while the remaining chips are inspected under a microscope (especially the points where there are chipped places). The chips are mounted on the metal bases of the packages by means of brazing with the formation of a gold eutectic compound. In glass or plastic packages, in which there are no metal plates in the bases of the packages, the chips are fastened to the support frame with easily fusible glass in an inert gas atmosphere at a temperature of up to 525 °C. Then the output bonding pads for the internal leads of the package are installed.

2.2.4. The Hermetic Sealing of IC Chips

To protect the elements of an IC (especially if the IC will be delivered as an unpackaged unit) against exposure to the external environment (moisture, dust, mechanical loads), its chip should be hermetically sealed. The simplest hermetic sealing can be produced by coating the chip (or hybrid OC board) with a thin layer of protective varnish or compound (conformal coating). To protect IC's, one must use organic potting and coating materials which have good electrical insulating and moisture protective properties, resistance to exposure to elevated temperatures and to the cyclical actions of low and high temperatures, as well as have no incluence on circuit parameters, be elastic and reparable.

The selfvulcanizing elastic type KL compounds based on low molecular weight silicone SKTN and SKTI-1 rubbers can be recommended, where these operate in a temperature range of from -60 to +300 °C and under conditions of elevated humidity, as well as type PEK hermetic sealing compounds based on epoxy resin, modified with carbosilate rubber and polyester. These compounds are distinguished by their strength, elasticity and freeze resistance and provide for stability of the parameters are well as immunity to thermal shocks and long term exposure to elevated humidity. Used as the materials for moisture protection are the SB-1s, UR-231, UR-930 and E-4100 varnishes, the EP-096 epoxy-cresol varnish, the K-47 and K-57 silicone varnishes, as well as the EP-74T, EP-91, EP-92 and EP-9114 epoxy enamels. K-18, viksent [sic] and MBK compounds are used to protect the surfaces of chips.

All of the materials enumerated above possess good electrical insulating properties: a volume resistance of $\rho_V 10^{11}$ to 10^{13} ohm · m, a dielectric permittivity

of ε = 3 to 5 (at a frequency of 1 MHz), tan $\delta \leq 0.005$ to 0.01 (1 MHz) and an electrical strength of 20 to 90 KV/m. However, conformal coatings which make it possible to create so-called unpackaged IC's do not provide the requisite protection against exposure to the external environment and can be used only in conjunction with overall vacuum type hermetic sealing of the entire electronic unit or piece of equipment. For reliable protection against exposure to the environment during operation, the chips or boards are packed in sealed packages.

2.2.5. The Manufacture of IC Packages

As was indicated above, the major function of the package is to protect IC elements against the influence of the environment, assure normal operation of the IC during the entire service life and provide reliable mechanical and electrical bonding of the board or chip to the other elements of the electronic assembly. The following requirements are placed on an IC package.

The package should assure the requisite electrical connections between the circuit elements and the leads, and at the same time guarantee electrical insulation between the individual leads. The package structure should provide for heat sinking from the IC chip; the package should be made of materials which are inert with respect to chemically corrosive components in the environment (for example, oxygen, moisture and salts; in some cases, possible electrochemical processes should be taken into account, such as corrosion in the presence of electrolytes). Moreover, the package should be sufficiently strong to protect the IC elements against various kinds of damage during mounting and operation, but the package structure should be well suited to manufacture and applications (for this purpose, one must strive towards universality of the processes of mounting the IC's in equipment). The package should have a convenient structure for printed circuit mounting with respect to the dimensions and the arrangement of the leads. Also of no small importance is the fact that the package should protect the IC chip against the influence of light (and where possible, other external radiation), as well as absorb the natural radiation of the circuit components themselves and serve as a shield against external magnetic fields (or create a path for shorting the magnetic flux).

Four kinds of structural and production process designs of IC packages are the most widespread. The metal-glass package has a metal cap and a glass (or metal) base with the leads insulated and secured by means of glass; the cap is attached to the base by welding or soldering. The metal-ceramic package has a metal cap and a ceramic base; the cap is connected to the base by potting with a moisture resistant compound. The ceramic package has a ceramic cap and base; the cap is connected to the base by soldering. The plastic package (the least expensive) has a plastic body, which is produced by means of compression molding of the chip and the frame framework for the leads.

The complexity of fabricating IC packages increases with increasing functional complexity of the IC's, where the cost of a package in a number of cases becomes greater than the fabrication cost for the semiconductor chip (or the substrate with the film elements). When an IC is housed in a package, defects frequently

TABLE 2.2 Integrated Circuit Packages

Designation in GOST 17467-79	Basic Characteristics	Weight with Substrate, g	Dimensions, mm: Package	Dimensions, mm: Substrate or Chip	Number of Leads
1202.14	Rectangular, metal-glass	4.5	19.5x14.5x(4-5)	16x8	14
1203.15	The same	4.5	19.5x14.5x(3-5)	16x8	15
1211.15	The same	7.0	22.0x19.5x5	17x15	15
1211.15	The same	12.0	29.5x19.5x5	22.17	15
1303.36	The same	12.0	29x19x3.6	26x16	36
1209.29	The same	17.0	39x29x5	34x20	29
2123.14	Rectangular, plastic	1.0	19x7.2x3.2	5x3	14
2102.14	The same	1.2	19.7.2x3.2	5x3	16
2103.16	The same				
2135.24	Rectangular, metal ceramic	3.4	29x14.5x4	4x4	24
2204.48	Rectangular, ceramic	5.0	31x16.5x4	8x8	48
3101.08	Circular, metal-glass	1.5	D = 9.5, H = 4.6	3x3	8
3103.12	The same	1.5	D = 9.5, H = 4.6	3x3	12
4104.14	Rectangular, metal--glass	1.0	10x6.6x2.2	4.9x2	14
4110.16	The same	1.0	12.0x9.5x2.5	5.5x3.5	16
4116.24	Rectangular, metal-ceramic	1.6	19.5x12x2.6	7.5x5	24
4132.40	Rectangular, metal-glass	6.0	35.5x23.5x4.5	24x15	40
4136.48	Rectangular, ceramic	12.0	36x24x5	30x15	48
4137.50	The same	12.0	36.5x24.5x5	30x15	50
4140.64	Rectangular, metal-glass	20.0	54.5x38.5x5	30x24	64

occur which are related to the poor quality of the mounting or sealing of the packages. For this reason, two to three packages are sometimes expended before obtaining a good IC.

Standardization of the structural design of packages plays a great part in improving the reliability of IC's and microelectronic equipment. At the present time, GOST 17467-79 [state standard 17467-79] "Integrated Circuits. Basic Dimensions", is in force in the USSR, which establishes the requirements placed on the shape and dimensions of packages and integrated circuits (Table 2.2).

In accordance with this standard, packages can be of five types. An outline drawing of the structural design of a rectangular package with leads perpendicular

to the plane of the base and arranged within the bounds of the projection of the package body onto the plane of the base (a package of the first type) is shown in Figure 2.6a.

The second type of package with rectangular leads, perpendicular to the plane of the package base and going beyond the bounds of the projection of the package body onto the plane of the base is depicted in Figure 2.6b, while a circular package with leads perpendicular to the base of the package and arranged within the bounds of the projection of the package body onto the plane of the base (the third type of package) is shown in Figure 2.6c. Finally, a drawing of a rectangular package with leads arranged parallel to the plane of the base and going beyond the bounds of the projection of its body onto the plane of the base (the fourth type of package) is shown in Figure 2.6d.

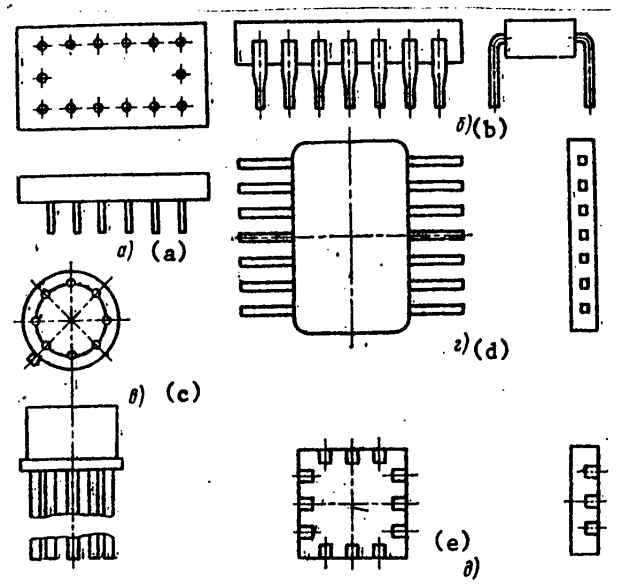


Figure 2.6. Outline drawings of package structures.

The fifth type of package is a rectangular flat "leadless package". The electrical connection of an IC housed in such a package is accomplished by means of metallized contact pads about the perimeter of the package (Figure 2.6e).

Packages which are similar in terms of their structural design are broken down according to overall size and connecting dimensions into standard sizes, to each of which a number is assigned which consists of the designation of the package subtype (12, 21, 31, 41, 51) and a two place number which designates the ordinal number of the standard size.

The spacing of the leads for the first and second types of packages is set at 2.5 mm and for the fourth and fifth types of packages at 1.25 mm. The leads can have either a circular or rectangular cross-section.

2.3. Specific Features of the Technology of IC's with a High Level of Integration

Integrated circuits of the first and second levels of integration (see §1.6) have made it possible to integrate the circuitry of traditional electronic equipment (these IC's appeared exclusively because of the influence of equipment problems). Integrated circuits of higher levels of integration are more the result of technological "initiatives": these IC's run ahead of the needs of equipment and are yet another step foreward in the continuing and continuous process of the further evolution of electronics [13]. The transition from the low level of integration IC technology to LSI technology takes place under the motto "From Circuit Integration to Systems Integration". For example, following the appearance of IC's of the fourth and fifth levels of integration, i.e., where the number of elements is more than 1,000 and 10,000, it became possible to produce new, quite complex functional assemblies such as memories and microprocessor sets on a single chip.

The increase in the level of integration of standard devices coincides with the group technique of fabricating IC's on a semiconductor wafer (or dielectric substrate), where several hundreds of identical circuits are produced simultaneously. Then the wafer is cut apart and chips are obtained, each containing one simple circuit (in which case, very many chips are rejected). The good chips are mounted in a package, where the chip is connected to the external leads of the package. The equipment manufacturer, by using connections made outside the packages (for example, printed circuit conductors) again combines a considerable number of identical circuits so as to obtain the requisite subsystem or system [14].

It is obviously desirable to eliminate intermediate operations (cutting the wafer, mounting the chips in a package, connecting the chips to the package leads, mounting the individual packages on a printed circuit board and connecting them to the printed circuit conductors). For this, one can leave the simple circuits on the original wafer, provide them with a definite system of interconnections, and thereby combine them into a subsystem on the wafer itself.

The overwhelming majority of defects in integrated circuits appear in the systems for transition contacts and interconnections. The contact pads of the chips are connected to the external package leads by means of thermal compression bonds. The breakage of these bonds which are made using manual labor is a rather widespread type of failure.

In semiconductor IC's of the third and higher levels of integration, the set of simple circuits which are joined together in a complex circuit is placed on a single chip and these circuits are connected together by metallized aluminum tracks. It is clear that in this case the overall number of external thermal compression connections is basically reduced (equal to only the number of package leads), something which leads to an improvement in the reliability. The reliability is also improved as a result of reducing the dimensions of the IC as compared

to the dimensions of an assembly consisting of the corresponding number of simple IC's, since the structure proves to be stiffer, less sensitive to vibration and shocks. Increasing the level of integration leads to a further increase in the layout density, to a reduction in the overall dimensions, and consequently the weight of radio electronic equipment assemblies, since the percentage of the volume and weight of the equipment allocated for the gaps between the IC's, the packages of the individual IC's and the printed circuit boards joining the IC's is reduced.

By virtue of the more optimal design of individual circuits taking the specific loads and connections into account, it is possible to reduce the power consumption of individual stages, which in the case of a high level of integration, can yield an extremely perceptible gain.

With the increase in the level of integration, it becomes possible in practice to realize a high operational speed for individual (usually micropower) simple circuits, since this reduces to a minimum the parasitic capacitance of connecting conductors.

However, increasing the level of integration entails an entire series of difficulties which are manifest at various stages in the design of the IC's. Thus, with an increase in the level of integration, the ICdevelopment time rises substantially. The labor intensity of the manual design of IC's can be approximated using the following formulas: the design time for analog IC's is $T_a = 70 \cdot N^{0.55}$; for digital IC's, the time is $T_d = 45 \cdot N^{0.55}$, where T is the labor intensity of the design work in hours, while N is the number of elements in the IC.

The design process can be accelerated by using machine techniques. In the case of computer assisted design, the design time is substantially curtailed: $P = 22 \cdot N^{0.22}$. The given functions were derived by Bulgarian specialists within the framework of scientific and technical cooperation of CEMA member nations.

The introduction of computer assisted design entails considerable preparatory work: the acquisition of expensive computers, the development of the relevant programs, and the mastery of machine design methods. All of this requires considerable funds and time, and for this reason, there is a certain amount of difficulty in the development of IC's of high levels of integration.

The actual capability of increasing the level of integration of IC's is tied to a great extent to the refinement of the production process quality in the process of manufacturing series produced products, i.e., to increasing the percentage yeild of good "conventional" products. The better the technological process is worked out, the more stable are its parameters and operating mode, the higher the percentage yield of good IC, and the greater the level of integration with satisfactory economic parameters that a new IC can have.

The process of measuring IC parameters poses considerable difficulty. In order to be sure of the requisite quality of all series produced IC's, it is necessary to make a large volume of measurements rapidly. For this reason, the quality control and measurement equipment needed for testing IC's takes the form of a complex automated system which is computer controlled.

For example, a measurement system for testing integrated circuits should feed 500-bit code combinations to the circuit. There are systems which execute up to 100,000 tests on one IC at a speed of from 20,000 to 286,000 tests per second, where up to 250 measurements can be made per second on each IC lead.

Despite the indicated difficulties, the level of integration of IC's is increasing at a very fast pace in step with the development of the capabilities of technology. It is anticipated that such a trend will be maintained at least until the 1980's. Thus, the number of elements on a single chip for semiconductor IC's may reach 200,000 to 1,000,000 in 1980. According to forecasts, the ultimate possible density of components for both bipolar and MOS integrated circuits will be achieved by the 1980's.

The reduction of bipolar transistor dimensions is limited by junction breakdown, the "punch-through" and doping impurity fluctuation phenomena. For circuits which operate only in dynamic modes, the package density is limited by the power dissipation.

The reduction of MOS transistor dimensions is limited by the breakdown of the gate-oxide gap and the "punch-through" of the drain-source gap. The power dissipation and migration of metal particles limits the layout density of MOS IC's which operate in a dynamic mode and complementary MOS IC's. For static circuits using MOS transistors with single polarity channels, the power dissipation is a major factor which limits the number of circuit functions on a chip (and consequently, the number of elements). The theoretical limit for the layout density of MOS transistors on a wafer amounts to 10^7 to 10^8 elements per cm^2, and for bipolar transistors, is 10^6 elements per cm^2.

Three major trends in the long term increase in the level of integration of semiconductor IC's have been noted at the present time.

First of all, there is a further refinement of temporary technological processes and the development of new processes underway. Thus, the transition from photolithography and diffusion of the doping impurities to the use of ion implantation and electron lithography makes it possible to increase the layout density of elements by an order of magnitude and substantially boost the percentage yield of good products. The layout density is also increased by an order of magnitude when injection supply circuits are used.

Secondly, an attempt is being made to change over to larger chips by refining the processes of photolithography and diffusion and improving the quality of semiconductor material. Thus, while the majority of IC developed during 1970--1973 had chip dimensions on the order of 1.5 x 1.5 mm, in 1973--1975 chips of from 2.5 x 2.5 mm up to 6.0 x 6.0 mm were being used and by 1980, it is planned that series produced IC's will be manufactured on chips with dimensions of 10 mm x 10 mm and more.

Finally, the techniques of IC design are being refined, new circuit design approaches are being developed (for example, one transistor is used instead of

three in the basic circuit of a random access memory, but it is equipped with capacitors), and injection logic circuits are being introduced.

The level of integration of hybrid integrated circuits will be increased primarily through the use of increasingly complicated unencapsulated semiconductor IC's [15]. The possibilities of this way of increasing the level of integration are considerable, while the use of unencapsulated microassemblies makes it possible to design radio electronic equipment of any degree of complexity.

We will note that at the beginning of the 1970's, progress in integrated circuit technology which had made it possible to sharply increase the level of integration of semiconductor IC's, was most effectively used by designers of electronic computers and their assemblies, and primarily, by memory designers. We shall consider a few examples of such devices. In 1975, the electronics industry started the production of main memories of 4,096 bits using MOS transistors made on a chip with dimensions of 4 x 4.7 mm and containing about 20,000 elements.

Progress in computer miniaturization through the use of IC's is characterized by the following data: desk type 8 to 10-digit computers (calculators) produced in 1964-1965 weighed more than 25 kg; in 1970, computers using several large scale integrated circuits weighed about 1 kg and in 1972, the production of pocket calculators just one IC in all was started, where these calculators weigh 200 to 300 g. At the present time, the eight digit "Elektronika B3-04" pocket electronic calculator has dimensions of 120 x 78 x 20 mm, weighs 200 g and has a power consumption of 600 mW. The pocket calculator is designed around four IC's which contain 7,000 MOS transistors. Calculators have been developed which perform four arithmetic operations, which are placed in a cigarette case, fountain pen and even in wrist watches.

Pocket calculators for engineers are produced at the present time which perform 20 to 40 and even more operations, including taking logarithms, calculating trigonometric functions and converting polar to cartesian coordinates. Thus, the "Elektronika B3-21" electronic pocket calculator (a 10 digit calculator) carries out 30 standard functions and operations (arithmetic, power, trigonometric, logarithmic and exponential). Moreover, the pocket calculator makes it possible to program calculations (up to 60 steps). The electronic portion of the pocket calculator is designed around four IC's which consume less than one watt.

At the beginning of the 1970's, the central portion characteristic of any computer, i.e., the processor (admittedly, having trunckated properties as compared to the processor of a "large" computer) came to be placed on a single chip primarily at the initiative of technologists who were looking for ways to apply their achievements in the field of producing regular semiconductor structures. Such semiconductor circuits were given the name microprocessors. Microprocessors, in conjunction with other IC's (read only and main memories, input/output devices as well as interfaces) form a finite microprocessor circuit, which is built on one printed circuit board. Both a conventional computer as well as a specialized control computer can be made from it.

Integrated circuits of low integration levels were previously for the design of the central processors of computers. It has become possible at the present time

to execute the majority of central processor functions (admittedly, at low operational speeds) by means of one or more third or fourth integration level IC's. Microprocessor sets (three to five packages) are the new "building block" of computer design. It is interesting that the appearance of such sets has caused a great deal of trouble of equipment designers, who had to change their traditional approach to the design of digital and even analog equipment.

The majority of modern microprocessors operate with word lengths of 4 and 8 bits, using parallel processing in this case. The difference between microprocessors and single chip calculators consist in the fact that they are program controlled devices (the permanent or programmable microprogram is placed in an individual IC of the permanent memory). The advantage of microprocessors consists in the fact that where they are used in a specific system, only a small number of IC packages is required, while adaptation for the solution of a new problem is accomplished by changing the control program.

Not just computer circuits can be made in the form of complex circuit configurations. For example, the digital circuitry for a voltmeter with four to five decades can be placed on a single chip (in this case, an IC having 24 leads contains binary decimal counters with a division factor of up to 100,000, a control circuit for the digital display, a control signal generator, a data erase control circuit and a five place ring counter). Electronic wrist watches have become ordinary, where an IC generats the time markers, converts them to a decimal code and turns on the appropriate segements of the light displays through encoders. The electronic industry is producing IC's for digital dialing telephone sets having a memory of 32 eight-place numbers. The IC is made on a 3.5 x 3.5 mm chip and contains about 3,000 elements.

In the development and fabrication of integrated circuits with levels of integration, questions of materials science, semiconductor device theory and the circuit design of radio electronic equipment assemblies merge into a single set of problems, and for this reason, IC designers are also compelled to resolve certain design questions which previously came within the competence of radio electronic equipment designers. For engineers who specialized in the field of IC design, this leads to the necessity of the unique "integrating" of knowledge from various fields of science and engineering.

It is important to note the initiating role played by IC's having an increased level of integration in the planning of subsequent generations of electronic equipment. It is becoming possible to construct not just highly reliable equipment, but also equipment which will prove to be automatically adaptable to the external environment.

BIBLIOGRAPHY

1. "Mikromoshchnaya elektronika" ["Micropower Electronics"], translation from the English edited by Ye.I. Gal'perin, Sovetskoye Radio, 1967.

2. Khamer D., Bigchers D., "Tekhnologiya tolstoplenochnykh gibridnykh integral'nykh skhem" ["Thick Film Hybrid Integrated Circuit Technology"], translation from the English edited by T.D. Shermergor, Moscow, Mir, 1975.

3. Sergeyev V.S., Bozhenin I.N., "Integral'nyye gibridnyye mikroskhemy" ["Hybrid Integrated Circuits"], Moscow, Sovetskoye Radio, 1973.

4. Gonorer M., "Mikroelektronika tolstykh plenok" ["Thick Film Microelectronics"], translation from the English edited by T.D. Shermergor, Moscow, Mir, 1973.

5. Veyko V.I., Libenson M.N., Melyuchev A.M., "Lazernaya tekhnologiya" ["Laser Technology"], Moscow, "Elektronika" Institute, 1970.

6. Lebedev O.T., Ogivin M.A., "Konstruirovaniye radioelektronnoy apparatury na osnove integral'nykh skhem" ["Radioelectronic Equipment Design Based on Integrated Circuits"], Leningrad State University, 1974.

7. Ushakov N.N.,"Tekhnologiya elementov vychislitel'nykh mashin" ["Computer Component Technology"], Moscow, Vysshaya Shkola, 1976.

8. Medlend G., Diken G., Richardson R., "Integral'nyye skhemy: Osnovy proyektirovaniya i tekhnologii" ["Integrated Circuits: Design and Technology Fundamentals"], translated from the English, Edited by K.I. Martyushov, Moscow, Sovetskoye Radio, 1970.

9. Ivanov-Yesipovich N.K., "Tekhnologiya mikroskhem" ["Microcircuit Technology"], Moscow, Vysshaya Shkola, 1972.

10. Penin V., Lou L., "Integral'nyye skhemy na MDP-priborakh" ["Integrated Circuits Using MOS Devices"], translated from the English, edited by A.N. Karmazinskiy, Moscow, Mir Piblishers, 1975.

11. Taryankov S.A.,"Dielektricheskaya izolyatsiya elementov integral'nykh skhem" ["Dielectric Insulation of Integrated Circuit Elements"], Moscow, Sovetskoye Radio, 1975.

12. Yefimov I.Ye., Kozyr' I.Ya., "Osnovy mikroelektroniki" ["Principles of Microelectronics"], Moscow, Svyaz' Publishers, 1975.

13. Khambata A., "Bol'shiye integral'nyye skhemy" ["Large Scale Integrated Circuits"], translated from the English, edited by B.I. Yermolayev, Moscow, Mir, 1971.

14. Gurevich D.Z., Yelizarov V.N., Ruvinskiy B.I., "Bol'shiye integral'nyye skhemy i EVM chetvertogo pokoleniya" ["Large Scale Integrated Circuits and Fourth Generation Computers"], Moscow, "Elektronika" Institute, 1970.

15. Chernyshev A.A., Aksenov A.I., Ivanov V.I., "Beskorpusnyye poluprovodnikovyye pribory" ["Unencapsulated Semiconductor Devices"], Moscow, Energiya, 1973.

CHAPTER THREE DIGITAL INTEGRATED CIRCUITS

3.1. Designation and Application

Digital integrated circuits (TsIs) are electronic devices which make it possible to construct practically all computer assemblies and circuits. In the overwhelming majority of modern computers and digital devices, the data being processed is represented in the form of binary numbers. The variables and functions of them which can take on only two values, 0 and 1, are called logic variables or logic functions. The properties of logic functions are studied in the algebra of logic, while the devices which realize the logic functions are called logic elements.

The simplest combination logic elements occupy an important place among modern digital IC's which are being produced by the electronics industry in both packaged and unencapsulated variants, along with complex circuits which realize the functions of entire circuits and assemblies (adders, counters, registers, memory elements). Among the existing logic elements (potential, pulse and pulse-potential), potential logic elements have become the most widespread, the distinctive feature of which is the existence of DC coupling between the circuit inputs and outputs. Direct coupled circuit designs eliminate the limitations placed on the lower signal frequency [1]. Circuit designs using the multiplicity of potential type digital IC's are realized on the basis of a number of standard basic functional components. The logic functions which can be realized using logic elements incorporated in the series of digital IC's and those which have found the most widespread applications in the construction of computer circuits and digital automation equipment are treated below [2, 3].

3.2. Logic Functions Which Can Be Realized Using Digital IC's

The simplest logic function is the NOT function (logic negation), which is written as $Y(X) = \overline{X}$. The truth values of the function Y(X) which are obtained by means of negating the variable X as a function of the truth values of the latter are determined from Table 3.1. Such a table is called a truth table.

TABLE 3.1

Negation

X	$Y(X)=\overline{X}$
0	1
1	0

Negation is realized in electronic circuits by means of a NOT switching element designed around an amplifying device. The signals at the switch output are inverted depending on the values of the input signals and correspond to Table 3.1. There exist $2^4 = 16$ different logic functions for the two variables X_1 and X_2, each of which is determined by four possible combinations of the variables [1].

Four of the most widespread types of logic gates are listed in Table 3.2 as well as the functions they perform, their designations and names. Each of the cited logic functions can also be extended to a larger number of independent variables, while the logic elements which realize these functions can also have not just two, but also n inputs. In actual digital

TABLE 3.2 The Most Widespread Types of Logic Elements and Their Functions

Logic Element	Function Performed	Variables X_1 | 0 0 1 1; X_2 | 0 1 0 1	Function Designation
AND	$Y = X_1X_2$	0 0 0 1	Conjunction
NAND	$Y = \overline{X_1X_2}$	1 1 1 0	Sheffer function
OR	$Y = X_1 + X_2$	0 1 1 1	Disjunction
NOR	$Y = \overline{X_1 + X_2}$	1 0 0 0	Pearce function

IC's, which take the form of logic gates, the number of inputs is limited by the number of leads in the standard packages, and as a rule, does not exceed eight. Following conversion of the Sheffer stroke and negation logic functions, the conclusion can be drawn that the function $Y(X_1X_2) = \overline{X_1X_2}$ is derived from the $Y(X) = \overline{X}$ function by means of replacing the argument X in it with the other logic function $Y(X_1X_2) = X_1, X_2$. Such an operation is called superposition. Complex logic functions can be obtained by using superposition.

The system of simple logic functions based on which one can derive any logic function using only the superposition operation is called a functionally complete system. For example, the following five systems will be functionally complete [1]:

$$\begin{cases} Y=\overline{X} & \text{— отрицание, negation} \\ Y=X_1X_2 & \text{— конъюнкция, conjunction} \\ Y=X_1+X_2 & \text{— дизъюнкция; disjunction} \end{cases} \quad (3.1)$$

$$\begin{cases} Y=\overline{X} & \text{— отрицание, negation} \\ Y=X_1X_2 & \text{— конъюнкция; conjunction} \end{cases} \quad (3.2)$$

$$\begin{cases} Y=\overline{X} & \text{— отрицание, negation} \\ Y=\overline{X}_1+X_2 & \text{— дизъюнкция; disjunction} \end{cases} \quad (3.3)$$

$Y = \overline{X_1X_2}$ conjunction negation (Sheffer stroke function); (3.4)

$Y = \overline{X_1 + X_2}$ disjunction negation (Pierce function). (3.5)

The functions missing in systems (3.2) ... (3.5) can be derived on the basis of the well known rules of algebraic logic [1]. Each of the systems indicated above can be realized by means of the appropriate logic gates. Thus, it is sufficient to have one NAND (or NOR) logic gate in order to use it as the basis for the construction of the entire diverse set of logic circuits. However, such an approach requires a large number of digital IC packages for the realization of the computer units and assemblies. In practice, logic gates

are incorporated in a digital IC series which not only realize a functionally complete system, but also have considerable diversity as regards the number of inputs, which makes it possible to minimize the volume of hardware in equipment design.

With respect to the kind of logic function which can be realized, the basic logic elements can be broken down into the simplest one-step (AND, OR, NOT, NAND, NOR) and two-step (AND-OR, AND-OR-NOT, etc.) logic gates.

It must be noted that all potential type logic gates can operate in two logic modes. The logic function which can be realized by the same element depends on the designations assigned to the electrical levels. If the "1" level is taken as the high level signal, "positive logic" is realized in the operation of an (NOR) gate. If a low signal level is taken as the "1" level, then we have "negative logic" for the operation of an (NAND) element [1]. As a rule, the data sheet designation of the logic element corresponds to the function realized in the "positive logic" mode.

Complex functional units of both a combinatorial type (half-adders) and with a memory (flip-flops) can be designed around logic elements with single and two-step logic. All of the modern series of digital IC's as a rule include various types of flip-flops, which take the form of a device with two stable states, containing a bistable memory element (the flip-flop itself) and a control circuit [1]. RS, D and JK flip-flops are the types which have become the most widespread.

A RS flip-flop has two information inputs: R and S. When S = 1 (the "one" input) and R = 0 (the "zero" input), the following signals appear at the flip-flop outputs: at the direct output Q = 1 and at the inverting output, $\overline{Q}$ = 0. When S = 0 and R = 1, the flip-flop output signals assume the opposite states (Q = 0, $\overline{Q}$ = 1). This flip-flop does not have a clock input. The truth table for a RS flip-flop is given in Table 3.3. With the simultaneous arrival of a "1" signal at the R and S inputs, the output signals of the flip-flop are indeterminate, and for this reason, it is necessary to preclude the mode in devices based on a RS flip-flop where both of the R and S signals are equal to one. The RS flip-flop (a bistable element) is present as the memory in other types of flip-flops.

A D flip-flop has an information input D and a synchronization (clock) input. The state of the flip-flop after the arrival of the clock pulse at the point in time (t + 1) coincides with the level of the input signal at the D input which acted at the point in time t. The input signal is delayed in a D flip-flop [1]. The truth table for a D flip-flop is given in Table 3.4.

A JK flip-flop has two information inputs, J and K, as well as a synchronization clock input. In contrast to the RS flip-flop, given the condition that J = 1 and K = 1, it inverts the previous state (i.e., reverses with the simultaneous arrival of J = 1 and K = 1). The truth table for a JK flip-flop is given in Table 3.5.

TABLE 3.3

Truth Table for a RS Flip-Flop

Time, t Время t				Время $(t+1)$	
(1) Предыдущая информация		(2) Записываемая информация		Result Результат	
(3) Выходы		(4) Входы		(5) Выходы	
Q	$\overline{Q}$	R	S	Q	$\overline{Q}$
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	0	1
0	1	1	1	X	X
1	0	0	0	1	0
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	1	X	X

Key: 1. Preceding information;
2. Information being entered;
3. Outputs;
4. Inputs;
5. Outputs.

TABLE 3.4

Truth Table for a D Flip-Flop

Time Время t			Время $t+1$	
Outputs Выходы		Input Вход	(1) Выходы (после подачи тактового импульса)	
Q	$\overline{Q}$	D	Q	$\overline{Q}$
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0

Key: 1. Outputs (after the clock pulse is fed in).

TABLE 3.5

Truth Table for a JK Flip-Flop

Time Время t				Время $t+1$	
Outputs Выходы		Inputs Входы		Выходы (после подачи тактового импульса) (1)	
Q	$\overline{Q}$	J	K	Q	$\overline{Q}$
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	0	1	1	0	1

Key: 1. Output (after the clock pulse is fed in).

It should be noted that besides the functional classification given above, distinctions can be drawn between flip-flops in accordance with the manner of data entry [1]. They can be asynchronous, where the information is entered directly with the arrival of the information signal, and clocked, where the information entry is accomplished only with the feed of an enabling clock pulse (fed to a special clock input). The actuation of a flip-flop can occur simultaneously with the arrival of the clock signal or after it is completed. The operational principle of flip-flops will be treated in more detail in subsequent sections in light of specific types of IC's.

The conventional designations (functional schematics) of the logic elements and flip-flops given above which are incorporated in the most widely used digital IC series and examples of their realization by means of logic gates performing various functions are given in Table 3.6.

TABLE 3.6 Functional Schematics of Logic Gates and Flip-Flops, Examples of the Realization of Various Functions by Means of Logic Gates

Element (Circuit)	Function Performed	Element (Circuit)	Function Performed
NOT (inverter) (Figure 1)	$Y = \overline{X}$	AND-OR-NOT (circuit based on NAND gates) (Figure 7)	$Y = X_1X_2 + X_3X_4$
AND (conjunction gate) (Figure 2)	$Y = X_1X_2$	AND-OR-NOT (Figure 8)	$Y = X_1X_2 + X_3X_4$
NAND (Sheffer stroke function) (Figure 3)	$Y = \overline{X_1X_2}$	Asynchronous RS flip-flop (the inputs in the R and S groups are coupled using AND logic) (Figure 9)	--
OR (disjunction gate) (Figure 4)	$Y = X_1 + X_2$	A JK flip-flop, designed on the principle of two stage storage of the data (the inputs in the J and K groups are coupled using AND logic) (Figure 10)	--
NOR (Pierce function) (Figure 5)	$Y = \overline{X_1 + X_2}$	A D flip-flop with a control input and R ("0" set) and S ("1" set) output (Figure 11)	--
AND-OR (circuit based on NAND gates) (Figure 6)	$Y = X_1X_2 + X_3X_4$		

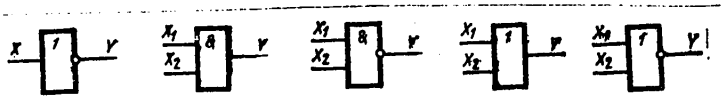


Fig. 1 Рис. 1 Рис. 2 Fig. 2 Рис. 3 Fig. 3 Рис. 4 Fig. 4 Рис. 5 Fig. 5

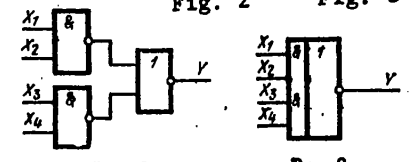


Рис. 6 Fig. 6. Рис. 8 Fig. 8.

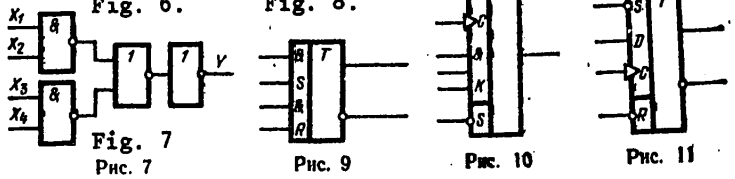


Fig. 7 Рис. 7 Рис. 9 Рис. 10 Рис. 11

3.3. The Classification of Digital Integrated Circuits and Their Main Electrical Parameters

The development of microelectronics over the past decade has promoted the appearance of miniature, highly reliable and economic computers based on digital IC's. The constant increase in the requirements calling for increased operational speed and reduced power consumption of computer hardware has led to the design of various bipolar digital IC's, the development of which, as a rule, is undertaken in series. A series is a set of IC's which have a single circuit design and structural and production process technology. Incorporated in a digital series, along with combination circuits which perform simple logic functions and flip-flops (memory elements) are also integrated circuits which take the form of entire arithmetic assemblies and modules. The series of bipolar digital IC's being produced by the electronics industries are broken down into the following types of circuits according to the types of basic electronic switches: resistor-transistor logic (RTL), diode transistor logic (DTL), resistor capacitor transistor logic (RCTL), transistor transistor logic (TTL), and emitter coupled transistor logic (ECTL). In these designations, the word logic is substituted for the concept of electronic switch.

Digital IC's using MOS structures (enriched channel p-type transistors, CMOS circuits using complementary transistors, etc.) have become widespread along with bipolar circuits. Although the RTL, RCTL and DTL series continue to be produced by industry, they are only used to put together equipment sets for series produced radioelectronic equipment and are not used in new designs. The TTL, ECTL and MOS circuits have become the most widespread in modern equipment. Experience has shown that these types of digital IC's are distinguished by better electrical parameters, are convenient to use, have a higher level of integration and possess a greater functional diversity. Thus, for example, about forty IC's are included in the 155 series, while in the K145 series there are IC's having more than 9,000 equivalent elements on a chip. The promising series of digital IC's of the types mentioned above, which are intended for applications in industrial and consumer electronics equipment, are shown in Table 3.7.

As has already been indicated, the majority of digital IC's incorporated in a series take the form of logic gates which perform the NOT, NAND, NOR and AND-OR-NOT functions. These are the so-called basic functional elements. Their main electrical parameters govern the characteristics of practically all of the IC's included within the complement of a series. The possibilities for joint operation of IC's of different series in the same equipment depend on these parameters. A number of the major electrical parameters are common to all types of digital IC's and make it possible to compare them with each other. Such parameters include the following: speed, power consumption (P_{con}), the noise immunity (U_n), the fan-out factor for the output (load capacity, K_{out}) and the fan-in factor for the input (K_{in}).

We shall treat each of these parameters in more detail [1]. The speed is governed by the dynamic parameters of the digital IC, which include the

TABLE 3.7 Digital IC Series for General Applications in Industrial and Consumer Equipment

Series	Number of IC's in the Series (1978)	Function
		TTL Integrated Circuits
K155	76	Construction of computer assemblies and medium speed digital automation hardware.
133	43	The same
130	12	Construction of high speed computer assemblies and digital automation hardware
K131	11	The same
134, 734 (unencapsulated)	30, 8	Construction of computer assemblies and digital automation equipment with a low power consumption; The same
530 K531 K555	8 15 12	The construction of computer assemblies and digital automation hardware with a high operational speed and low power consumption
		ECTL Integrated Circuits
100	42	Construction of high speed computer complexes
K500	39	The same
700 (unencapsulated)	37	The same
		Integrated Circuits Using p-Channel MOS Transistors
505	8	The construction of main computer memories for all types of computer systems
K527	2	The same
K507	3	Joint applications with the 508 and K508 integrated circuit series in the main memories of radio-electronics equipment
K145	51	Microcalculator construction
		Integrated Circuits Using n-Channel MOS Transistors
K565	2	Construction of main computer memories (OZU) for all types of computer systems

TABLE 3.7 [cont.]

Series	Number of IC's in the Series (1978)	Function
		Integrated Circuits Using CMOS Transistors
164 764 (unencapsulated)	24 12	Construction of miniature digital automation and computer hardware with a low power consumption
564 765 (unencapsulated)	33 9	The construction of miniature digital automation and computer hardware with a low power consumption
K176	33	The same
		Integrated Circuits Based On Glass Semiconductor Switches
K524	2	Construction of erasable programable read-only memories for computers and digital automation systems
		Integrated Circuits Using Transistors With Nitride Oxide Insulation (MNOS)
509	1	The construction of erasable read-only memories for computers and digital automation systems
519	2	The same

following: $t^{1,0}$ is the time for the transition from the logic one state to the logic zero state; $t^{0,1}$ is the time for the transition from the logic zero state to the logic one state; $t_{zd}^{1,0}$ is the turn-on delay time; $t_{zd}^{0,1}$ is the cut-off delay time; $t_{zd.r}^{1,0}$ is the propagation delay time during turn-on; $t_{zd.r}^{0,1}$ is the propagation delay time during cut-off; $t_{zd.r.avg.}$ is the average propagation delay time; τ_i is the pulse width and f_r is the working frequency.

The read-out levels relative to which the dynamic parameters are determined are shown in Figure 3.1. The average propagation delay time is defined in accordance with the formula:

$$t_{zd.r.avg.} = 0.5(t_{zd.r}^{1,0} + t_{zd.r}^{0,1}). \qquad t_{зд\,р\,ср} = 0{,}5\left(t_{зд\,р}^{1,0} + t_{зд\,р}^{0,1}\right).$$

This parameter serves as the averaged parameter for the operational speed which is used in the calculation of the time characteristics of series connected digital IC's.

The following are the most frequently cited in the handbook data for digital IC's from the list of dynamic parameters indicated above: $t_{zd}^{1,0}$ and $t_{zd}^{0,1}$ the

turn-on and cut-off delay times, as well as $t^{1,0}_{zd.r}$ and $t^{0,1}_{zd.r}$ the propagation delay times during turn-on and cut-off.

Potential logic gates, when operating as part of a digital device, can be either in a static mode which is characterized by one of two states ("0" or "1"), or in a switching stage. Depending on the type of logic gate, the power consumed from the power supply will differ for each of these states. Some elements consume considerable power in the static mode, which increases only insignificantly at the moment of switching, while others, on the other hand, are characterized by a relatively low power consumption in the static state and a considerable increase in the power consumption in the transient processes. Logic gates with a low power consumption in the dynamic mode are characterized by the average power consumption:

$$P_{con.avg.} = 0.5(P^0_{con.} + P^1_{con.}),$$

where P^0_{con} is the power consumed by the circuit in the "0" state, while P^1_{con} is the power consumed by the circuit in the "1" state. For these circuits, the power consumed at the point in time of the transient processes does not exceed the power consumed in one of the logic states.

Logic gates with a large dynamic power consumption are characterized by the power consumed at the maximum switching frequency, when the currents in the power supply circuits increase sharply, in addition to being characterized by the average static power consumption. The CMOS integrated circuits are examples of such circuits.

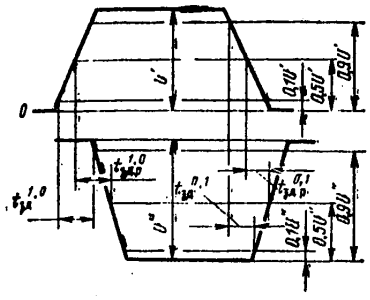


Figure 3.5. The readout levels for dynamic parameters.

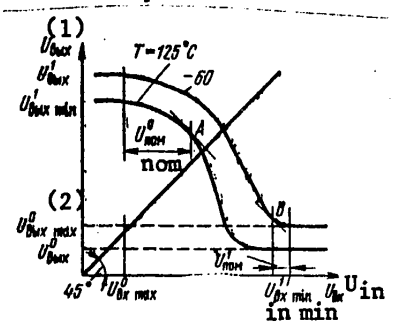


Figure 3.2. The transfer functions of a NOT logic gate and the ultimate transfer functions for the family [of IC's] obtained at various temperatures.

Key: 1. U_{out} 2. $U^0_{out\ max}$.

The static noise immunity of logic switches defines the level of the voltage which can be fed to the switch input relative to the "0" or "1" level without causing it to falsely actuate [1]. Since a logic gate in the static mode can be in one of two states ("0" or "1"), a distinction is drawn between the static noise immunity for the "0" level (U^0_n) and the "1" level (U^1_n). The values of U^0_n and U^1_n are determined from the transfer functions (Figure 3.2).

As can be seen from Figure 3.2, the parameter U_n^1 is defined as the difference between the minimum "1" level ($U_{in\ min}^1$) and the point B voltages on the upper curve. The parameter U_n^0 is defined as the difference between the voltage at point A on the lower curve and the maximum voltage for "0" ($U_{in\ max}^0$) To completely evaluate the noise immunity of a circuit, it is necessary to take into account the dynamic noise immunity along with the static value. The dynamic mode noise immunity depends on the width, amplitude and waveform of the interference signal, as well as the level of the static noise immunity and the switching speed of the logic gate.

The fan-out factor for the output (the load capability), K_{out}, characterizes the number of similar gate inputs which can be connected to the output of the logic switch. With an increase in the load capacity, the possibilities for digital IC applications are improved and the number of packages in the digital device under development are reduced. Simultaneously with an increase in the number of loads, some of the IC parameters are degraded: the speed and noise immunity fall off and the power consumption increases. For this reason, high power buffers with K_{out} = 20 to 30 are included in an IC series along with the main logic gates having a load capacity of K_{out} = = 4 to 10. This makes it possible to obtain optimal indicators with respect to the number of IC packages which are used and the power consumption when designing digital devices.

It must be noted that in RTL and RCTL circuits, the load inputs consume current from the output of the loaded element, while DTL and TTL circuits in one logic state deliver current to the load, and in the other receive current from the load. The load is of a capacitive nature for MOS circuits.

The input fan-in factor (K_{in}) defines the maximum number of digital IC inputs. A distinction is drawn between the input fan-in factor for an AND ($K_{in\ AND}$) and for an OR ($K_{in\ OR}$) gate.

In the existing series of digital IC's, the main logic gates are made with a small number of inputs ($K_{in\ AND}$ = 2 to 4; $K_{in\ OR}$ = 2 to 4). To increase the number of inputs in individual logic elements, incorporated in a series, special inputs are provided for the connection of an "expander", which provides for an increase in the fan-in factor of up to 10 and more. An expander circuit is correspondingly incorporated in a series as an individual element. There are logic elements with eight inputs in a number of IC series.

3.4. Transistor-Transistor Logic Circuits

Transistor-transistor logic gates (TTL) appeared as the result of the development of diode-transistor logic, through the replacement of the matrix of diodes with a multiple emitter transistor (MET). An MET is an integrated circuit component which combines the properties of diode logic gates and a transistor amplifier. The AND function in a TTL switch is performed in the base and collector regions which are common to several emitters. The basic structural difference between an MET and conventional transistors consists in the fact that it has several emitters arranged in such a fashion that direct coupling between them is practically eliminated by a passive base region which separates them. Thus, the MET represents a set of several transistor structures, having a common collector and which interact directly with each other through the motion of the majority carriers. We shall treat the operation

of a multiemitter transistor using the example of a NAND gate (Figure 3.3.) with a simple inverter (unipolar switch) [4].

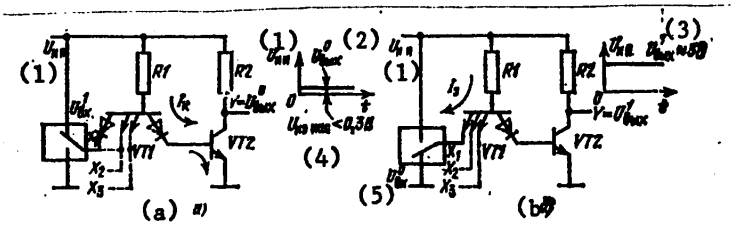


Figure 3.3. The current distribution in a NAND gate with a simple inverter where a "1" is fed to the input (a) and a "0" is fed to the input (b).

Key: 1. U_{ip} = Supply voltage, V_{cc};
2. U^0_{out};
3. U^1_{out} of approximately 5 volts;
4. $U_{KE\ NAS} = V_{ce\ sat} \approx 0.3$ volts;
5. U^0_{in}.

If voltages corresponding to the "1" level (U^1_{in}) are fed to all of the inputs of an MET, the emitters of the input transistor do not received the turn-on bias current (a sufficient potential difference is not present). In this case, the current delivered to the base of the MET through resistor R1 flows from the supply V_{cc} to the collector circuit I_K [I_c], which is forward biased, and then to the base of transistor VT2. Transistor VT2 is saturated in this case and the voltage at the output of the circuit corresponds to the "0" level (U^0_{out}). All of the MET transistor structures are in the inverse active mode in this case, since their collector junctions are forward biased, while the emitter junctions are reverse biased. If the "0" voltage (U^0_{out}) is fed to one of the MET inputs, the corresponding base--emitter junction is forward biased. The current fed to its base through resistor R1 flows in this emitter circuit. In this case, the MET collector current falls off, transistor VT2 cuts off and the voltage at the circuit output becomes equal to the "1" level (U^1_{out}).

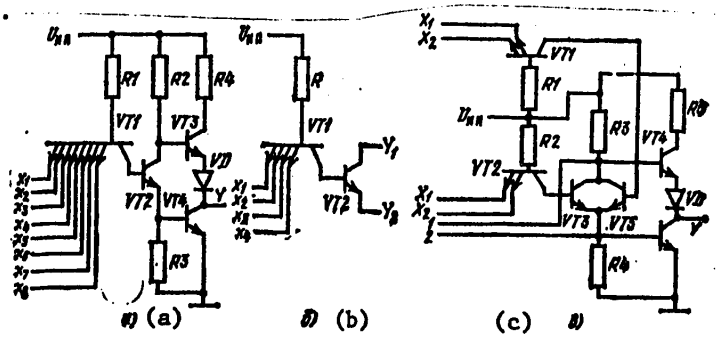


Figure 3.4. Schematics of an 8-input TTL NAND logic gate (a), an OR expander (b) and an AND-OR-NOT logic gate (c)

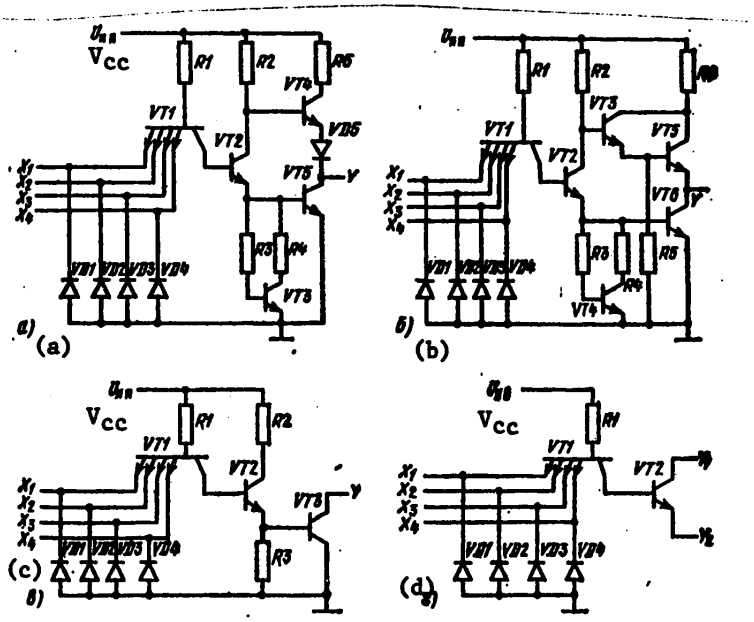


Figure 3.5. Basic schematics of standard TTL series.
a. NAND logic gate (133LA1 and K155LA1 IC's);
b. NAND logic gate with a large fan-out factor (133LA6 and K155LA6 IC's);
c. Circuit with an open collector (133LA7 and K155LA7 IC's);
d. OR expander (133LD1 and K155LD1 IC's).

TTL circuits with a simple inverter have not found widespread applications because of the poor noise immunity, low load capacity and poor speed of the unipolar switch when operating as a driver for display elements. With the development and refinement of the technology, a dual polarity switch became the basic circuit for TTL switches with a complex inverter (Figure 3.4a). The use of a complex inverter made it possible to increase the speed over that of the simple circuit configuration (especially in devices with multiple layer printed circuit boards), as well as the noise immunity and fan-out, and also reduce the requirements placed on the transistor parameters; the latter led in turn to an increase in the percentage yield of good IC's.

Several variants of TTL series circuits are produced at the present time. These are the standard 133 and K155 series (functionally analogous to the SN54/74 developed by Texas Instruments); high speed series: 130, K131 (functionally analogous to the SN54 H/74H series; here, the H designates increased speed); and the micropower series 134 (functionally analogous to the SN54L/74L series; here, L indicates a lower power consumption); series with Schottky diodes: 530 and K531 (functionally

analogous to the SN54S/74S; here, S indicates the presence of Schottky diodes in the structures); and the micropower series with Schottky diodes, K555 (functionally analogous to the SN74LS).

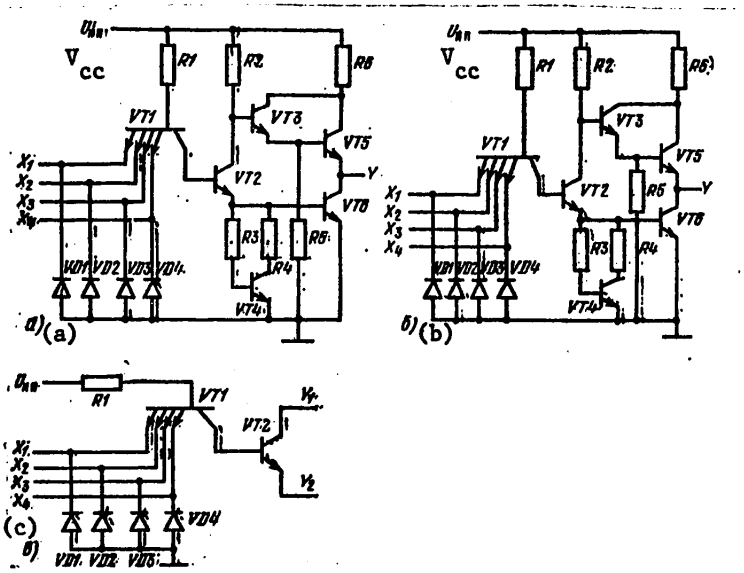


Figure 3.6. Basic schematics of the high speed TTL series.

Key: a. NAND logic gate (130 LA1 and K131LA1 integrated circuits);
b. NAND logic element with a large fan-out factor (130LA6 and K131LA6 integrated circuits);
c. OR expander (130LD1 and K131LD1 integrated circuits).

In terms of circuit design, almost all of the logic gates incorporated in the indicated series can be formed by a combination of two basic circuits: a NAND logic gate (Figure 3.4a) and an OR expander (Figure 3.4b). An OR expander in conjunction with a NAND logic gate forms an AND-OR-NOT logic gate (Figure 3.4c). By connecting the expander (Figure 3.4b) to points 1 and 2 (Figure 3.4c), one can increase the fan-in load for the OR logic input. For all TTL circuits which have the OR expansion capability, the maximum fan-in is eight inputs. When one expander is connected the circuit propagation delay increases by approximately 5 nsec, while the power consumption increases by 5 mW. TTL logic gates have a high fan-out load capacity (K_{out} = 10).

The large output and comparatively low input currents promote good matching of the circuits to each other. As a rule, the complement of TTL series includes a circuit with an open collector output (Figure 3.5c) and a logic element with a large fan-out factor (improved load capability) (Figure 3.5b). Basic schematics of each of the varieties of TTL series indicated above are shown in Figures 3.5 to 3.8.

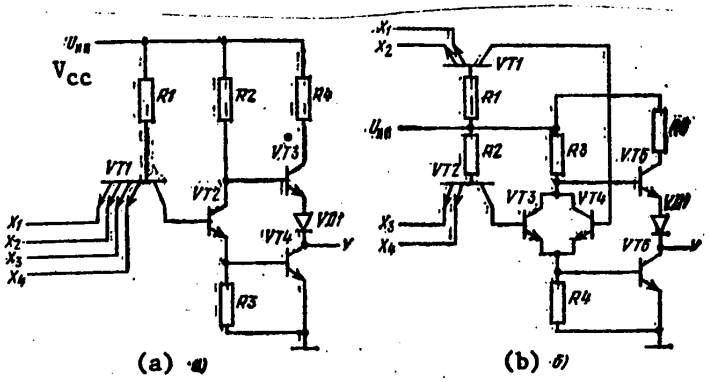


Figure 3.7. Basic schematics of the micropower TTL series.

Key: a. NAND/NOR logic gate (134LB2 IC);
b. AND-OR-NOT logic gate (134LR1 IC).

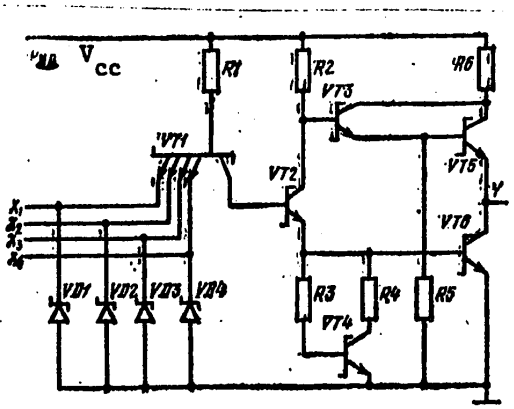


Figure 3.8. Basic schematic of Schottky diode TTL (NAND logic gate, 530LA1 and K531LA1 IC's).

We shall consider the operational principle of TTL circuits using the example of a NAND logic gate, which is shown in Figure 3.4a [4]. The circuit contains simple n-p-n transistors (VT2, VT3, VT4), a multiemitter transistor VT1, as well as resistors R1 ... R4 and diode VD. Such a circuit provides for the capability of operating into a larger capacitive load with high speed and noise immunity.

The circuit of a basic TTL gate consists of the following elementary stages: the input multiemitter transistor VT1 with a low inverse current gain, a phase splitter, designed around a transfer transistor VT2 (this stage operates with a small working current and has low p-n junction capacitances); and the push-pull output stage VT3, VT4. Transistor VT4 is designed for a large working current and has a short saturation cutoff time during circuit switching. The input currents of the load switches flow through this transistor to ground.

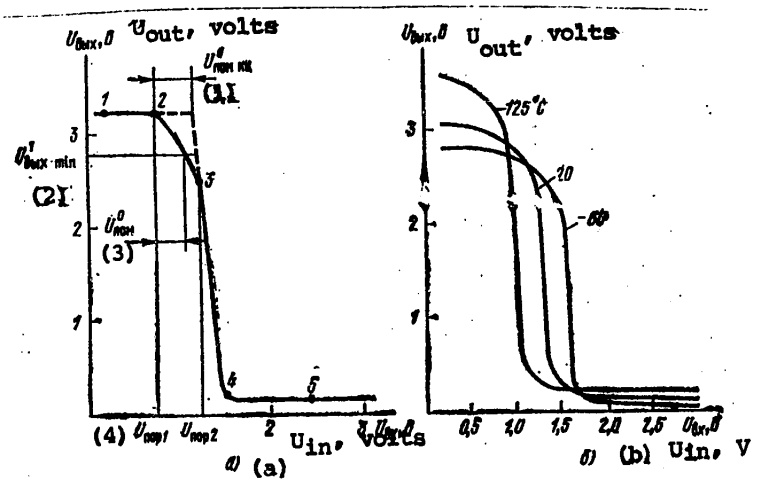


Figure 3.9. The transfer characteristics of a standard series TTL NAND gate for T = 25 °C (a), and in a range of temperatures (b); V_{cc} = 5 volts, K_{out} = 10 [fan-out]; the dashed curve applies to circuits with a correcting network.

Key: 1. $U^0_{\text{noise cor. net.}}$; 2. $U^1_{\text{out min}}$;
3. U^0_{noise}; 4. $U_{\text{thresh.1}}$.

The ability of TTL circuits to work into a large capacitive load at high switching speeds is explained by the fact that with these circuits, both the charging and discharging of the load capacitance is accomplished through the low impedance output network. However, when switching the states of the output transistors, there is a point in time when they are both turned on. Because of this, short term but high power current pulses occur in the power supply circuit, where these pulses can lead to the appearance of interference pulses. To avoid this in equipment constructed with TTL circuits, it is necessary to design a power supply with low lead inductance and to provide decoupling between adjacent assemblies.

We shall analyze the transfer function (Figure 3.9a) of the NAND logic gate shown in Figure 3.4a. When $U_{in\ 1} = 0$ (the ground potential is applied to one of the emitters of transistor VT1), the base-emitter junction (b-e) of transistor VT1 is turned on, but the potential which is produced in this case, $U_{b\ VT1} = 0.8$ volts, cannot turn on three p-n junctions: the base-collector junction (b-c) of transistor VT1, the b-e junction of transistor VT2 and the b-e junction of transistor VT4 (a potential of approximately 3 x 0.6 = 1.8 volts is needed to turn on this circuit). The potential at the base of transistor VT4 is close to 0 and transistor VT4 is turned off. The potential at the collector of VT2 and at the base of VT3, which is close to the supply voltage of +5 volts, turns on the b-e junction of transistor VT3 as well as diode VD, producing the current I^1_{out}. The voltage at the collector of transistor VT4 is correspondingly equal to U^1_{out} (section 1 - 2).

With an increase in U_{in} (at all of the emitter inputs to transistor VT1) up to the threshold voltage level $U_{thr\ 1} = 0.8$ volts (point 2 on the transfer function),

transistor VT2 begins to conduct, but transistor VT4 is still cut off, and with a further increase in U_{in} up to the voltage level of $U_{thr.2}$ = 1.25 volts, transistor VT2 turns on, while transistor VT4 only begins to conduct (point 3 on the transfer function).

A further increase in U_{in} leads to an increase in the potential at the base of transistor VT1 up to 1.2 volts. This is altogether sufficient to turn on two junctions: the b-c junction of transistor VT1 and the b-e junction of transistor VT2. Transistor VT2 turns on, and the current through resistor R2 increases, which causes a reduction in the voltage $U_{c\ VT2}$. An increase in the current through resistor R3 causes the potential at the base of transistor VT4 to increase and makes it conduct. The turned-on transistor VT4 (section 3--4 of the transfer function) shunts resistor R3, which sharply increases the transmission gain of transistor VT2 and causes a further reduction in the voltage $U_{c\ VT2}$. However, transistor VT4 has already been turned on for some time while transistor VT3 is still not turned off, something which leads to a current spike and an increase in the power consumed from the supply. The current consumption is limited in this case by resistor R4, as well as the bulk resistances of transistors VT3, VT4 and diode VD. This is the so-called short-circuit current which leads to an increase in the power consumption in the dynamic mode.

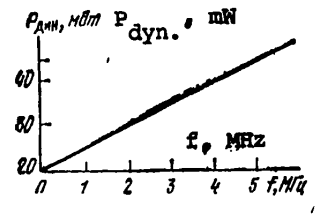


Figure 3.10:
The dynamic power as a function of switching frequency where V_{cc} = 5.25 v, T = 70 °C and C_{load} = = 15 pFd.

With a further increase in U_{in}, transistors VT2 and VT4 change over to the saturation mode (section 4--5 of the transfer function) (Figure 3.9a). The potentials $U_{c\ VT3}$ and $U_{c\ VT4}$ will be 1.2 and 0.3 volts respectively. Their difference, which is equal to 0.9 volts, is not sufficient to turn on the base-emitter junction of transistor VT3 and the junction of diode VD. The presence of diode VD (Figure 3.4a) provides for shifting the turn-on level for transistor VT3 as well as reliably turning it off when U^0_{out} = 0.3 volts.

In real TTL circuits (Figure 3.5a), in contrast to the simplified NAND circuit (Figure 3.4a), an equalizing network is tied to the base of the output transistor in place of resistor R4, where this network consists of resistors R3 and R4 as well as transistor VT3. The insertion of the correcting network makes it possible to produce a transfer function shape close to rectangular (Figure 3.9a) and thereby improve the noise immunity in the logic "1" state as compared to the noise immunity of the circuit shown in Figure 3.4a ($U^0_{n\ eq.net.} > U^0_n$).

The resistance of the correcting network is less temperature dependent than resistor R4, something which provides a number of special properties for the circuit. At an elevated temperature (125 °C), the recovery time for transistor VT5 (Figure 3.5a) is short, which promotes a rapid cutoff of the circuit. This in turn reduces the short circuit current pulse (when transistors VT4 and VT5 are turned on simultaneously) and means that the dynamic power consumption is also reduced. At reduced temperatures (-60°C), the resistance of the correcting network exceeds the resistance of the resistor R4 (Figure 3.4a), which increases the turn-on current of transistor VT5 and correspondingly leads to a reduction in the circuit switching time.

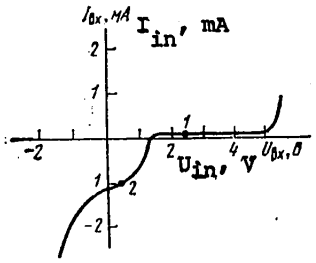


Figure 3.11:
The input characteristic for the case w[illegible]e V_{cc} = = 5 v and T = 25 °C.

As can be seen from the curves of Figure 3.9b, the characteristic shifts to the left with increasing temperature, something which reduces the circuit noise immunity at a temperature of 125°C.

As was shown above, at the moment of switching of the NAND circuit, the current consumption increases, which in turn leads to an increase in the dynamic power consumption.

It can be seen from the characteristic curve (Figure 3.10) that with an increase in the frequency up to 5 MHz, the power consumption rises to 43 mW as compared to 20 mW in the static mode. The current spikes in the supply circuit, which is inductive, can produce induced currents and degrade the noise immunity of the equipment.

We shall analyze the input characteristic (Figure 3.11) of the NAND logic gate shown in Figure 3.5a. In the case of joint operation of TTL circuits, one of the circuits serves as the load for the other. Two modes are possible in this case. When the control IC is in the "1" state (point 1 on the input characteristic curve) and the voltage at its output is equal to U^1_{out} (Figure 3.12a,b), the b-e junction of transistor VT1 of the load IC is cut off and the current I^1_{in}, which is governed only by the inverse current through the cut-off junction, is quite low. The control IC is shown in Figure 3.12b in the form of a switch. If the control IC is in the "0" state (point 2 on the input characteristic curve) and the voltage at its output is U^0_{out}, the b-e junction of transistor VT1 of the load IC is turned on and the input current changes its direction: it flows from the power supply of the load circuit through the conducting b-e junction of transistor VT1 and the conducting transistor VT4 of the control IC to ground (Figure 3.12c, d).

As can be seen from the input characteristic, when U^1_{in} = 5.5 volts, the input current I^1_{in} increases sharply, reaching a level of 1 mA. This value of the input voltage is the ultimate permissible value and exceeding it can cause the circuit to fail. The value of the input current I^0_{in} increases in a similarly sharp fashion with an increase in the negative voltage at the input. For the majority of TTL series, the ultimate permissible value of the negative voltage at the IC input is 0.4 volts. In actual equipment circuits, the signal fed to the IC input does not have a strictly rectangular or trapezoidal waveform. At the moment of signal termination, decaying oscillations appear in the hookup wiring, which can cause false actuation of the circuitry. To prevent such false actuations, a number of TTL circuits have been refined, as a result of which, so-called damping diodes, VD1 ... ... VD4 are connected to each of the multiemitter transistor inputs (Figure 3.5a).

When there is no oscillatory process at the input, such a diode is turned off and inserts an additional capacitance at the circuit input of less than 1 pFd, which does not degrade the dynamic characteristics of the circuits for practical purposes. With the first negative pulse which exceeds 0.8 volts, the damping diode turns on and limits the amplitude of the pulse to a level of 0.8 volts, the subsequent positive voltage pulse becomes considerably less than 0.8 volts (does cause the

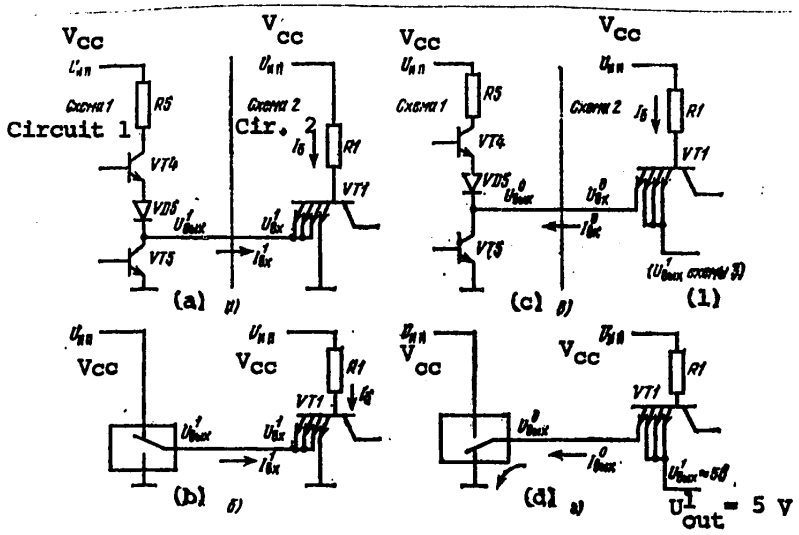


Figure 3.12. Combined operation of a TTL signal source and load.

Key: a,c. Circuit 1 generates "1" and "0" respectively;
b,d. The equivalent circuits for these operating modes;
1. U^1_{out} for circuit 3.

circuit to actuate, since U'_{thr} = 0.8 volts) and the oscillatory process at the input decays rapidly.

We shall analyze the output characteristics of the NAND logic gate shown in Figure 3.5a. The output characteristics are shown in Figure 3.13a for the logic gate at various temperatures. With an increase in the load current, I'_{out}, the output voltage level will fall off until a certain value of the current is reached, $I'_{out} \approx$ $\approx$5 mA, when the voltage drop across resistor R5 is small. In this case, one can assume that transistor VT4 operates as an emitter follower, and the slope of the characteristic $U'_{out} = f(I'_{out})$ is small. With a further increase in the current, I'_{out}, the voltage drop across resistor R5 increases, the voltage at the collector of transistor VT4 becomes less than at the base and transistor VT4 goes into saturation. The characteristic curve changes its slope and then the current falls off linearly. The rate of drop is now determined by the nominal value of resistor R5. It can be seen from Figure 3.13a that although the slope of the characteristic is practically independent of the temperature, nonetheless at a temperature of -60°C the current level decreases by approximately 0.5 mA, something which causes a reduction in the fan-out capacity of the circuit.

The output characteristics of a logic gate in the "0" state are also shown in Figure 3.13a for various temperatures. As can be seen from Figure 3.13a, the slope of the characteristic $U^0_{out}(I^0_{out})$ changes with a change in temperature.

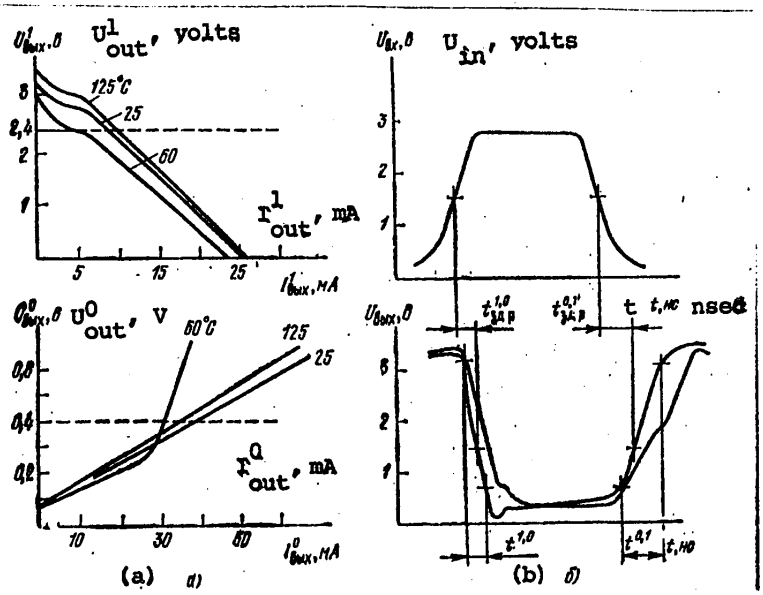


Figure 3.13. The output (a) and dynamic (b) characteristic curves for a standard series TTL NAND gate.
Key: 1. "1,0" propagation delay time;
2. "0,1" propagation delay time.

At a temperature of -60 °C, when the output current I^0_{out} reaches a value of 25 mA, the slope of the characteristic increases sharply and subsequently, even a slight increase in I^0_{out} leads to a substantial rise in the voltage at the circuit output. Thus, the lower temperatures are more critical from the viewpoint of the load fan-out capacity of TTL circuits.

We shall consider the operation of a NAND gate in the dynamic mode. As has already been stated above, the circuit speed is characterized by several parameters, and in particular, the propagation delay time when switching the circuit on and off, ($t^{1,0}_{zd.r}$) and ($t^{0,1}_{zd.r}$) respectively (Figure 3.13b).

When switching a NAND logic gate (Figure 3.14), the fraction of the propagation delay time due to transistor VT1 may be disregarded, assuming that the switch actuates instantaneously. Then, the overall signal propagation delay in the circuit will be governed by the delay due to transistors VT2 and VT4:

$$t^{1,0}_{зд\,р} = t^{1,0}_{зд\,VT2} + t^{1,0}_{зд\,VT4}.$$

In turn, the delay due to transistor VT2 is primarily governed by the parasitic capacitance charging time for $C_{\Sigma 1}$, which takes the form of the sum of the parasitic capacitances of resistor R1 of the collector of transistor VT1 to the substrate and to the b-e junction of transitor VT1. The delay due to transistor VT4 is determined by the charging time for the parasitic capacitance $C_{\Sigma 2}$, which takes the form of the sum of the capacitances of the structure of resistor R4 and the b-e junction of transistor VT4.

When the gate is switched off, the signal propagation delay for the NAND logic gate, $t^{0,1}_{zd.r}$, is determined primarily by the resorption time for the minority carriers in the bases of transistors VT2 and VT4. For standard TTL circuits at a temperature of 25 °C, where K_{out} = 10 and C_n = 15 pFd, typical values of the propagation delay time during turn-on and turn-off are $t^{1,0}_{zd.r}$ = 7 nsec and $t^{0,1}_{zd.r}$ = = 13 nsec respectively.

It can be seen from the curves shown in Figure 3.15 that with a rise in temperature, the propagation delay time during turn-on falls off slightly while the propagation delay time in the case of cut-off, on the other hand, increases, especially in a temperature range of from 20 to 120 °C. With an increase in the load, the values of the propagation delay increase somewhat and an increase in the load capacitance has a greater influence than an increase in the number of IC inputs connected to the output of the TTL switch.

As has already been stated, various types of flip-flops and circuits designed around them - registers, counters, adders - are incorporated in a series of digital IC's along with simple logic elements.

As an example of a standard TTL series, we shall treat the operational principle of JK and D flip-flops. The schematic of a JK flip-flop is shown in Figure 3.16. As can be seen from Figure 3.16b, the entire device consists of the main flip-flop T1 and the auxiliary flip-flop T2. The information is entered in the main flip-flop at the moment of arrival of the positive edge of the synchronization pulse which is fed to input C. During the action of the sync pulse in the upper auxiliary flip-flop, the data entered during the preceding cycle is preserved. Upon the completion of the synchronization pulse, the data is rewritten from the main flip-flop into the auxiliary one.

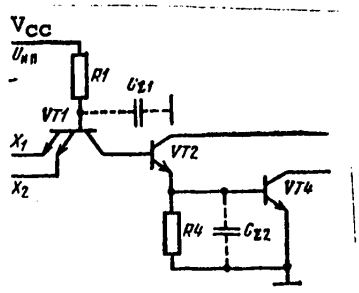


Figure 3.14. The equivalent circuit for the generation of dynamic parameters.

Three operational variants are possible for this two-stage flip-flop. In the first case, a signal corresponding to "1" is fed to the information inputs J and K while a sync pulse is fed to input C. The JK flip-flop then operates as a divide-by-two circuit (i.e., as a counter). This mode is utilized in the construction of frequency dividers and counters of any degree of complexity. In the second mode, a paraphase logic signal is fed to information inputs J and K. The flip-flop then operates in a synchronous information write mode from the J and K inputs.

Following the input of the clock pulse, this information appears at the Q and $\overline{Q}$ outputs, i.e, it is shifted to the next location. The given mode is utilized in the construction of shift registers, pulse distributors and synchronous counters. And finally, information in the form of the "0" level is fed to the R or S inputs. In this case, the flip-flop is

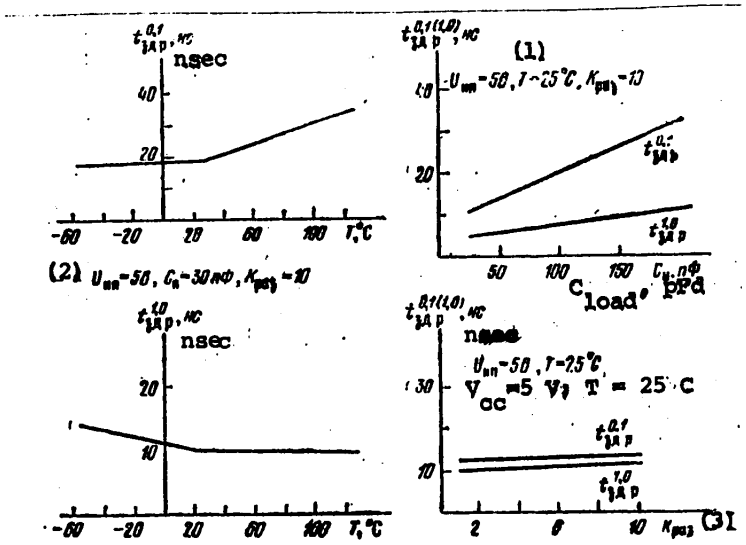


Figure 3.15. The propagation delay times of standard TTL circuits as a function of temperature, capacitance and the number of similar IC inputs connected at the output.

Key: 1. V_{cc} = 5 volts, T = 25 °C and K_{out} = 10;
2. V_{cc} = 5 volts, C_{load} = 30 pFd and K_{out} = 10;
3. K_{out}[fan-out load factor].

forcibly set in the "0" or "1" state (the states of the J, K and C inputs are arbitrary). One must take into account the fact that the state when the signal corresponding to the "0" level is simultaneously fed to the R and S inputs is indeterminate. The possibility of the occurrence of such a state should be precluded.

The circuit of D flip-flop (Figure 3.17b) consists of the main asynchronous RS flip-flop T3, the auxiliary synchronous RS flip-flop T1 which is used for writing "1" into the main flip-flop, as well as the auxiliary synchronous RS flip-flop T2 for writing "0" into the main flip-flop.

The information write into flip-flops T1 and T2 takes place at the point in time t only with the apperance of the positive edge of the synchronization pulse which is fed to the count input C. At the point in time t+1 (with the next clock pulse), the information appears at the output of the D flip-flop. Thus, a D flip-flop generates a "1" of output information at the moment of arrival of a positive synchronization pulse gradient, if a "1" was present beforehand at the *D* input. When a signal is not present at the count input C, the flip-flop maintains its previous state. A D flip-flop performs the function of a count flip-flop if the inverted out $\overline{Q}$ is connected to the *D* input. In the asynchornous mode, a D

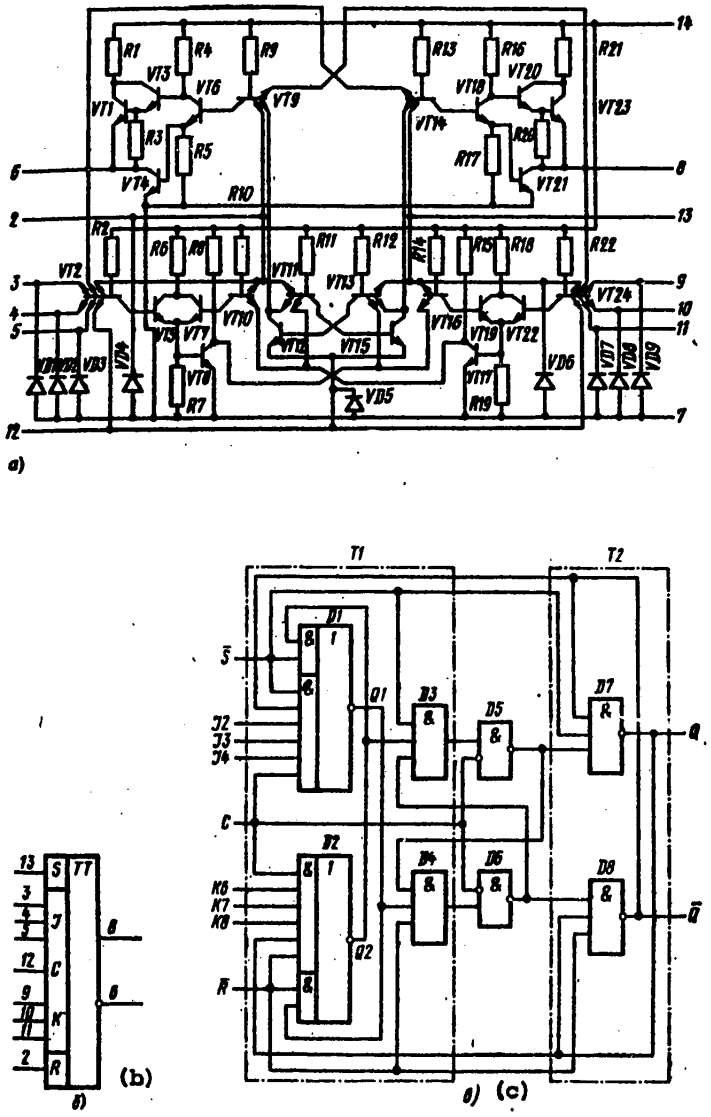


Figure 3.16. Schematics of a K155TV1 JK flip-flop with 3AND logic at the input; the basic electrical circuit (a), electrical block diagram (b) and its logic structure (c).

flip-flop operates in a manner similar to that of an RS flip-flop (the states of *D* and C inputs are arbitrary).

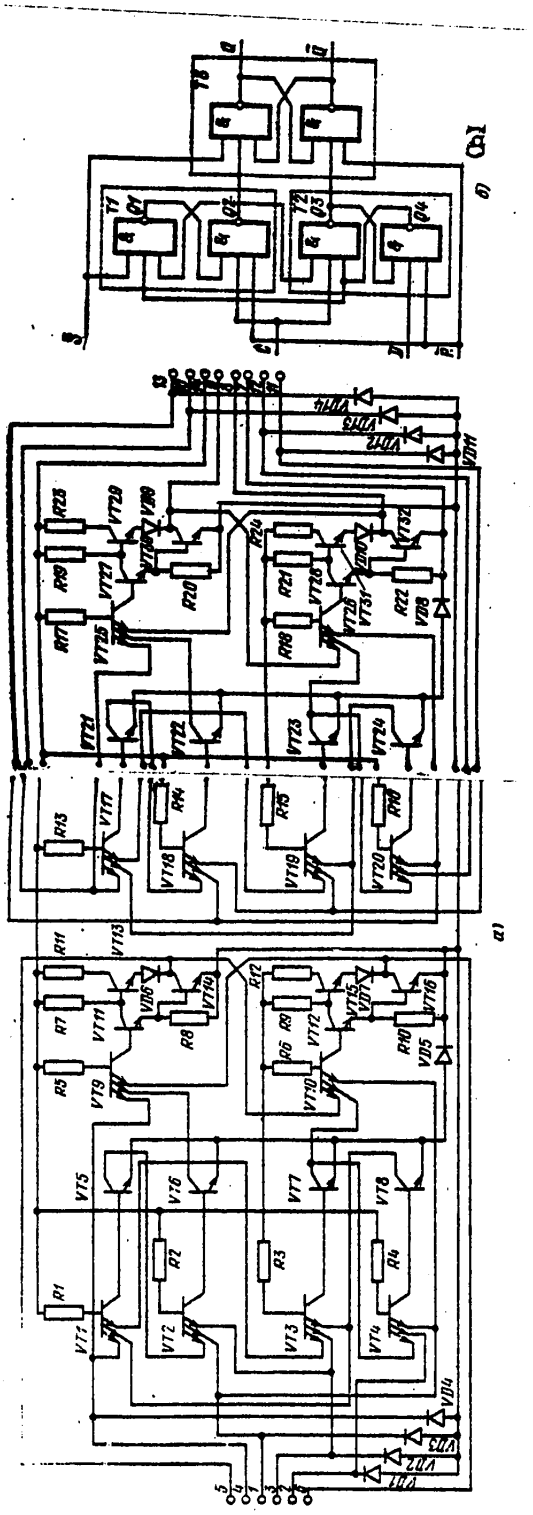


Figure 3.17. The basic electrical schematic of a K155TM2 D-flip-flop (a) and its logic structure (b).

The integrated circuits of the high speed TTL series, an example of which can be the 130 series, make it possible to obtain a typical propagation delay time of 7 nsec with a power consumption per elementary switch of 44 mW. The basic circuits of this series (Figure 3.6) differ from the basic circuits of the standard series (Figure 3.5) in the reduced nominal values of the resistors and lower parasitic capacitances of the elements. Since the output current of an ultrafast TTL switch is increased, a Darlington configuration (transistors VT3 and VT5) is used in the output stage, which makes it possible to boost the current gain of the output transistor and thereby assure approximately equal values of the output impedances of the circuit when it is switched on (governed by the top emitter follower VT5) and switched off (governed by the saturation of transistor VT6) which yields almost symmetrical values of the signal propagation delay.

The low output and input impedances of TTL circuits provides small time constants for the parasitic load capacitances of the printed board conductors, which makes it possible for this series of IC's to operate at clock frequencies of up to 30 MHz.

Micropower series IC's, an example of which is the 134 series, make it possible to obtain an average value of the power consumption of 2 mW for a TTL switch at a temperature of 25 °C. The basic circuits of this series (Figure 3.7) differ from the basic circuits of the standard series in the absence of damping diodes and a correcting network, as well as in the significantly increased nominal values of the resistors. The latter is responsible for the low current and power consumption levels with the concurrent decrease in circuit speed. The turn-on and turn-off delay time for a micropower series TTL switch amounts to 100 nsec.

IC series with Schottky diodes, an example of which is the 530 series, differ from the TTL series treated above in the use of diodes and transistors in which the Schottky effect is used. The 530 series circuits make it possible at a temperature of 25 $\pm$ 10 °C and a load resistance of R_{load} = 280 ohms and load capacitance of C_{load} = 15 pFd to obtain typical values of the propagation delay time of 5 nsec per switch with an average power consumption of 19 mW (cf. the parameters of the 130 series). The basic schematic of the 530 series gate is shown in Figure 3.8.

The increase in the speed is obtained here through a reduction in the level of saturation of the transistors, which is accomplished through the use of Schottky diodes which shunt the collector-base junction of the saturated transistor. Schottky diodes, formed by the contact between a metal and a semiconductor, have a substantially lower threshold turn-on voltage then the c-b junction, and for this reason, during the action of the pulse, the Schottky diodes turn on earlier than the collector-base junction, thereby preventing the storage of excess charges in the base region of the transistors. Charge accumulation does not take place in the Schottky diodes themselves since the current flowing in them is due to majority carrier transport.

The operation of Schottky transistors in the unsaturated range leads in turn to an increase in the voltage drop across their base-emitter junction, which reduces the current consumption in the static mode and correspondingly, the power consumption. A Darlington circuit is used in the output stage (VT3 and VT5), which makes it possible when switching the circuit off to assure an elevated charging

current for the capacitive load, something which reduces the delay time for the leading edge of the output signal. By virtue of the small voltage drop across the b-e junction of transistor VT3, as well as the low output impedance of the circuit in both logic states, the Darlington configuration makes it possible to obtain a higher output voltage level U^1_{out} in these series. We shall analyze TTL integrated circuits in more detail.

3.4.1. The Major Electrical Parameters of TTL Integrated Circuits

As was shown in §3.2, the following number among the main electrical parameters which rather completely characterize all TTL circuits and make it possible to compare them with each other: speed, power consumption, load capacity, noise immunity and input fan-in factor. Also to be included among these parameters is the value of the logic levels, since they determine the possibility of joint operation of integrated circuits of different series. It is important to know these levels when interfacing TTL integrated circuit signals with other digital and analog circuit signals. All of the TTL series treated above have the same power supply voltage, V_{cc} = 5 V ± 10% and similar values of the logic levels, something which makes it possible to directly couple integrated circuits from various TTL series, and also permits the connection to DTL integrated circuits.

The direct electrical compatibility makes it possible to reduce the number of power supplies and precludes the necessity of designing special level matching circuits. The major operational electrical parameters of various TTL series are compared in Table 3.8. All of the parameters are given for the basic circuits. They make it possible to trace the specific features of each series, evaluate their advantages and drawbacks and give an overall idea when selecting a series during the equipment development stage. It should also be noted that the parameters given in Table 3.8 apply to the total working temperature range.

When designing equipment, one must also take into account the ultimate permissible operational modes of the IC's, exceeding which can lead to IC failure. The ultimate permissible operating modes for various TTL series are compared in Table 3.9. One must keep in mind the fact that when utilizing the modes indicated in Table 3.9, the values of the electrical parameters can differ from those indicated in Table 3.8.

3.4.2. The Functional Complement of the TTL Series

Digital TTL integrated circuits became the basis for the construction of computer hardware in the 1970's. One of the decisive advantages of TTL series is the presence of such circuits as JK and D flip-flops, decoders, shift registers, counters, adders, main memory elements and ROM's with control circuits. The availability of circuits which take the form of ready-made computer assemblies which immediately include several bits makes it possible to significantly reduce the number of digital IC packages and obtain a substantial savings in equipment volume. Thus, for example, the K155, K131 and K158 series TTL IC's found widespread applications in the "Ryad" unified system of electronic computers: the

TABLE 3.8 Electrical Parameters of Various Series of TTL Integrated Circuits

Parameter	Series						
	Standard		High Speed		Micropower	With Shottky Diodes	
	133	K155	130	K131	134	530	K531
The input "0" current, I^0_{in}, mA, no more than	-1.6	-1.6	-2.3	-2.3	-0.18	-2	-2
The "1" input current, I^1_{in}, mA, no more than	0.04	0.04	0.07	0.07	0.012	0.05	0.05
The "0" output voltage, U^0_{out}, volts, no more than	0.4	0.4	0.35	0.35	0.3	0.5	0.5
The "1" output voltage, U^1_{out}, volts, no less than	2.4	2.4	2.4	2.4	2.3	2.7	2.7
Output fan-out factor, K_{out}	10	10	10	10	10	10	10
The OR input fan-in factor, K_{in}	8	8	8	8	2	-	-
Turn-on propagation delay time, $t^{1,0}_{zd,r}$, nsec, no more than	15 (C_l = = 15 pF)	15 (C_l = = 15 pF)	10 (C_l = = 30 pF)	10 (C_l = = 30 pF)	100 (C_l = = 40 pF)	5 (C_l = = 15 pF)	5 (C_l = = 15 pF)
Turn-off propagation time, $t^{0,1}_{zd,r}$, nsec, no more than	22 (C_l = = 15 pF)	22 (C_l = = 15 pF)	10 (C_l = = 30 pF)	10 (C_l = = 30 pF)	100 (C_l = = 40 pF)	4.5 (C_l = = 15 pF)	4.5 (C_l = = 15 pF)
Average static power consumption, P_{con}, mW, no more than	22	22	44	44	2	19	19
Noise immunity, U^*_n, volts, no more than	0.4	0.4	0.4	0.4	0.35	0.5	0.5
Switching frequency, f, in MHz, no more than	10	10	30	30	3	50	50

*The lowest of the two values of the permissible interference level U^0_n and U^1_n are given in the Table.

TABLE 3.9 Ultimate Permissible Operating Modes for Various Series of TTL Integrated Circuits

Mode Parameter	Series						
	Standard		High Speed		Micropower	With Schottky Diodes	
Maximum supply voltage, V_{cc}, volts	6	6	6	6	6	5.5	6
Maximum voltage at the input, $U_{in\ max}$, volts	5.5	5.5	5.5	5.5	5.5	5.0	5.0
Maximum voltage applied to the output of a cut-off circuit, U_{out}, volts	5.5	5.25	5.5	5.25	5.5	5.5	5.25
Minimal input voltage, $U_{in\ min}$, volts	-0.4	-0.4	-0.4	-0.4	-1.56	-0.4	-0.4
Maximum load capacitance, C_{load}, pFd	200	200	200	200	200	150	200

YeS EVM. The functional composition of standard, high speed, and micropower series as well as series with Schottky diodes developed in recent years is given in Table 3.10. The functional analogs of these integrated circuits are also indicated there. The complete symbol for TTL integrated circuit series is formed from the number of the series and the designation indicated in the "subgroup, kind ..." column, for example, 133LA3. The complete designation of the functional analog is formed from the designation of the series (SN54 or SN74H) and the number given in the "Designation of the Functional Analog" column, for example, type SN5420 or SN74H50 integrated circuits.

3.4.3. Some Specific Features of TTL Integrated Circuit Applications

In the structural design of equipment using IC's, their structural packaging is of considerable importance (Table 3.11).

The specific features of TTL IC's, in particular, the use of a complex inverter in the output stage increases the current consumption during switching. This boosts

TABLE 3.10 The Composition of the TTL Series and Their Functional Analogs in the SN 554/74 Series

Functional Designation [1]	Subgroup, Kind and Ordinal Number of the Design (with Respect to Function [2]	Designation of the Functional Analog [3]	Number of the Outline Drawing in Appendix 3.1 [4]
Four 2AND-NOT logic gates (133, K155, 130, K131, 530, K531, K555)	LA3	00	3.1.5
Three 3NAND logic gates (133, K155, 130, K131, 530, K531, K55)	LA4	10	3.1.6
Two 4NAND logic gates (133, K155, 130, K131, 530, K531, K555)	LA1	20	3.1.1a[1]
8NAND logic gate (133, K155, L30, K131, 134, 530, K555)	LA2	30	3.1.2
Two 4NAND logic gates with a large fan-out factor (133, K155, 130, K131)	LA6	40	3.1.7
Two 2AND-2OR-NOT logic gates, one OR expandable (133, K155, 130, K131, 134, 734)	LR1	50	3.1.3
Two 4-input OR logic expanders (133, K155, 130, K131)	LD1	60	3.1.4
Four 2NAND/2NOR logic gates (134, 734)	LB1	-	3.1.52
Two 4NAND/4NOR logic gates and a NOT logic gate (134, 734)	LB2	-	3.1.53
2-2-3-4AND-4NOR logic gates (134, 734)	LR2	-	3.1.54
Four 2-input NAND gates with an open collector output (test elements), 133, K155, 134 [sic]	LA8	01	3.1.12
Four 2NAND logic gates with an open collector output (K531, K555)	LA9P[2]	03	-
Six NOT logic gates (K155, 130, K131, K531, K555)	LN1	04	3.1.39
Four 2NOR logic gates (133, K155, K531, K555)	LYe1P	02	-
Six NOT logic gates (with open collector) (K531)	LN2P	05	-

[Table 3.10, continued]:

1	2	3	4
Six buffer inverters with elevated collector voltage (K155)	LN3	06	-
Six buffer drivers with open collector (K155)	LN4	07	-
Four 2AND logic gates (133, K155, K555)	LI1	08	3.1.22
Three 3AND logic gates (530, K531)	LI3P	11	-
Three 3NAND logic gates (with open collector) (K155)	LA10	12	-
Two Schmitt triggers with a logic gate at the input (133, K155)	TL1	13	-
Six NOT buffer elements (K155)	LN5	16	-
Two 4AND logic gates	LI6	21	-
Two NOR logic gates with gating in one gate and an OR expansion capability in the other (K155)	LYe2	23	-
Two 4-input NAND gates with open collector output and increased load capacity (display elements) (133, K155)	LA7	22	3.1.11
Two gated 4NOR logic gates (K155)	LYe3	25	-
Four high voltage 2NAND logic gates with open collector (K155)	LA11	26	-
Four 2NOR logic gates (buffer unit) (k155)	LYe5	28	-
MOS memory to TTL interface for four 2NAND logic gates (133)	LA15	-	3.1.30
Four 2OR logic gates (133, K155, K555)	LL1	32	-
Four 2NAND buffer logic gates (K155)	LA12	37	-
Four 2NAND buffer logic gates with open collector output (K155)	LA13	38	-
Two 4-2-3-2AND-4NOR logic gates (530, K531, K555)	LR11P	51	-
2-2-3AND-4NOR with OR expander capability (133, K155, 130, K131)	LR3	54	3.1.8
4-4AND-2NOR logic gate with OR expander capability (133, K155, 130, K131, 134)	LR4	55	3.1.10

1	2	3	4
4 x 10 decoder (134)	ID6	42	3.1.49
4-2-3-2AND-4NOR logic gate (530, K531)	LR9P	64	-
Binary code digital input signal to seven segment code digital signal converters (133)	PP4	49	3.1.31
Four D flip-flop with direct and inverting outputs (133, K155)	TM7	75	3.1.19
Four D flip-flops (133, K155)	TM5	77	3.1.18
Single digit full adder (133, K155)	IM1	80	3.1.35
16 bit main memory with control circuits (133, K155)	RU1	81	3.1.21
Two bit (binary) full adder (133, K155)	IM2	82	3.1.36
Four bit (binary) adder (133, K155)	IM3	83	3.1.37
16 bit main memory with gate input for the write amplifier (K155)	RU3	84	3.1.33
Four bit number comparison gate (134)	SP1	85	-
Four 2-input "exclusive OR logic gates (K155)	LP5	86	3.1.47
Binary JK flip-flop (134)	TV14	78	3.1.55
64 bit main memory random access memory (133, K155)	RU2	89	3.1.34
8 bit shift register (134)	IR2	91	3.1.48
Counter--divide-by-12 (133, K155)	IYe4	92	3.1.16
Binary counter (133, K155, 134)	IYe5	93	3.1.17, a[3]
4-bit universal shift register (133, K155, 134)	IR1	95	3.1.20, a[4]
Two D flip-flop (133, K155, 130, 134)	TM2	74	3.1.14
Binary-decimal 4-bit counter (133, K155, 134)	IYe2	90	3.1.15, a[5]
JK flip-flop with logic at the 3AND input (133, K155, 130, K131, 134)	TV1	72	3.1.13, a[6]
Frequency divider with variable division factor (133, K155)	IYe8	97	3.1.32
Four bit selective register (134)	IR5	98	-
Two JK flip-flops (K531)	TV9P	112	-

1	2	3	4
Two JK flip-flops (K531)	TV10P	113	-
Dual JK flip-flop (K531)	TV11P	114	-
Four buffer gates with three output states (K155)	LP8	125	-
Four 2NOR logic gates (trunk amplifier) (K155)	LYe6	128	-
Binary decoder for eight directions (K555)	ID7	138	-
Two 4NAND logic gates (trunk amplifier) (K531)	LA16P	140	-
High voltage decoder for controlling gas discharge displays (133, K155)	ID1	141	3.3.27
Gated eight channel selector-multiplexor (133, K155)	KP7	151	3.1.26
Eight channel data selector-multiplexer (133, K155)	KP5	152	3.1.25
A dual 4-1 digital selector-multiplexer (133, K155, 530, K531)	KP2	153	3.1.41
Gated 16 channel data selector-multiplexer (155)	KP1	150	3.1.40
16 to 4 line decoder-demultiplexer (133, K155, 134)	ID3	154	3.1.44
Dual 2--4 decoder-multiplexer (K155)	ID4	155	3.1.46
Multifunction logic gate for computers (K155)	KhL1	-	3.1.38
One-shot multivibrator with a logic gate at the input (133, K155)	AG1	121	-
Synchronous decimal four-bit counter (K155)	IYe9	160	-
Eight bit series shift register with a parallel output (134)	IR8	164	-
16 bit register memory (K155)	RP1	170	-
Four bit register with three output states (K155)	IR15	173	-
Quad D flip-flop (K155)	TM8	175	-
Eight bit parity and nonparity checker (K155, 134)	IP2	180	3.1.42

1	2	3	4
Arithmetic logic unit (K155, 134)	KP3	181	3.1.45, a[7]
Fast carry circuits for an arithmetic logic unit (K155, 134)	IP4	182	3.1.43
Dual accelerated carry full adder (134)	IM5	183	3.1.50
Decade counter with pulse-phase data representation (K155)	IYe1	-	3.1.23
Bit write driver, playback amplifier and zero set circuit (K155)	AP1	-	3.1.24
Eight input OR expander (133, K155)	LD3	-	3.1.9
Binary-decimal code to binary converter (K155)	PR6	184	-
Binary code to binary-decimal converter (K155)	PR7	185	-
1,024 bit ROM used as a binary code to Russian, Latin alphabet code converter as well as arithmetic codes and supplmental characteristics	RYe21... RYe24	187	-
256 bit ROM with control circuits (K155)	RYe3	-	-
Binary-decimal bidirectional counter (133, K155)	IYe6	192	3.1.28
Four bit binary bidirectional counter (133, K155)	IYe7	193	3.1.29
Four storage elements (134)	RM1	-	3.1.51
Majority gate (134)	LP3	-	3.1.56
Multipurpose digital structure gate (METsS) (134)	KhL3	-	3.1.58
Multipurpose digital structure gate (METsS-2) (134)	KhL2	-	3.1.57
Three switch circuits (134)	KP8	-	3.1.59
Dual four channels into one switcher (134)	KP9	-	3.1.60
Eight channel switcher (134)	KP10	-	3.1.61
Four bit half-adder (134)	IM4	-	3.1.62
Two 2NAND logic gates with a common input and two power transistors (K155)	LP7	SN75450	-

[Table 3.10, continued]:

1	2	3	4
Two 2AND logic gates with a high power open collector output (K155)	LI5	SN75451	-
12 bit sequential approximation register (133)	IR17	AT2504	-
Bidirectional eight bit shift register (133, K155)	IR13	198	-

Note: The 133 series IC's are the functional analog of the SN54 IC series; the K155 series are analogous to the SN74; the 130 series are analogous to the SN54H; the K131 series to the SN74H; the K531 series to the SN74S; the 530 series to the SN54S; the K555 series to the SN74LS.

1. See Figure 3.1.1b for the K155LA1 integrated circuit.
2. The letter P" applies only to the K531 series and means that is produced in a plastic package.
3. See Figure 3.1.17b for the 134YeI5 integrated circuit.
4. See Figure 3.1.20b for the 134IR1 integrated circuit.
5. See Figure 3.1.15b for the 134IYe2 integrated circuit.
6. See Figure 3.1.13b for the 134TV1 integrated circuit.
7. See Figure 3.1.45b for the 134IP3 integrated circuit.

the dynamic power consumption with an increase in the switching frequency and limits the rise and fall time of the input pulses to 150 nsec (with the exception of circuits having an open collector output, for which this time is not limited).

When wiring equipment, to increase the operational stability of TTL circuits their free inputs must be connected to a 5 V $\pm$ 10 % power supply through a 1 KOhm resistor or directly to a 4 V $\pm$ 10 % supply. The connection of 20 free inputs to each resistor is permitted.

Considerable attention in the wiring of equipment is to be devoted to assuring integrated circuit noise immunity. As was indicated above (Table 3.8), the permissible static noise level for the majority of TTL gates amount to 0.4 volts (in the full range of working temperatures). However in coupling lines and in logic circuits, composed of a number of IC's working into each other, pulse interference can occur. The permissible pulse interference level depends on the pulse width. It can be seen from a graph of the function $U^{n}(\tau_{p\ n})$ for type 155LA3 integrated circuits (Figure 3.18) that for a pulse width of 15 nsec, the permissible pulse interference level can reach two volts. Pulse noise immunity is

practically independent of the supply voltage, and does depend on the number of loads, K_{out}, and the OR fan-in factor, K_{in}. The worst case is when a gate having a value of $K_{out} = 10$ and $K_{in} = 1$, and a gate with $K_{out} = 1$ and $K_{in} = 8$ alternate in the logic circuit. Such circuits are the most sensitive to pulse interference.

TABLE 3.11 Types of Rectangular TTL Series Packages

Series	Kind of Package	Conventional Designation	Series	Kind of Package	Conventional Designation
133	Metal-glass	401.14-4	134	Glass	401.14-3
	Glass	401.14-3		Metal-glass	401.14-5
	Metal-glass	401.14-2		"	401.14-4
	"	402.16-1		"	402.14-1
	"	402.16-2		Metal-ceramic	402.16-2
	"	405.24-1		"	405.24-2
				"	402.16-3
K155	Plastic	201.14-1		"	405.24-1
	"	201.14-2		"	402.16-1
	"	239.24-1		"	402.16-11
	"	239.24-2			
	"	238.16-1	530	Metal-glass	401.14-4
	"	238.16-2		"	401.14-5
13	Metal-galss	401.14-4	K531	Plastic	201.16-12
	Glass	401.14-3		"	201.14-1
				"	238.16-2
K1313	Plastic	201.14-1			

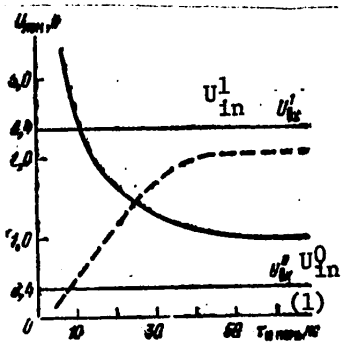


Figure 3.18. The permissible dynamic interference as a function of its pulse width. The solid curve is for positive interence at T = = 125 °C; the dashed curve is for negative interference when T = -60 °C.

Key: 1. $\tau_{pulse\ int.}$, nsec.

In order to prevent low frequency interference when IC's are mounted on printed circuit boards, it is necessary to provide for the installation of decoupling capacitors close to the connector based on a design figure of no less than 0.1 μFd per IC. To prevent high frequency interference, it is recommended that the isolating capacitors (not less than 0.002 μFd per IC) be located on the printed circuit board based on a design figure of one capacity per group of no more than 10 IC's.

To increase the noise immunity of assemblies and modules designed around rather high speed integrated

circuits, among which practically all TTL series may be included, attention is to be devoted to the wring layout for the power supply. When using multilayer printed circuit boards, it is recommended that the "power" buses be arranged in one layer, while the "ground" buses are placed in another adjacent layer and the buses are arranged one under the other. When free area is available in a layer, it is used to increase the surface of the "ground" bus.

TABLE 3.12 The Maximum Permissible Length of Printed Circuit Conductors on Circuit Boards with 155 Series IC's

(1) Число параллельных проводников	(2) Интервалы между печатными проводниками, мм				
	0,5	1,0	1,5	3,0	5,0
2	100	120	130	150	170
3	60	70	75	90	100
4	50	60	65	70	80
5	40	50	60	65	70

Key: 1. Number of parallel conductors;
2. Spacings between the printed circuit conductors, mm.

We shall discuss the recommended rules for the execution of the electrical connecting lines between IC packages on a printed circuit board using the example of the K155 series. The electrical connecting lines are intended for transmitting the information, synchronization, display and switching signals, and as was noted above, also as the "power" and "ground" buses. The information carrying lines are made in the form of printed circuit tracks within the bounds of the printed circuit board. In this case, it is essential that the conductors which are arranged on different sides of the circuit board or in adjacent layers intersect at angles of 45 to 90°. The maximum permissible length of parallel conductors arranged on the same side of a circuit board or in the same layer (where the printed circuit conductor width is 0.5 to 1.5 mm), should not exceed the values indicated in Table 3.12. In this case, one must keep in mind the fact that the length of printed circuit conductors which do not go beyond the bounds of the printed circuit board can be increased by 40% relative to the values shown in Table 3.12.

The information coupling lines between the circuit boards can be made by means of a special hook-up panel (cross field), made in the form of a printed circuit board. The length of the connecting lines on the hook-up panel are determined as the sum of the values of the length obtained from Table 3.12 and the connecting lengths on the printed circuit hook-up panel. If the length of the information connecting lines exceeds 20 cm, it is recommended that they be made by means of three--dimensional wiring. Where the coupling line length runs up to 20 cm for asynchronous devices and up to 30 cm for synchronous devices, they are made with a single wire. It is permissible to connect up to five radial lines l_i with an

overall length of no more than 50 cm to the output of one transmitting element. On panels with lengths of from 0.2 to 1 m, the connecting lines should be made as unmatched twisted pairs. No more than three twisted pairs with an overall length of no more than 2 m may be connected to the output of one transmitting element. It must be kept in mind that when making connections using unmatched twisted pairs, the the signal propagation delay time increases in proportion to the length of such a line. At the output of a transmitting element, the increase in the propagation delay during turn-on, $\Delta t^{1,0}_{zd.r} = 6l_\Sigma$, and during cut-off, $\Delta t^{0,1}_{zd.r} = 8l_\Sigma$, where l_Σ is the total length of the connecting lines which are connected to the output of the transmitting element. (Here, $\Delta t^{0,1}_{zd.r}$ is obtained in nanoseconds if l_Σ is figured in meters).

At the output of a connecting line, l_i, the propagation delay increment is increased even more and amounts to:

$$\Delta t^{0,1}_{зд.р} = 8l_\Sigma + 5l_i,\ \Delta t^{1,0}_{зд.р} = 6l_\Sigma + 6l_i.$$

The return wires of the twisted pairs should be grounded at the transmitting and receiving ends. In this case, the length of a separate portion of a twisted pair should not exceed 3 cm. It is permissible to make taps with a single wire from an unmatched pair. The total length of the taps can run up to 20 cm.

Connecting lines of from 1 to 3 m, which do not go beyond the bounds of the digital device, should be made using matched twisted pairs. Where the length is more than 3 m, the coupling lines must be made using a coaxial cable with a characteristic impedance of 100 ohms. The connecting line is matched by means of an inserted series resistor of R = 82 ohms with a permissible resistance deviation of $\pm$5%. The resistor should be inserted directly at the output of the transmitting IC. The coaxial cable length should not exceed 30 m.

In the case of a matched connecting line, the increase in the propagation delay at the output of the transmitting element during turn-on is $\Delta t^{1,0}_{zd.r} = 6$ nsec, and during cut-off, $\Delta t^{0,1}_{zd.r} = 8$ nsec. At the output of the connecting line, the propagation delay increases in proportion ot the connecting line length l (in meters): $\Delta t^{1,0}_{zd.r} = 6 + 5l$; $\Delta t^{0,1}_{zd.r} = 8 + 5l$.

In contrast to the series matching treated above, it is also possible to work with a coaxial cable with parallel matching. In this case, the resistor having a value equal to the characteristic impedance of the cable is inserted "in parallel" at the end of the connecting line.

In the TTL series treated above, there is no circuit which provides for operation into a cable. A type 109LI1 DTL integrated circuit is used for this purpose, which takes the form of a six input AND logic gate, intended for driving a low impedance load as a trunk amplifier. This IC operates directly from the TTL IC and can be loaded in these circuits through a coaxial cable with a characteristic impedance of 75 ohms.

An example of the joint operation of 155LA3 and 109LI1 IC's through a cable with a characteristic impedance of 75 ohms for the case of series and parallel matching is shown in Figure 3.19. The pulse width at the output of the 109LI1 integrated circuit with parallel matching (Figure 3.19a) should be no less than 200 nsec, and in the case of series matching (Figure 3.19b), no less than 1 μsec. The maximum cable length is chosen so that the voltage drop in the cable does not exceed 50 mV.

The information signals can be transmitted by means of a shielded wire with the necessary transmission of the strobing signal via a coaxial cable. In this case, strobing signals should be delayed relative to the information signal by the amount of time necessary for the transient processes, while the width of the information signal pulses should be chosen from the condition:

$$t_{pul} > t_{zd.r.str} + t^{0,1\ (or\ 1,0)}$$

where $t_{zd.r.str}$ is the gating signal delay time relative to the information signal; $t^{0,1(or\ 1,0)}$ is the switching time of the circuit which receives the information.

In the case of printed circuit wiring, the coupling lines for the synchronization signals should be separated from the information lines and from the synchronization lines or another phase by a spacing of no less than 2.5 mm. It is recommended that the connecting lines from the outputs of IC's to display segments be made with single wires, which can be wrapped into a bundle. The length of a connecting line in this case is determined from the conditions necessary to meet the requirements of the technical specifications for the maximum permissible voltage applied at the IC output.

It is recommended that switched connecting lines (lines between toggle switches, relay contacts and integrated circuits) be made with shielded wire. It is permissible to use single conductors with lengths of up to 0.3 m and twisted pairs with lengths of up to 3 m.

The functional complement of the TTL series which has been expanded in recent years, especially the 155 and 134 series, because of the inclusion of counters, registers, adders and memory elements has significantly simplified the design of digital devices and made it possible to reduce the number of external wiring connections, which in the final analysis has led not only to a reduction in the volume of equipment which used IC's, but also to an improvement in its reliability.

However, besides the standard circuits which take the form of typical computer assemblies and modules, as well as digital automation hardware, for equipment design it is essential to have specialized circuits which provide for working into nonstandard loads such as relays, incandescent lamps, LED's and delay lines. Taking this into account, 133LA7, 155LA7, 133LA8 and K155LA8 IC's with open collectors were incorporated in the 133 and K155 series. The 133LA7 and 155LA7 integrated circuits are designed to operate as display amplifiers and made it possible to switch a current of up to 40 mA in the output circuit.

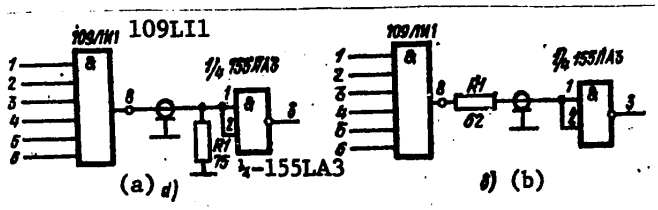


Figure 3.19. The coupling circuit for a coaxial cable in the case of parallel (a) and series (b) matching.

A schematic for a display using a type K155LA7 driving a NSM-6.3-20 incandescent lamp is shown in Figure 3.20a. A resistor with a nominal value of R_1 = 680 ohms limits the current through the output transistor, the level of which at the moment of turning the lamp on can reach 100 mA.

The 133LA8 and K155LA8 integrated circuits are designed for operation as test elements in computers and make it possible to realize the "wired OR" function with a large fan-out factor. A fan-out configuration for the 155LA8 integrated circuits is shown in Figure 3.20. The nominal value of resistor R1 is chosen as a function of the requisite output fan-out factor $K_{ob\ out}$ and number of logic gates connected to the combined output of the K155LA8 integrated circuit (K_{out}) in accordance with the formula:

$$R_1 = \frac{5}{I^0_{вых} - 1{,}6K'_{раз}} = \frac{5}{I^1_{вх} \cdot K'_{раз} + I^1_{ут} K_{об\ вых}}, \qquad (3.6)$$

where K'_{out} is the actual fan-out factor (taking into account the combined inputs of the logic gates which are the load); $K_{ob\ out}$ is the output fan-out factor, I^1_{yt} is the leakage current of the turned-off K155LA8 integrated circuit; I^0_{out} and I^1_{in} are the output current of the K155LA8 and input current of the K155LA3 [respectively], R_1 is the resistance of the resistor (the values of the currents are substituted in milliamperes, but the nominal value of R_1 is obtained in kilo-ohms).

The number of circuits which can be combined at the output is limited by the maximum permissible load capacity. When 134 series logic gates are connected as the load, the nominal value of resistor R1 calculated from formula (3.6) is to be doubled, and when 130 series logic gates are connected, it is to be cut in half. The 133LA7, K155LA7, 133LA8 and K155LA8 integrated circuits can also be used as NAND logic gates when their outputs are connected through an external resistor to a 5 volt + 5% power supply. In this mode, the turn on time, and especially the turn-off time for the input signal is not stipulated, in contrast to the other logic gates of the TTL series, for which this time is limited to a value of 150 nsec, as has laready been stated above.

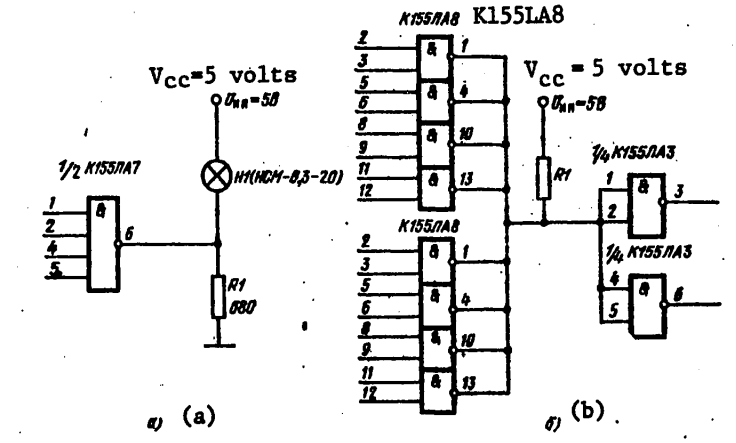


Figure 3.20. Display circuit based on K155LA7 integrated circuits (a) and the fan-out configuration for several K155LA8 integrated circuits (b).

3.5 Emitter Coupled Transistor Logic Circuits

Digital IC emitter-connected transistor logic circuits (ESTL) [ECL] are transistor switching circuits with connected emitters and, compared to other digital switches have the highest speed of operation and a high power consumption. High speed of operation (or to put it another way, a small average time of propagation delay) of ESTL is due to the fact that transistors in these keys operate in an unsaturated (linear) mode. Emitter followers that accelerate the process of charging the capacitance of the load are used at the circuit output. A reduction in the propagation delay time is also achieved due to the limitation of the output voltage gradient which, however, leads to a reduction in the interference rejection of the ESTL circuits. Of the digital IC ESTL developed in recent years, the most widely used are series 100 and K500 that are similar to a widely known MS10,000 series abroad (original developer -- the Motorola Co.).

We will consider the principle of designing the ESTL switch on an example of a basic series 100 logic element that implements simultaneously functions OR-NOT and OR (Fig. 3.21). The circuit consists of a differential amplifier assembled with VT1 and VT4 and VT5 transistors. When the signal gradient is applied to the input of this amplifier, current $I_э$ may flow either through transistor VT5 to whose base is constantly applied reference voltage $U_{оп}$ =-2.9 volts (during this time a negative blocking voltage is present at inputs X_1-X_4), or through transistors VT1-VT4, when a voltage greater than $U_{оп}$ is applied to their bases.

Output emitter repeaters (transistors VT7 and VT8 are connected to the bias level source $U_{см}$ =-2 volts ± 5% through external load resistors $R_{Н1}$ and $R_{Н2}$ with rated resistances of 51 ohms. The low output impedance of the circuits provides for the matching of the output and input levels of the logic elements when they are operating together and the possibility of feeding signals into a cable with 50 ohm wave impedance. The ESTL circuit is connected to a negative voltage power source $U_{ип}$=5.2 volts ± 5%. The collector circuits are grounded. Such a connec-

tion provides a lower dependence of the output voltage on inductions from the feed circuit and a better interference rejection. The value of the logic gradient for the ESTL is 0.69 millivolts, while the interference rejection reserve is -125 millivolts. Negative and logic levels of the ESTL circuits ($U^{1}_{вых}$ =0.96 volts, $U^{0}_{вых}$ =-1.65 volts) low in value, make it impossible to interface them directly with the TTL [Transistor-transistor logic] series circuits. The joint operation of TTL and ESTL circuits is implemented by special circuits of mutual level converters, entering the composition of all the above-indicated ESTL series.

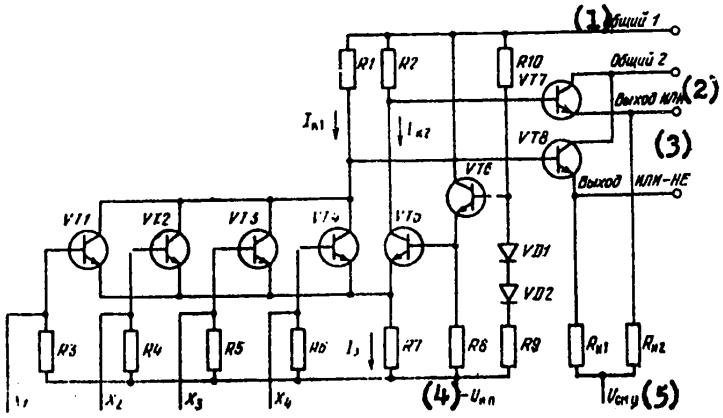


Fig. 3.21. Basic logic element OR-NOT/OR of the ESTL series

1. Common 1
2. OR output
3. OR-NOT output [NOR output]
4. $U_{ип}$ [supply, V_{cc}]
5. $U_{см\ у}$ [bias]

All inputs to the base logic element through leakage resistors R3...R6, with a resistance of about 50 kohms, are connected to power source $U_{ип}$ =-5.2 volts ± 5%. This connection makes it possible to leave the unused inputs in the apparatus unconnected. To eliminate the effect on the logic part of the circuit of pulse interferences originating in the collector circuits of the emitter repeater at

the moment of switching the circuit when operating with a low impedance load, two "ground" buses are used: one for output emitter repeaters and the other -- for the internal logic part of the circuit.

Reference voltage $U_{оп}$ =-2.09 volts is produced by a special temperature-compensated circuit (transistor VT6, diodes VD1, VD2, as well as resistors R8, R9, R10) and is selected so that it would be lower than minimum voltage 1. We will consider the principle of operation of the basic logic element (Fig. 3.21). If a low voltage level, corresponding to 0 ($U^0_{вх}$ =-1.85 volts), is applied to all inputs $X_1 \ldots X_4$, transistors VT1-VT4 are cut-off (only leakage currents are flowing) because their emitters have the following voltage applied:

$$U_э = U_{оп} + U_{б,VT6} = -1.29 + (-0.80) = -2.09 \text{ volts}$$

The level of current $I_э$ is determined by voltage $U_э$ and the rating of resistor R7. Current $I_э$ flows through open transistor VT5 to whose base is applied reference voltage $U_{оп}$, as well as resistors R7 and R2. A voltage drop U_{R2}=-0.98 volts is produced across resistor R2. The voltage at the OR output at this moment corresponds to level 0($U^0_{вых}$ =-1.65 volts), while at the output of OR-NOT, the voltage corresponds to 1 ($U^1_{вых}$ =-0.96 volts) (voltage $U_{отэ}$ of transistor VT7 should be added to the voltage drop across resistor R2).

When a high voltage level, i.e., 1 ($U^1_{вх}$ =-0.81 volts), is supplied to one of the inputs (or to all inputs $X_1 \ldots X_4$), the input transistor opens because the reference voltage selected was more negative than the minimal voltage 1. Transistor VT5 closes by the formed voltage gradient and all of current $I_э$ will flow through the opened input transistor (one of the VT1-VT4 row) and resistors R1 and R7. The negative voltage on the joined collectors of the input transistors will increase to level -.97 volts and a level, corresponding to 0, will be established at the output of the emitter repeater VT8, while 1 will be established at the output of emitter repeater VT7. Thus, the circuit produces logic function OR at the output of transistor VT7 and logic function OR-NOT at the output of transistor VT8. Thus, jumps in the input signal cause switching of current $I_э$ which, depending upon the value of the input signal, flows either through transistor VT5 or through transistors VT1-VT4. Because of this, the circuit with joined emitters is frequently called a current key. The paraphase outputs of the basic ESTL switch shorten the propagation path of the signals in digital devices. The presence of emitter repeaters that have low output impedance at the circuit outputs, provides a considerable load capacity of the ESTL circuits ($K_{раз} \geqslant 15$). To provide a still higher load capacity the ESTL digital series include special circuits with a high branching coefficient ($K_{раз}$ = 50...100 at $C_н$ > 100 picofarads).

An increase in the joining coefficient with respect to inputs may be achieved by connecting a logic expander to the basic circuit; however, this causes a considerable reduction in the speed of operation of the circuit due to parasitic capacitances; therefore, expander circuits are not included in the ESTL series [3]. We will now consider ESTL circuits in greater detail.

3.5.1. Functional Composition of the ESTL Series

In recent years technological successes made it possible to increase the functional possibilities of the ESTL series considerably. Along with logic elements and D triggers, decoding and multiplex circuits, memories and arithmetic device units were introduced into these series. This provides for their wide use in high speed computers. The functional composition of the ESTL digital series, developed in recent years, and their analogs are shown in Table 3.13.

We will consider in greater detail the purpose and special features of operation of several IC of series 100. IC types 100LM101, 100LM102, 100LM105, 100LM109 and 100LYe106 (and corresponding IC of series K500) implement functions OR-NOT and are designed with the basic logic element.

IC types 100LP115, 100LP116 are receivers from the line and may be used in two modes: as receivers of a paraphase signal from a two-wire communications line (in this case, the built-in leads in the housing of reference voltage source are not used) and as logic elements with constant voltages 0 or 1 at the output (with an external connection of the leadout from the reference voltage source with certain input leadouts. The use of both modes simultaneously for elements contained in the same IC housing is permitted.

IC type NR400 is a matrix of load resistors (four resistors rated at 500 ohms and four resistors rated at 800 ohms) which, with proper switching, are used as a load on the nonmatching inputs of the logic circuits of the series.

IC type 100TM130 (Fig. 3.22a) are two D triggers -- "latches," equipped with setting (S), resetting (R), synchronizing (C_E) inputs and a general synchronization input (C). Data is received from input D during the time when C=0; $\overline{C}_E$=0. In this case, any change in the data at input D is transmitted to the trigger output. The data is stored at the moment that the signal at input C changes from state 0 to state 1. For $\overline{C}_E$=1, the trigger is suppressed at input C. A forced setting of the trigger into state 1 (input S) and resetting (input R) is done when C=$\overline{C}_E$=1; in this case, the signal at input D does not affect the trigger. When the trigger is controlled by the R and S inputs, the setting and resetting pulses should not overlap in time.

IC type 100TM134 [Fig. 3.22b), unlike IC type 100 TM130, has two data inputs, D_1 and D_2 and an additional selector input S. When 1 is applied to input S, the data is recorded only by input D_1; when 0 is applied to input S, the data is recorded only by input D_2.

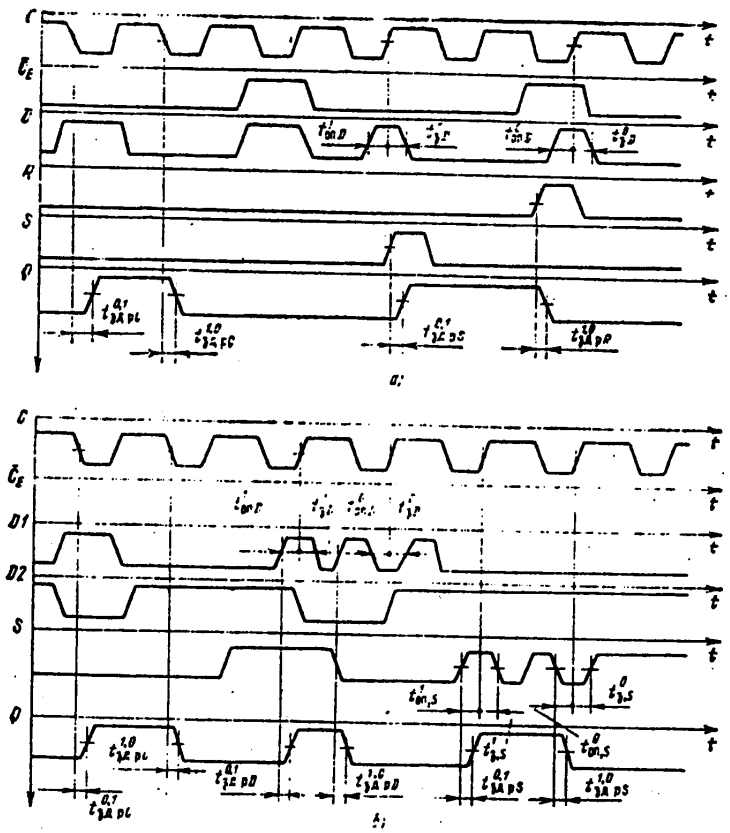


Fig. 3.22. Time diagrams of D trigger operation for IC type 100TM130 (a) and type 100TM134 (b).

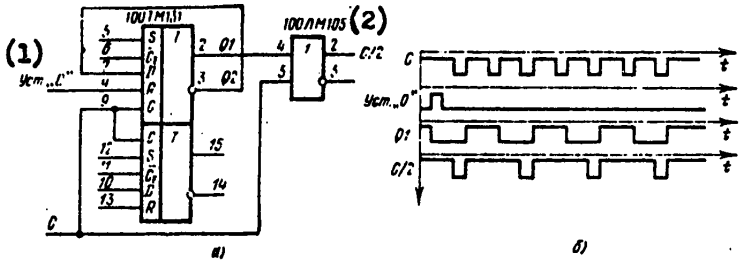


Fig. 3.23. Frequency divider for IC type 100TM131 (a) and its time diagram (b).

1. Zero setting
2. 100LM105

Table 3.13

Compositions of ESTL series and their functional analogs in the MS10000 series

Functional purpose	ESTL series		Analog	Variation without housing	No. of Figure in supplement 3.2
	100	K500	MS10000	700	
Four logic elements 2OR-NOT/2OR	100LM101	K500LM101 K500LM101T	MS10101	700LM101-2	3.2.1
Three logic elements 2 OR-NOT and logic element 2 OR-NOT/2 OR	100LM102	K500LM102 K500LM102T	MS10102	700LM102-2	3.2.2
Two logic elements 2 OR-NOT/2 OR and logic element 3 OR-NOT/3 OR	100LM105	K500LM105M K500LM105T	MS10105	700LM105-2	3.2.3
Two logic elements 3OR-NOT and logic element 4 OR-NOT	100LE106	K500LYe106T K500LYe106M	MS10106	700LYe106-2	3.2.4
Three logic elements "exclusion OR-NOT/OR"	100LP107	K500LP107 K500LP107M	MS10107	700P107-2	3.2.5
Two logic elements 5 OR-NOT/ 5OR, 4 OR-NOT/ 4 OR	100LM109	K500LM109 K500LM109M	MS10109	700LM109-2	3.2.6
Two logic elements 3OR with high power input	100LL110	K500LL110T K500LL110M	MS 10110	700LL110-2	3.2.7

Table 3.13 continued

Functional purpose	ESTL series 100	ESTL series K500	Analog MS10000	Variation without housing 700	No. of Figure in supplement 3.2
Two logic elements 3 OR-NOT with high power input	100LE111	K500LYe111T K500LYe111M	MS10111	700LYe1111-2	3.2.8
Four line receivers	100LP115	K500LP115 K500LP115T	MS10115	700LP115-2	3.2.9
Three line receivers	100LK116	K500LP116 K500LP116T	MS10116	700LP116-2	3.2.10
Two logic elements 2-3 OR-2 AND-NOT/3 OR-2 AND	100LK117	K500LK117 K500LK117M	MS10117	700Lk117-2	3.2.11
Resistor matrix	-	-	-	700NR1-2	-
Two logic elements 3-3 OR-2 AND	100LS118	K500LS118M	MS10118	700LS118-2	3.2.12
Logic element 3-3-3-4 OR- 4 AND	100LS119	K500LS119M	MS10119	700LS119-2	3.2.13
Two D triggers	100TM231	K500TM231M K500TM231T	MS10231	700TM231-2	3.2.47
Logic element 3-3-3-3OR-4 AND-NOT/3-3-3-3 OR-4 AND	100LK121	K500LK121 K500LK121M	MS10121	700LK121-2	3.2.15
Level converter	100PU124	K500PU124 K500PU124T	MS10124	700PU124-2	3.2.16
Level converter	100PU125	K500PU125 K500PU125T	MS10125	700PU125-2	3.2.17

Table 3.13. continued

Functional purpose	ESTL series		Analog	Variation without housing	No. of Figure in supplement
	100	K500	MS10000	700	3.2
Two D triggers	100TM130	K500TM130 K500TM130M	MS10130	700TM130-2	3.2.18
Two D triggers	100TM131	K500TM131T K500TM131M	MS10131	700TM131-2	3.2.19
Four triggers with latch	100TM133	K500TM133T K500TM133M	MS10133	700TM133-2	3.2.20
Two D triggers	100TM134	K500TM134 K500TM134M	MS10134	700TM134-2	3.2.21
Universal binary counter	-	K500IYe136	MS10136	-	3.2.22
Universal decimal counter	-	K500IYe137	MS10137	-	3.2.23
Universal shift register	100IR141	K500IR141	MS10141	-	3.2.24
SOZU 64 word memory - 1 bit	100IR141	K500RU148 K500RU148M	MS10148	-	3.2.25
12-input parity check circuit	100IYe160	K500IYe160 K500IYe160T	MS10160	700IYe160-2	3.2.26
3-stage low level decoder	100ID161	K500ID161M	MS10161	700ID161-2	3.2.27
3-stage high level decoder	100ID162	K500ID162M	MS10162	700ID162-2	3.2.28
8-channel multiplexer	100ID164	K500ID164M	MS10164	700ID164-2	3.2.29
Rapid transfer circuit	100IP179	K500IP179 K500IP179T	MS10179	700IP179-2	3.2.30
Duplexed high speed adder-subtractor	100IM180	K500IM180 K500IM180T	MS10180	700IM180-2	3.2.31
Resistor matrix	100NR400	K500NR400T	MS10400	700NR400-2	3.2.32

Table 3.13 continued

Functional purpose	ESTL series		Analog	Variation without housing	No. of Figure in supplement 3.2
	100	K500	MS10000	700	
SCZU 16-bit memory with control circuits	100RU401	K500RU401 K500RU401M	MS10401	700RU401-2	3.2.33
Associative memory with readout (2 words with 2 bits each)	100RU402	-	-	700RU402-2	3.2.34
Memory with 256 bits (256 words with 1 bit each) with circuit controls	-	K500RU410	MS10410	-	3.2.35
Memory with 128 bits (128 words with 1 bit each) with circuit controls	-	K500PU411	MS10411	-	3.2.36
Memory with 128 bits (128 words with 1 bit each) with circuit controls	-	K500RU412	MS10412	-	3.2.37
Permanent PZU memory with 1024 bits	-	K500RU149	MS10149	-	3.2.38
Arithmetic-logic device for 16 operations with 2 4-bit words	100IP181	K500IP181T K500IP181	MS10181	700IP181-2	3.2.39
Two OR logic elements with high power output	100LL210				
Two OR-NOT logic elements with high power output	100LYe211				
Two reproduction amplifiers	100UL480				
Coding element with priority	100IV165				

Table 3.13 continued

Functional purpose	ESTL series		Analog	Variation without housing	No. of Figure in supplement 3.2
	100	K500			
Four D triggers with input multiplexers	100TM173				
Two control circuits with voltage key	100KN490				
Three line receivers	100LP216	K500LP216M K500LP216T			
Line exciter	100LP128	K500LP128			
Two control circuits with universal current key	100KT491	-			
Line receiver	100LP129	K500LP129			

Notes 1.: IC series 100 and K500 have the same temperature range (-10...+70°C) and are made in the following housings: series 100 -- in housings 402.16-1, series K500 -- in housing 201.16-1, 201.16-5, 201.16-6, 238.16-2, 239.24-2. 2. Index M means that the microcircuit has ceramic housing type 201.16-5, 201.16-6; index 10 - in ceramic housing 201.16-1.

IC type 100TM1 (Fig. 3.23) is two double D triggers of the ms type with separate inputs for setting S, resetting R, synchronizing $\overline{C}_E$ and with common synchronization input C. The data is received on the master trigger from input D at C=0 and $\overline{C}_E$=0. During this time, the slave trigger stores the data received by the trigger in the previous cycle. The data storing occurs when the signal changes at input C from state 0 to state 1. In this case, trigger m changes to the storage mode, while trigger s changes to the receiving mode. Previously recorded data in the m trigger is transferred to the output of the circuit. At $\overline{C}_E$=1, the trigger is blocked at input C.

To achieve the calculating mode it is necessary to connect output Q to input D and feed counting pulses to input C or $\overline{C}_E$ (Fig. 3.23b). Compulsory setting (S) and resetting (R) are achieved at any moment of time, independently of the state of other trigger inputs (Fig. 3.24).

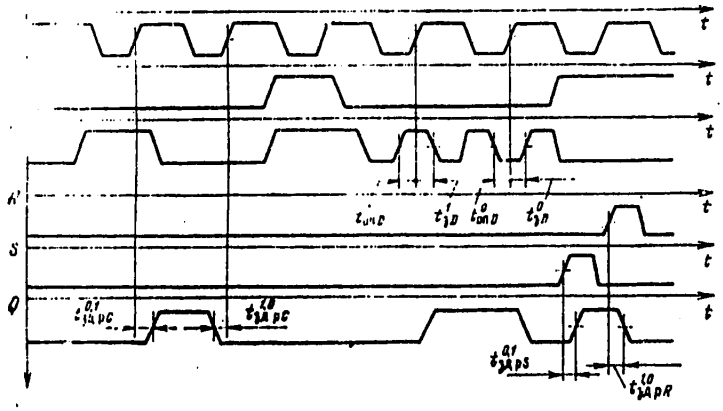


Fig. 3.24. Time diagram of a D trigger type 100TM131 operation in the calculation mode.

IC type 100TM133 is four D triggers with strobing elements at the trigger inputs. Strobing elements are divided with respect to trigger pairs by strobing outputs (G1, G2), synchronization input $\overline{C}_E$ and common synchronization input C. The data is received from input D at C= 1 and $\overline{C}_E$ =1, in this case direct data transmission from the input to the output of the system may be blocked by signal 1 at the input of the strobing element. Data storing occurs when the signals change at inputs G1 and G2 from state 1 to state 0. When all triggers are synchronized with respect to the common input C, 0 must be set at the inputs of separate synchronization or they must remain switched off. With separate synchronization of trigger pairs with respect to $\overline{C}_E$ inputs, the common synchronization input C must remain switched off , or signal 0 must be fed to it (Fig. 3.25).

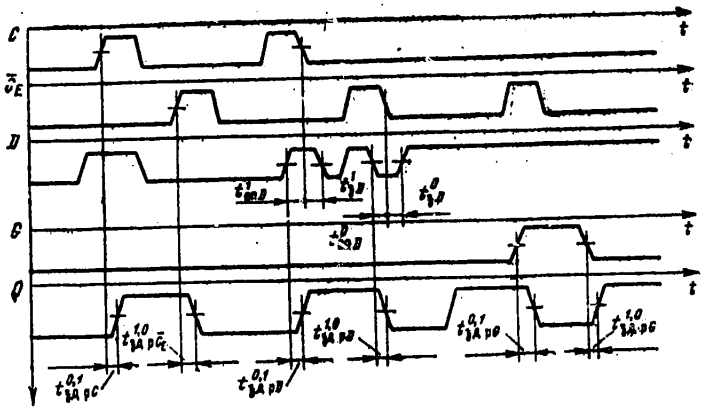


Fig. 3.25. Time diagram of D trigger type 100TM133.

To provide proper operation of the trigger circuits, it is necessary to take into account a number of additional parameters shown in the above-cited time diagrams:

$t^{1,0}_{s\,D}$, $t^{1,0}_{s\,S}$ -- minimum allowable delay time of the signal front or cut-off at inputs D or S with respect to the positive synchronization pulse front; $t^{1,0}_{on\,D}$, $t^{1,0}_{on\,S}$ -- minimal allowable time for advance of the front and cut-off of signals at inputs D or S with respect to the positive front of the synchronization pulse. The values of these parameters must be as follows: $t^{1}_{on\,D}$ with respect to the D input -- not less than 2.5 nanoseconds; $t^{1}_{on\,S}$ with respect to the S input -- not less than 3.5 nanoseconds, $t^{1}_{s\,D}$ with respect to the D input -- not less than 1.5 nanoseconds and $t^{1}_{s\,S}$ with respect to the S input -- not less than 1.5 nanoseconds.

IC type 100ID164 is an 8-channel multiplexer with an inhibition input W made of basic logic elements. The presence of the inhibition input makes it possible to organize high level decoding circuits and implement an "OR wiring" operation of circuits for multiplexing (combining) over eight channels. IC type 100IYe160 (12-input parity check circuit) is a combination of nine logic elements that implement the "OR locking" to function. The circuit is designed to determine a parity of words up to 12 bits long. The output voltage corresponds to level 1 if an odd number of digit "units" is present at the circuit inputs.

IC type 100IP179 is a high-speed carry unit and is designed for combined use with IC types 100IP180 or 100IP181 in high-speed acting arithmetic and logic devices, operating with long words. The circuit consists of ten OR-NOT-OR logic elements in which the collectors of the input transistors are combined in an "OR wiring" circuit. IC type 100IP181 are high-speed universal arithmetic-logic devices (ALU), designed to implement 16 logic functions and 16 arithmetic operations with two four-bit numbers.

$A_0 \ldots A_3$ and $B_0 \ldots B_3$ are data inputs. Input variables A and B in the positive logic circuits are fed in the complementary code and output function Y, in this case, is also formed in the complementary code. The direct code of variables A, B and of output funcetion Y is used in the operation of the ALU in the negative logic function (0 corresponds to the upper level and 1 -- to the lower level). Inputs $S_0 \ldots S$ are used to assign the code of the function being implemented. Depending upon the signal at output M, the device implements logic or arithmetic operations. Full internal carry circuits are built-in in the ALU circuit. Input C is the carry input from the previous stages. The carry signal into the following stage is formed at output X_2.

The combined utilization of IC types 100IP 181 and 100IP179 makes it possible to almost halve the arithmetic operation time for 32-bit words. Two complementary group carry signals (outputs X_1 and X_3) produced in the ALU are used in the accelerated carry operating mode. The implementation of logic transformations of input variables A and B is done when signal 1 is fed to input M which blocks the internal carry circuits.

The value of the typical parameters of the ALU in inplementing arithmetic operations with words from 4 to 64 bits long, using accelerated carry circuits in 100IP179, are shown in Table 3.14. For the combined operation of series 100 and IC series 133 and 155 circuits, IC type 100PU124 is used. It consists of four 2-input level converters for transferring from TTL to IC of the ESTL type, as well as type 100PU125, which consists of four 2-input level converters for transferring from ESTL to IC type TTL.

We will consider the operation of level converters in greater detail. Fig. 3.26a shows one of four level converters included in IC type 100PU124. It consists of input diodes VD1-VD4, an input emitter repeater (transistor VT1), a differential amplifier (transistors VT5 and VT7), operating in a current switching mode, emitter repeaters(transistors VT4 and VT8), as well as a source of reference voltages (transistors VT9 and VT10).

TTL feed voltage (5.0 volts $\pm 5\%$) is fed to leadout 9 and the ESTL feed voltage (-5.2 volts $\pm 5\%$) is applied to leadout 8. Leadout 16 (common) is grounded and the load is connected to paraphase outputs 4 and 2. For strobing all four elementary converters located in this IC, second inputs of each converter are combined at leadout 6.

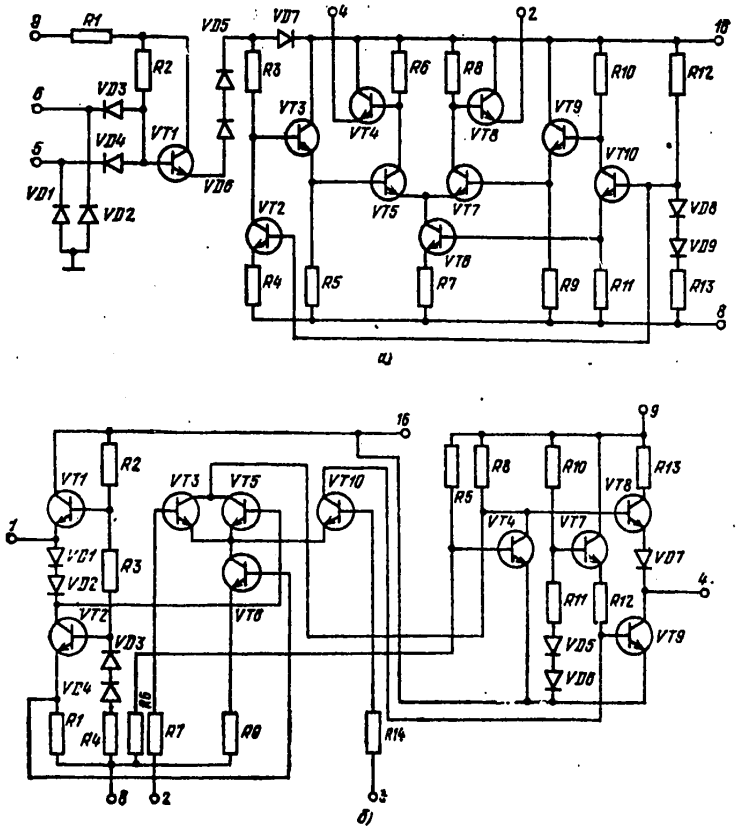


Fig. 3.26. Level converter for transferring from the TTL to the ESTL (IC type 100PU124 (a) and for transferring from the ESTL (IC type 100PU125) (b).

When using the circuit as a one-input level converter, the reference voltage U (leadout 1) is fed to leadouts 2 or 3 depending on whether the circuit must produce an inverted or noninverted conversion. Thus, in case U_{on2} is connected to input 3 and 1 is present at input 2, transistor VT3 is open, while transistor VT10 is closed. The voltage of the VT3 transistor collector is about 1 volt which is enough to block transistor VT8 reliably. The current through open transistorVT7 enters the base of transistor VT9, insuring its saturation,as a result of which

Table 3.14

Typical parametersof the ALU type 100IP181 when operating with accelerated carry circuit type 100IP179

Word length, bits	Adding time nanoseconds		Number of IC	
	With series carry	With accelerated carry	type 100IP181 in ALU	type 100IP179 in ALU circuit with accelerated carry
4	7	-	1	-
8	11	-	2	-
12	14	13	3	1
16	17	16	4	1
32	30	18	8	2
48	43	20	12	3
64	56	22	16	4

The reference voltage source forms the bias voltage for the current oscillator (transistor VT6). This voltage is taken off the emitter of transistor VT10. Two reference voltages are also created, U_{on1} =- 1.8 volts and U_{on2} =-0.7 volts. Voltage U_{on1} from emitter of transistor VT9 is fed to one input of the differential amplifier (base of transistor VT7), the voltage from resistor R12 enters the base of still another current oscillator (transistor VT2). When a 2.4 volt signal is applied to the input, a voltage of about 0.05 volts originates at the base of transistor VT3 and the voltage on the base of transistor VT5 will,in this case, be approximately equal to 0.8 volts which corresponds to level 1 in the ESTL circuits. Transistor VT5 is found to be open, level 0 is established at output 4 and level 1 -- at output2. To suppress interference pulses originating at the moment of switching in the feed circuits of the TTL circuits, diodes VD1 and VD2 are installed at the level converter input.

Fig. 3.26b shows a circuit of one of the four level converters in IC type 100PU125. The circuit consists of a current key (transistors VT3, VT5 and VT10), equipped with a stable current oscillator in the emitter circuit (transistor VT6 and resistor R9) and an output stage (similar to the inverter in the TTL circuits), operating in the saturation mode (transistors VT4, VT7,...VT9.). Feed foltage 5.0 volts $\pm$ 5% is applied to leadout 9 and feed voltage -5.2 volts $\pm$ 5% is applied to leadout 8. Leadout 16 (common) is grounded.

A bias is applied to the stable current oscillator from the internal source of reference voltages (elements VT1, VT2, VD1...VD4, R1...R4) and two reference voltages are also used: U_{on1} =-2.8 volts, taken off the collector of transistor VT2 and U_{on2} =1.29 volts, entering from the emitter of transistor VT1. Reference voltage U is used to fix the output voltage of 0 when the circuit inputs are connected to the -5.2 volt voltage source or are free.

voltage $U^{o}_{вых} \leq 0.5$ volts is established at output 4, corresponding to level 0 of the TTL circuits. When logic 0 is fed to input 2, transistorVT10 opens and VT3 closes. The voltage on the base of transistor VT9 reduced to the level of 1 volt which leads to the closing of transistor VT9. The voltage on the collector of transistor VT3 increases, which leads to the opening of transistor VT8. As a result a voltage is established at output 4 which corresponds to level 1 of TTL circuits (U^{1}=2.4 volts).

When all four elements of circuit 100PU125 are used, reference voltage $U_{вх2}$ from leadout 1 is fed to corresponding inputs of all four elements. In designing functional units using level converter circuits, it should be taken into account that the zero level $U^{o}_{вых} \leq 0.5$ volts is somewhat higher than the zero level of TTL circuits ($U^{o}_{вых} \leq 0.4$ volts) which reduces the noise resistance of the latter by 100 millivolts.

The branching coefficient of level conterters when operating at inputs of IC series 123, 155 is no greater than 8, and at inputs of IC series 130 -- no greater than 6.

IC type 100RU401 is a superoperative memory with nondestructive readout and consists of a matrix of trigger memory elements organized as 16 one-bit words. The matrix is equipped with a circuit for address and bit control. The electrical functional circuit of such a memory (Fig. 3.27a) consists of 16 triggers (elements for storing data) organized into a two-dimensional (along X and Y) 4x4 matrix (VT1-1...VT4-4), 8 address formers (F), read-in amplifiers(Зп 0,Зп 1) and two read-out amplifiers (Сч 0, Сч 1). The circuit operates in three modes: data storing, read-out and read-in. Addressing (selection when reading out and reading in) is done by simultaneously feeding level 1 into selected address buses (X,Y). Zero level must be maintained at all address buses not selected. When there are no signals at read-in amplifier inputs ($U_{вх\ Зп0}$=0, $U_{вх\ Зп1}$ =0) the signal from the selected cell of data storage is fed over the read-out buses to the input of the read-out amplifier 0 or 1. Depending upon whether 0 ar 1 were read-in in the selected cell, level 1 is formed at the output of the corresponding amplifier. The interrogated cell stores its data. Switching the trigger to the new state will occur only when new data is received. To read-in 0 or 1,it is necessary to supply level 1 simultaneously to the selected buses x, y and to one of the read-in buses (Зп 0 or Зп 1 respectively).

The data storage element (Fig. 3.27b) is an unsaturated trigger with direct coupling made with two three-emitter transistors VT1 and VT2, and three resistors. In the storage mode, the trigger has emitters E2...E5 operating while the circuits of emitters E1, E6 are disconnected. In the read-out and read-in modes, the trigger has emitters E1, E6 operating, while circuits of emitters E2...E5 are disconnected. Read-out and read-in is done over the P_1 and P_2 buses.

IC type 100RU402 is an associative memory device. The associative memory device (AZU) is designed for operation with 2-bit words. Besides storage functions, the

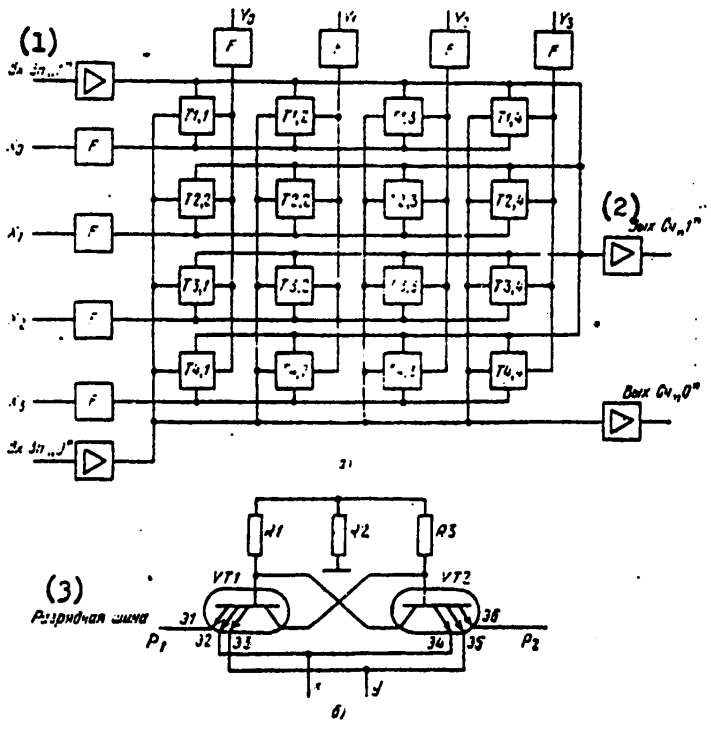


Fig. 3.27. Electrical functional circuit of a superoperative memory (a) and a data storage element (b).
1. Вх Зп 1 -- input read-in 1
2. Вых Зп 1 -- output read-out 1.
3. bit bus

AZU does arithmetic operations on the stored numbers. At the basis of the AZU design is a system of access by a tag -- the access to the needed word and its selection is made by a tag contained in the desired word itself. Associative selection (search mode) in microcircuit 100RU402 may be made under conditions of "masking" the interrogated data. The retrieval is over two buses for each address.

Combinations 1-0 and 0-1 are used respectively for the retrieval of the 1 and the 0 states. Combinations 1-1 correspond to the "mask," i.e., in this case, the reaction at the "word comparison" output corresponds to noncoincidence of the interrogated data and any data stored under any address.

3.5.2. Basic Electrical Parameters and Typical Characteristics of IC type ESTL

Digital type ESTL IC, besides the usual list of electrical parameters typical for other digital IC also have special static parameters: input and output threshold voltages.

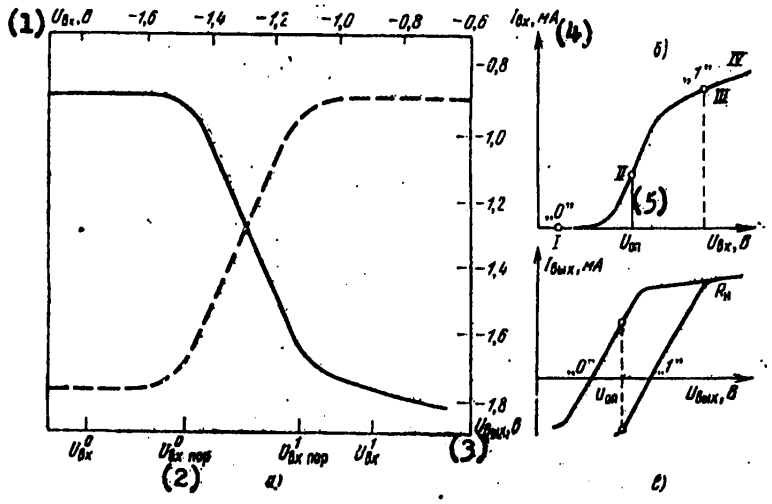


Fig. 3.28. Characteristics of basic logic element of the ESTL series;
a -- transfer (OR-NOT output, solid line; OR output, broken line)
b -- input, c -- output, with respect to current.

1. $U_{вх}$, volts -- input voltage
2. $U_{вх\ пор}$ -- threshold input voltage
3. $U_{вых}$ volts -- output voltage
4. $I_{вх}$, milliamps -- input current
5. $U_{оп}$ -- reference voltage.

Fig. 3.28a shows the typical transfer characteristics of a basic logic element of series 100, K500 with direct and inverse outputs. By means of these curves, it is possible to give the following parameter definitions for ESTL circuits: $U^1_{вх\ пор}$, $U^0_{вх\ пор}$ -- input threshold voltages; $U^1_{вых\ пор}$, $U^0_{вых\ пор}$ -- output threshold voltages; $U^1_{вх}$, $U^0_{вх}$ -- input voltages; $U^1_{вых}$ $U^0_{вых}$ -- output voltages of unity and zero. These parameters may be used to calculate the following: voltages of static noise resistance $U^1_{пом} = U^1_{вых\ пор} - U^1_{вх\ пор}$ and $U^0_{пом} = U^0_{вх\ пор} - U^0_{вых\ пор}$, logic gradient $U_л = U^1_{вых} - U^0_{вых}$, as well as the zone of switching $\Delta U = U^1_{вх\ пор} - U^0_{вх\ пор}$.

Taking into account the low values of output logic and the unavoidable technological spread of rated elements (therefore, also of the electrical parameters of the keys), maximum and minimum parameter values were established for the ESTL circuits that determine the transfer characteristic (Table 3.15). These parameters correspond to the allowable values of static interferences (for $-10 < t < 75°C$) $U^1_{пом} \geq 125$ millivolts, $U^0_{пом} \geq 155$ millivolts; to deviation of output levels of 1 and 0 (for $t = 25°C$), $\Delta U^0_{вых} \geq 690$ millivolts; switching zone (for $t = 25°C$) $\Delta U_п \leq 370$ millimeters.

We will now consider the input characteristic of the basic logic element OR-NOT/OR of the ESTL series (Fig. 3.21). The input characteristic of this circuit (Fig. 3.28b) has four zones.

In zone 1 the input transistors are blocked and the input current is low (equal to the leakage current between the collector and the base). Entire current $I_э$ flows through the emitter circuit of transistor VT5. In zone II, as the voltage increases on one of the input transistor VT1-VT4, it gradually becomes conducting. The input current increases which increases collector current I_{k1} due to the corresponding reduction in collector current I_{K2} of transistor VT5. At a certain value of voltage $U_{вх}$, collector current I_{K2} is reduced to a value considerably lower than $I_э$. In this case, the current through resistor R7 remains practically constant.

In zone III, as voltage $U_{вх}$ increases further, current $I_э$ and voltage U_{R7} will increase as a result of which the differential input impedance of the circuit will rise sharply. In zone IV, the transistor becomes fully conducting and picks up all of current $I_{K1} \approx I_э = \text{const}$.

In the cut-off state of the circuit, at voltage 1 on output 2, its working point is located on zone I of the input characteristic, while in the conducting state -- in zone III. Zone II is a transition zone. In this state the input impedance is minimal, while in zones I and III for $U_{вх}$ equal to voltages 0 or 1 the input impedance is high.

Table 3.15

Electrical parameters of IC series ESTL that determine the transfer characteristic

Parameter	Parameter values at t, °C						Values of electrical mode at inputs, volts, at $U_{пит}$ = -5.2 volt			
	-10		25		75					
	min.	max.	min.	max.	min.	max.	$U^1_{вх\ пор}$	$U^0_{вх\ пор}$	$U^1_{вх}$	$U^0_{вх}$
Output threshold voltage 1, $U^1_{вых\ пор}$ volts	-1.040		-0.980		-0.920		-1.165 -1.105 -1.105	-1.495 -1.475 -1.450	- - -	- - -
Output voltage 1, $U^1_{вых}$, volts	-1.020	-0.860 -1.650	-0.960	-0.810	-0.900	-0.720			-0.860 -0.810 -0.720	-1.880 -1.850 -1.830
Output threshold voltage 0, $U^0_{вых\ пор}$, volts				-1.630		-1.605	-1.165 -1.105 -1.045	-1.495 -1.475 -1.450	- - -	- - -
Output voltage 0, $U^0_{вых}$, volts	-1.880	-1.670	-1.850	-1.650	-1.830	-1.625	-0.860 -0.810 -0.720	-1.880 -1.850 -1.830	- - -	- - -

Table 3.16

Electrical parameters of IC series of ESTL

Parameter	Values minimal	Values maximal	Ambient temperature, t°, C
Input current 0, $I^0_{вх}$, microamp.	0.5	-	25
Input current 1, $I^1_{вх}$, microamp.	-	265	25
Output threshold voltage 1, $U^1_{вых\ пор}$, volts	-.92 - 1.04	- -	75 -10
Output threshold voltage 0, $U^0_{вых\ пор}$, volts	- -	-1.605 -1.650	75 -10
Output voltage 1, $U^1_{вых}$, volts	-0.9 -1.02	-0.72 -0.86	75 -10
Output voltage 0, $U^0_{вых}$, volts	-1.88	-1.67	-10
Current used $I_{пот}$, ma	-	25	75
Time of propagation delay when connected, $t^{1,0}_{здр}$, nanoseconds	-	2.9	25
Time of propagation delay when disconnected $t^{0,1}_{здр}$, nanoseconds	-	2.9	25
Output branching coefficient		15	75 -10
Power consumed $P_{пот}$, milliwatts (per logic element OR-NOT/OR)	-	35	25

The output characteristics of the key at the transistor VT8 output (see Fig. 3.21) are shown in Fig. 3.28c. Depending upon the value of the given voltage at the output, current $I_{вых}$ will flow into or out of the circuit. At each circuit state, the reduction in $U_{вых}$ at the VT8 transistor output leads to this transistor being more conductive, and an increase in outflowing output current $I_{вых}$. An increase in $U_{вых}$ makes this transistor less conducting and increases the inflowing output current $I_{вых}$. A further increase in $U_{вых}$ may make the emitter repeater fully nonconducting, after which the current will be determined by the load impedance which will determine the slope of characteristic $I_{вых}$ ($U_{вых}$).

The low output impedance of the emitter provides a high loading capacity of the ESTL circuits on DC. However, the actual loading capacity in the dynamic mode, due to the input capacitance of the circuit and the capacitance of the wiring is reduced to $K_{раз} = 15$.

We will now consider the dynamic parameters of the ESTL circuits. The basic parameter that determines the dynamic properties of the circuit is the propagation delay time when connecting and disconnecting ($t^{1,0}_{зд.р}$, $t^{0,1}_{зд.р}$). ESTL circuits are the quickest digital IC. At normal conditions and load impedance $R_н$ = 51 ohms, their typical propagation delay time is 7 nanoseconds. The delay time is measured at the level of 50% from the full gradient of the logic level when the circuit is switched.

It may be seen from the characteristics shown in Fig. 3.29 that the greatest effect on the propagation delay is produced by a change in the feed voltage, the voltage bias level and by an increase in the capacitive loading.

ESTL series 100, K500 are considered to have identical electrical parameters and differ only in functional composition, the type of housing and the operating conditions. Table 3.16 shows the values of the operating electrical parameters of the basic logic element of series 100 and K500 in a temperature range. The limiting allowable modes of operation for the ESTL series is shown below:

Maximum feed voltage, $U_{ип}$, volts	-7 for 5 millisec; -6 constantly
Maximum input voltage $U_{вх\ max}$, volts	0
Minimum input voltage $U_{вх\ min}$, volts	-5.5
Maximum output current $I_{вых\ max}$, milliamp	40

3.5.3. Certain Special Features in the Use of IC type ESTL

We will consider the special features of using IC type ESTL on an example of the series 100. As already mentioned above, ESTL circuits have a negative feed voltage source of -5.2 volts ± 5% and, because of this, negative voltages of logic levels. Moreover, ESTL circuits logic levels are low in absolute value($U^1_{вых} \approx$ - 1 volt and $U^0_{вых}$ =-1.65 volts). All this does not allow direct connection to inputs and outputs of IC type ESTL to IC type TTL or the use of MOS structures. For the mutual interfacing of logics, special circuits of converter 100PU124 and 100PU125 must be used. In wiring apparatus of IC series 100 (besides IC types 100LP115, 10CLP116 and 100LP124) all unused inputs and outputs are left free.

Unused inputs of IC types 100LP115 and 100LP116 must be connected to a reference voltage source (leadout 9 of IC type 100LP115 and leadout 11 of IC type 100LP116) or to feed voltage source $U_{ип}$ = -5.2 volts ± 5%. Unused inputs of IC type 100PU124 are connected to feed source $U_{ип}$ = 5.0 volts ± 5% through a resistor rated at 1 kohm. No more than 20 unused inputs may be connected to one resistor. If it is necessary to feed a constant signal 0 to inputs of several IC, it may be obtained from any logic IC series 100 that forms signal 0 with the connected inputs. The number of loads which may be connected to the output of such an element should not exceed 24.

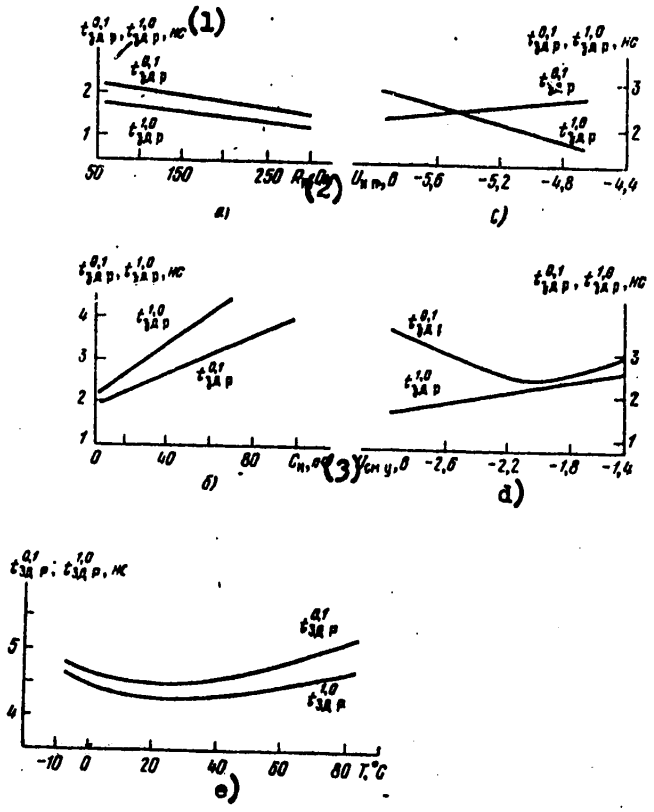


Fig. 3.29. Relationships between dynamic parameters and: resistive load (a), load capacitance (b); voltage feed source (c); bias voltage (d); and temperature (e).

1. nanoseconds
2. ohms
3. picofarads

The ESTL microcircuits considered above allow a combination of direct and inverse outputs into a "wired OR" and a "wired AND" with a combination coefficient $K_{o\sigma} \leqslant \leqslant 4$, as well as a combination of a direct output with an inverse one (Fig. 3.30). The latter combination method makes it possible to receive and transmit signals from several elements over one common communications line (Fig. 3.31a).

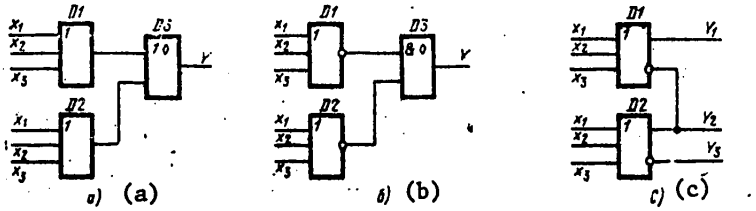


Fig. 3.30. Combination of IC type ESTL outputs into a "wired OR" (a) into a "wired AND' (b), a combination of direct and inverse outputs (c).

It should be remembered that as the number of combined outputs is increased, the levels of output voltage change which leads to a reduction in the noise resistance of the IC. Moreover, in the "wired OR" operating mode when even one IC is switched from state 1 to state 0, a negative interference appears at the output of the combined circuits (Fig. 3.31b) which may cause a false operation of the load element. The amplitude and duration of the interference depends on the length of the communications line that connects the elements in the "wired OR." Taking the above into account, it is recommended to combine outputs within one board and, if possible, outputs of IC which are beside each other. Taking the output from the board of an IC that does not have an output combination is recommended.

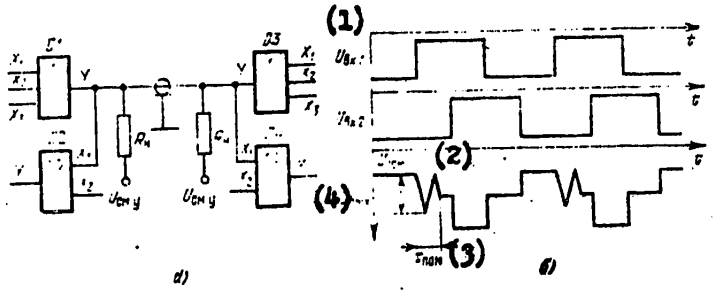


Fig. 3.31. Circuit for signal transmission from several IC type ESTL over one common communications line (a) and a time diagram (b)

1. $U_{вх}$ -- input voltage
2. $U_{пом}$ -- interference voltage
3. $U_{вых}$ -- output voltage
4. $\tau_{пом}$ -- interference time

As already mentioned above, ESTL circuits have a fairly high load capacity ($K_{paz} \geq 10$) which is due to the low input impedance of the emitter repeaters with which the keys are equipped and the low values of the input current (less than 265 microamperes). Within one board, the load capacity increases to $K_{paz} = 20$ and for microcircuits 100LL110 and 100LYe111, designed to operate simultaneously on three transmission lines, the load capacity is still higher ($K_{paz} = 30$). It is recommended that the output of trigger circuits be loaded no more than with 6 inputs of IC loads. It is recommended to connect inputs of no more than 16 key-loads to the output of circuits, combined in a "wired OR." In this case, the reduced level of the output voltage and an increase in the propagation delay time should be taken into account.

When the logic element operates with a load resistor rated at 51 ohms (at $U_{cmy} = -2$ volts) the delay increase when connecting one input of the IC load is 0.1 nanoseconds, while the change in the duration of the output signal front for an increase in the load from 1 to 10 inputs does not exceed 0.5 nanoseconds. In all cases, when determining the allowable number of inputs that may be connected to the IC output, it is necessary to take into account the combination of several inputs within these IC. With the direct operation of elements with one another (over short lines of communications), resistors of various ratings connected to voltage sources $U_{un} = -5.2$ volts or to $U_{cmy} = -2.0$ volts may be used in the emitter circuits of the output repeaters.

The presence in the above-considered ESTL series triggers and logic elements of various types makes it easy to design typical functional computer units and discrete automatic system devices. Fig. 3.32 shows a 4-stage shift register circuit. The output part of the circuit is made up of 100TM131 triggers, the parallel data input circuit -- is made up of IC type 100LS119, while the output part is a decoder with two inputs and four outputs made of IC type 100LM105. To increase the number of register stages, data is fed to input D_{n-1} from the output of the previous stage and to input D_{n-4} from the output of the following stage. Depending on the type of signal, operations, enumerated in Table 3.17, are implemented at inputs S_1 and S_2 by the circuit.

Synchronous binary pulse counter (Fig. 3.33) is made of IC types 100TM131 (D5, D6, D8.1), 100LS118 (D1...D4) and 100LM105 (D7). Input Q_{n-1} implements the carry from the previous stage and output Q_{n-4} -- the carry to the following stage. The counter operation is controlled at input S of IC100LM105. With 1 at the S input, the circuit implements the function of a counter. With 0 at the S input, the circuit operates as four triggers and receives data in inputs $D_0 \ldots D_3$.

The combined utilization of ESTL and TTL circuits (Fig. 3.34) makes it possible to design special purpose units. Fig. 3.34a shows an indication circuit, designed with IC type 100PU125 (D1) (series ESTL) and IC type 133LA7 (D2) (series TTL) using the NSM 6,3-20 incandescent lamp as an indicator.

Table 3. 17

Operations implemented by the four-stage shift register, depending on signals S_1 and S_2

Inputs		Implemented operation
S_1	S_2	
0	0	Blocking
1	0	Shift right
0	1	Shift left
1	1	Data received in inputs D (the circuit operates as four triggers with separate inputs and outputs)

Table 3.18

Rated resistance resistors R1 and R2 with parallel matching

ρ, ohms	R_1, ohms	R_2, ohms
50	81	130
75	121	195
100	162	260
150	243	390

Taking into account the high-speed action of the ESTL circuits, special attention should be given to the arrangment of the communications lines between individual IC, as well as to boards and units. Circuits types 100LP115 and 100LP116 which are paraphase signal receivers from a two-wire communications line, were considered previously. However, data transfer between individual circuit boards may be implemented by single-phase signals (Fig. 3.34b).

When a single-phase signal is fed from the output of IC series 100 (D1...D3) to one of the inputs of the IC types looLP115 (D5...D7) or 100LP116, a reference voltage must be fed to the second input, produced in IC type 100LP115 (leadout 9) or 100 LP116 (leadout 11) located in the board from which the signal is transmitted Fig. 3.34b). One reference voltage source on the transmitting board (D4) may be loaded in the receiving board with no more than 10 inputs. Each IC type 100LP115 or 100LP116 may be used as a reference voltage source (D4) when transmitting beyond the limits of the board and as a signal receiver from the communications line (D5...D7). The reference voltage transmission line must be decoupled at the transmitting and receiving ends by no less than 1000 picofarad capacitors.

Three basic communications methods are recommended within the limits of one board. The series method is used for a communications line not over 200 millimeters

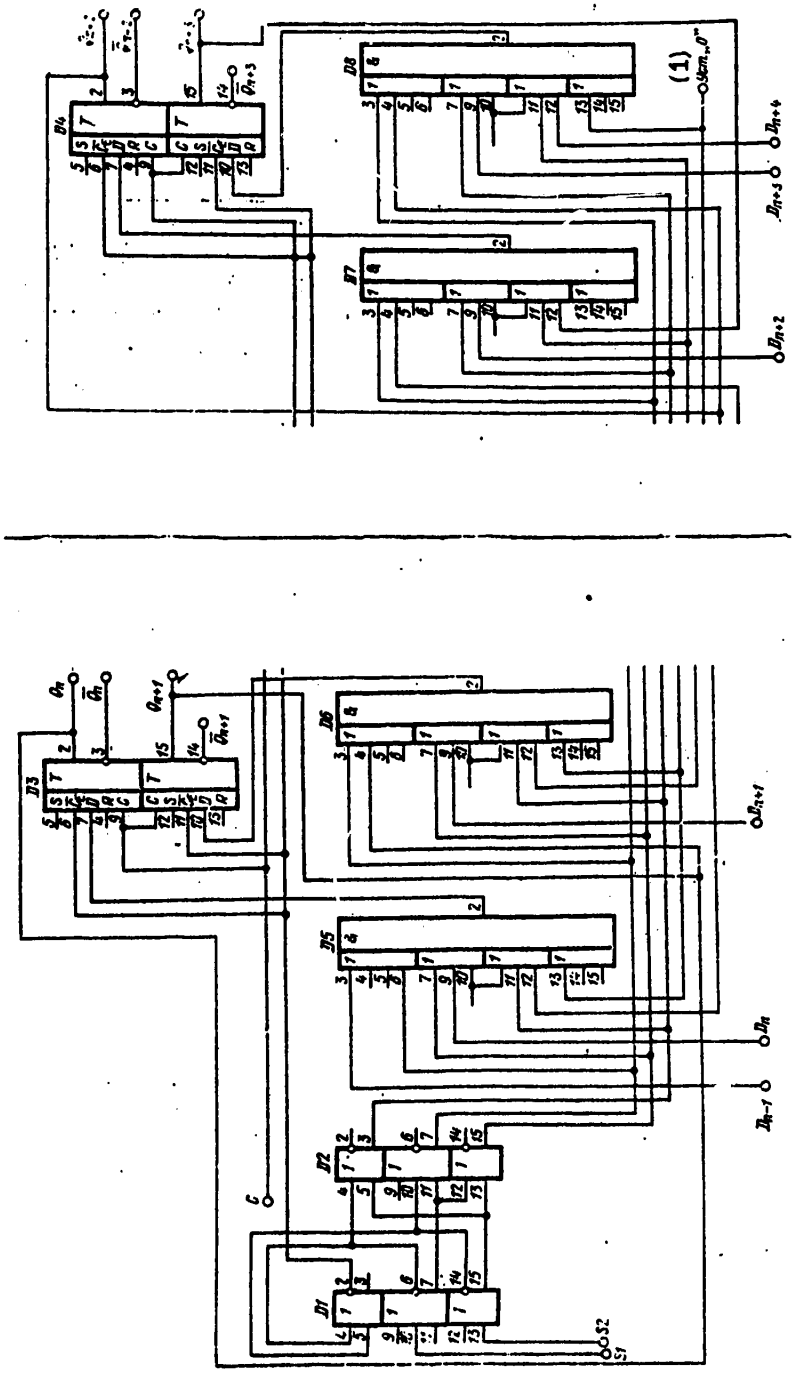


Fig. 3.32. Circuit of a 4-stage shift register, made of triggers 100TM131 (D3, D4), IC100LM105 (D1, D2) IC100LS119 (D5...D8).

1. Set 0

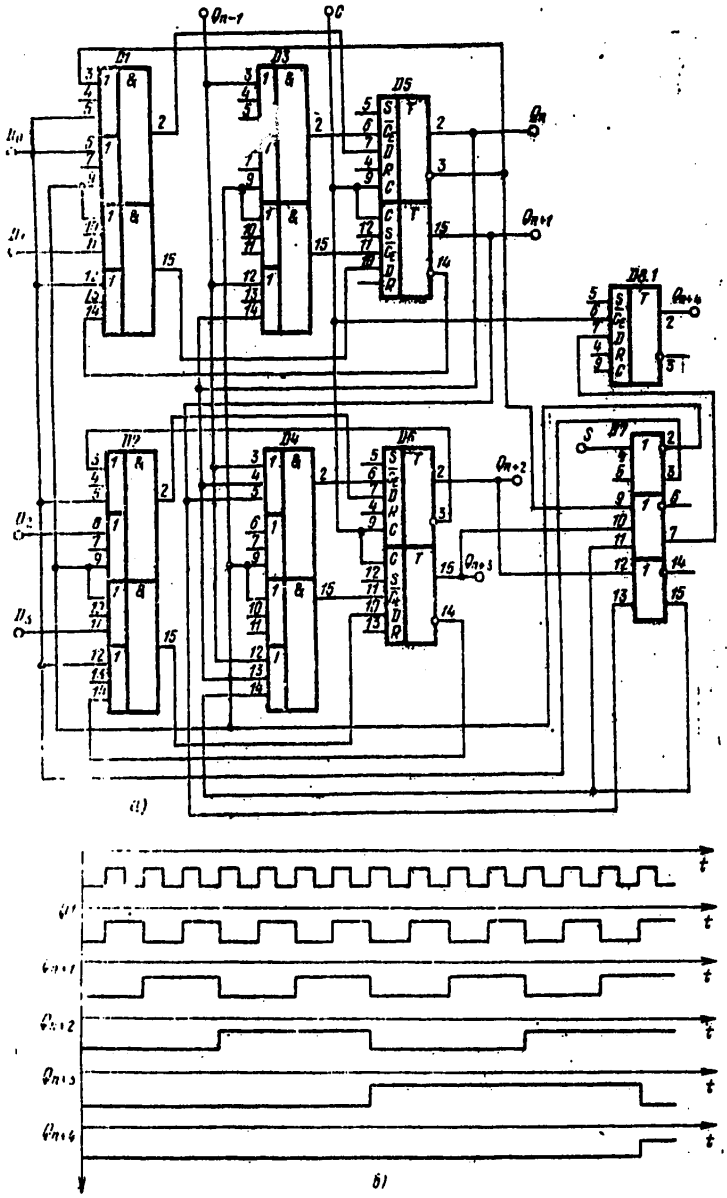


Fig. 3.33. Synchronous binary pulse counter from 0 to 15 (a) and time diagram of counter operation (b).

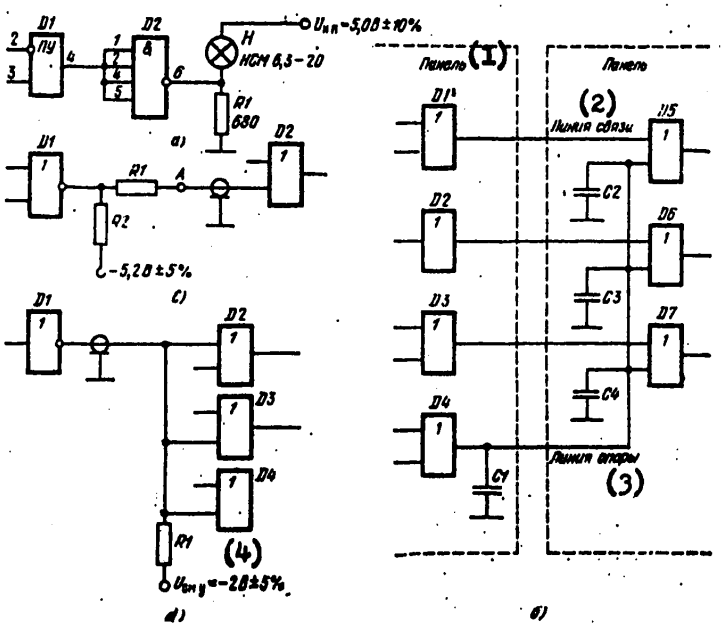


Fig. 3.34. Some ESTL connection circuits:
a -- indication circuit; b -- data transfer circuit between two boards of the device; c and d -- series and parallel matching of communications lines.

1. Panel
2. Communications line
3. Reference line
4. -2 volts

between the IC signal source and the load resistor. IC loads are connected along this communications line. The recommended length of the communications line should not be greater than 30 mm. In the beam method, beam lines no longer than 70 mm branch out at the end of which are connected IC loads. The load resistor is connected to one of the IC loads. Finally, in the concentration method, from the point of connection of the load resistor, at the end of communications line 200 mm long, communications lines also 200 mm long branch out to IC loads.

To eliminate "ringing" at the signal receiver input, it is recommended that the data be transmitted over a matched communications line. Fig. 3.34c, d shows circuits for implementing the series and parallel methods for matching communications lines. For communications lines with wave impedance ρ = 50 ohms, rated resistors R_1 = 43 ohms and R_2 = 240 ohms (with series matching) and R_1 = 51 ohms (with parallel matching) are used. Another method for parallel matching (by means of two resistors, R1 and R2, connected at the end of the line) is allowed, using the voltage of the bias level source U_{cmy} = -5.2 volts ± 5% to which resistor R2 is connected. The recommended values of resistors R1 and R2, depending on the wave impedance of the line, are shown in Table 3.18.

2291
CSO: 1863/209

3.6. Digital Integrated Circuits Based on MOS Structures

Integrated circuits based on field effect structures have become widespread in recent years. These structures are so named because their operation is based on the regulation of the current level in the layer of semiconductor near the surface by means of the influence of a transverse electrical field on the channel conductivity. Field effect transistors with oxide insulation which form a metal-oxide-semiconductor (MOS) structure and transistors with combination nitride-oxide insulation (MNOS) have found practical applications in digital IC's.

MOS structures are divided into two kinds: MOS transistors with built-in (doped) and with induced channels (Figure 3.35). In transistors of the latter type, the channel is created (induced) with the action of a control voltage which is fed to the gate. With an increase in this voltage, the channel is enriched by the carriers. In doped channel transistors, the channel is created in the production process. In terms of the type of conductivity, field effect transistors are broken down into p and n channel types.

In contrast to bipolar transistors, the current in the channel in MOS transistors is transfered by the majority carriers. MOS transistors are four-electrode semiconductor devices. The electrodes from which the motion of the majority carriers in the channel begins is called the source; the electrodes towards the majority carriers move is called the drain and the gate is the control electrode. The fourth electrode is connected to substrate - the semiconductor region on which the transistor is fabricated.

By applying a voltage to the gate, one can change the current level in the channel (with a constant voltage at the drain), and this means, one can change the channel resistance. MOS transistors, in contrast to bipolar ones, are voltage controlled, and in this sense are an analog of vacuum tubes. Three variants of NOT gates using MOS transistors with induced channels are shown in Figure 3.36. Integrated circuits with MOS structures have a number of advantages over bipolar circuits. They are simple in terms of structural design, well suited for production processes, have a high noise immunity as well as well as a low power dissipation. An MOS switch occupies enormously less area on the surface of the substrate as compared to a bipolar switch. This makes it possible to produce IC's with the equivalent of up to 10,000 switches on a single chip.

The majority of digital IC's using MOS structures which are being produced at the present time are based on MOS transistors with induced p-type channels, or as they are still called, p-channel transistors. Integrated circuits using complementary MOS transistors (CMOS) as well as n-channel transistors have become widespread in recent years. We shall deal with IC's based on MOS structures in more detail.

3.6.1. The Operational Principle of Integrated Circuits Using p-Channel MOS Transistors

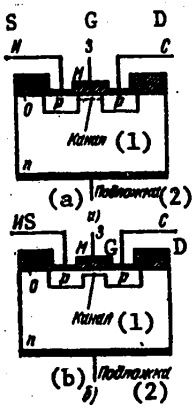


Figure 3.35. Cross-section through a structure with an induced (a) and a built-in (b) channel.

Key: 1. Channel;
2. Substrate.

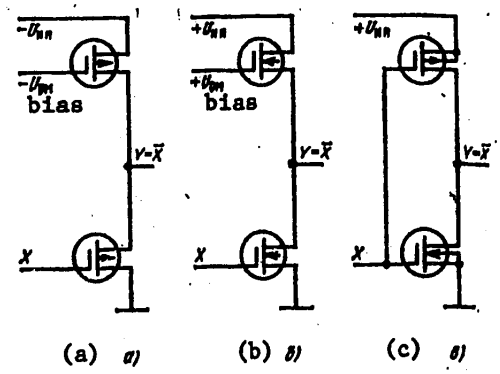


Figure 3.36. Circuits of inverters: using p-type channel MOS transistors (a), with an n-type channel (b) and using complementary transistors (c).

We shall analyze the operational principle of an MOS transistor with an induced p-channel [5] (Figure 3.37). If no voltages are applied to the structure, the p-n junctions which are formed by the drain, source and substrate regions, are cut off. A negative charge of mobile electrons, which establishes equilibrium for the positive charge of the surface states Q_{sur} (Figure 3.37a) is formed at the separation boundary between the semiconductor and the dielectric. The electrical field is concentrated at the separation boundary of the semiconductor and the SiO_2 oxide. When a negative voltage is applied to the gate, an electrical field appears, the action of which reduces the internal electrical field at the separation boundary. With an increase in the negative voltage at the gate, the free electrons are displaced from the region adjoining the gate and a depleted layer is formed in it. With a further increase in the gate voltage, the concentration of positively charged holes increases at the separation surface (Figure 3.37b).

With a definite voltage at the gate, when a sufficient quantity of holes is accumulated in the channel region, the conductivity of the separation surface becomes of the hole type and the p-type regions prove to the joined to each other by means of the inversion layer with the p-type conductivity. This layer also serves as the channel (Figure 3.37c). By applying a signal to the gate, one can modulate the number of carriers (holes) in the channel region, i.e., regulate the current flowing in the channel. The channel of the transistor is isolated from the major portion of the substrate by a high resistance bulk charge layer. For this reason, if several transistors are fabricated on a substrate, one can disregard their cross-coupling. A further increase in the voltage at the gate does not change the voltage in the bulk charge layer in the substrate, since the channel which is formed shields the remainder of the substrate.

However, the voltage drop across the bulk charge layer can be varied by applying a voltage to the substrate. A negative voltage applied to the substrate turns on the p-n junctions between the substrate and the drain and source regions. A positive voltage increases the bulk charge thickness, reduces the channel conductivity and with a further increase, can lead to the complete disappearance of the channel. Thus, the substrate, just as the gate, can be used as an electrode which controls the channel conductivity.

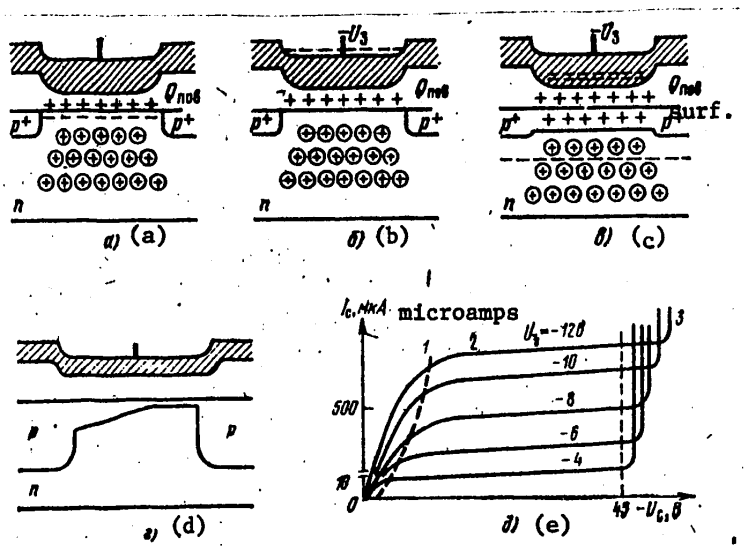


Figure 3.37. MOS transistors with an induced p-channel.

a,b,c. Various degrees of channel enrichment;
d. Saturation mode (the channel length decreases);
e. An example of the volt-ampere characteristic.

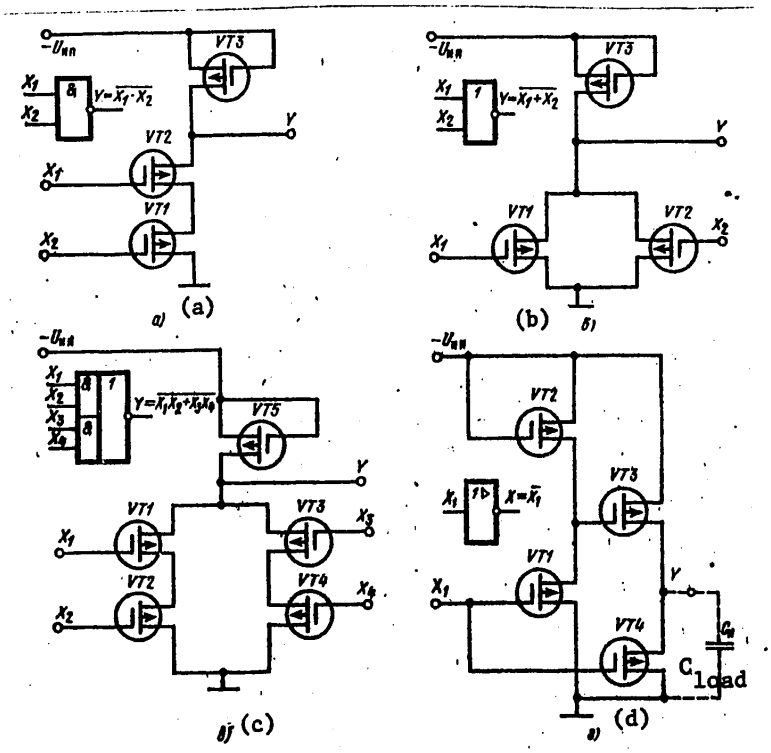


Figure 3.38. Schematic of basic logic elements for p-channel MOS transistors and their functional designation.

a. NAND gate;
b. NOR gate;
c. AND-OR-NOT gate;
d. NOT gate with a buffered output.

The voltage at the gate for which an induced channel appears between the drain and the source is called the turn-on voltage (U_{on}). A certain drain current I_D flows in the transistor channel with the action of a potential difference between the drain and the source. When the drain voltage U_D is low, the current I_D is directly proportional to the applied voltage and changes linearly. With an incrase in U_D, the current I_D will increase, since the electrical field along the channel increases, but U_D will simultaneously compensate for the voltage applied to the gate, something which causes a reduction in the channel thickness near the drain (Figure 3.37d), i.e., causes a reduction in its conductivity and leads to a deviation of the function I_D (U_D) from a linear law. Moreover, increasing U_D leads to an increase in the potential difference between the channel and the substrate, something which in turn causes the thickness of the bulk charge along the channel to change. A further increase in U_D leads to a reduction in the channel

length and the saturation of I_D. The saturation condition is defined by the expression:

$$|U_{D\ limit}| \simeq |U_G| - |U_{on}|.$$

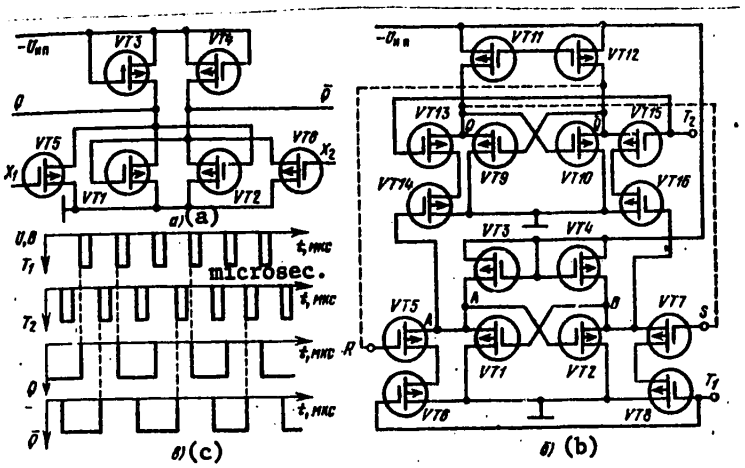


Figure 3.39. Schematics of flip-flops using p-channel MOS transistors.

a. Static flip-flop;
b. Universal two-stage flip-flop;
c. Time diagram showing the operation of the push-pull flip-flop in a count mode.

As can be seen from the volt-ampere characteristic of an MOS transistor (Figure 3.37e), the limiting voltage $U_{D\ lim}$ divides it into two working regions: the triode mode region (1) where the drain current I_D is strongly dependent on the drain voltage U_D and the pentode mode region (2), where the drain current I_D almost does not change with a change in the drain U_D. The breakdown region (3) is not used in operation [6].

We shall not consider examples of digital IC design based on p-channel MOS transistors. Three kinds of circuits using MOS transistors exist and are rather widely used: static, quasi-static and dynamic. The high input impedance of MOS transistors is used in quasi-static and dynamic circuits from which follows the capability of the parasitic gait capacitance of retaining a charge for a long time and maintaining the voltage level across the gate. Circuits of this type are most widely used for the construction of flip-flop devices, registers and counters [1].

3.6.2. Static Circuits Using p-Channel MOS Transistors

Circuits of basic logic gates which perform NAND and NOR functions are shown in Figure 3.38. For the sake of simplicity, the circuits of the substrate, which as a rule, is joined to the source of the transistor, are not shown here and in subsequent figures.

In switching circuits with a common source, designed around p-channel MOS transistors, a negative drain supply voltage is used. These are so-called negative logic circuits, i.e., the lower voltage (low level) corresponds to the output "1" voltage, and the higher voltage (high level) corresponds to the output "0" voltage. The circuits shown in Figure 3.38a,b contain two switching transistors each, VT1 and VT2, as well as one load transistor VT3. The gate of the load transistor may be connected to the bias voltage source, which usually has a higher level (in terms of its absolute value) than the voltage being switched by the switching circuit. The gate of the load transistor is most often connected to the source of the supply voltage for the drain circuits.

To realize the "NAND" function (Figure 3.38a), switch transistors VT1 and VT2 are connected in series with the load transistor VT3, forming a so-called tiered configuration. The current can flow through transistor VT3 only given the condition that transistors VT1 and VT2 are turned on, i.e., when signals are present at both inputs to the NAND gate. The number of switching transistors (the input fan-in factor $K_{in\ AND}$) can be increased, however, it usually does not exceed four. Because of the high input impedance of MOS transistors ($R_{in} > 10^{12}$ ohms), digital IC's designed around them have a high load fan-out factor ($K_{out} > 10 \ldots 20$). The load factor is limited only by the reduction in the switch speed with an increase in the number of loads, since the time constant for charging the parasitic capacitance of the load with the current flowing through the load transistor increases. When $K_{out} = 10$, the parasitic capacitance of the load will amount to $C_{load} = 20$ pFd. Considering the fact that the resistance of the turned-on load transistor usually falls in a range of 25 to 50 KOhms, we obtain a charging time constant of $R_{load}C_{load} = 0.5$ to 1 μsec, which corresponds to a maximum working frequency, f_r, of about 1 MHz.

A NOR gate (Figure 3.38b) is formed by the parallel connection of the switching transistors and the connection of their common drains to the source of the load transistor VT3. Here, the current path through transistor VT3 is turned on when one of the transistors turns on: VT1 or VT2, i.e., when a signal is present at one of the NOR circuit inputs. The number of inputs (the fan-in factor, K_{inOR}) can here be twice as great than in the case of series (multitiered) circuits, and runs up to 10. This is explained by the fact that parallel NOR circuits have a value for K_{inOR} which is limited only by the reduction in the "1" level by virtue of the voltage drop across the load from the overall leakage current in the drain--source circuits of the input transistors. Since this current is quite small, K_{inOR} can reach 10. An increase in the number of input transistors in multitiered circuits though complicates the topology and reduces the level of integration of p-type MOS integrated circuits. Although K_{inAND} does not exceed 4, the tier configuration makes it possible to realize more complex logic functions, for example AND-OR-NOT (Figure 3.38c).

To increase the load capacity, the IC output is provided with a buffer stage. In these circuits, the load capacitance is always charged and discharged through the small resistance of one of the turned-on output transistors. The output stage of such circuits is similar to the push-pull transistor output of TTL circuits (Figure 3.38). When there is no signal at the input to the circuit, transistor VT3 turns on and the capacitance C_{load} is charged; and when a signal is fed to the X_1 input of the circuit, transistor VT3 turns off, but VT4 turns on. The capacitance C_{load} is rapidly charged through it. The load capability of such circuits can be 20 to 30.

The connection of two inverters makes it possible to obtain a simplified RS flip-flop which contains four MOS transistors in all. The complete schematics of flip-flops included the complement of an IC series built using MOS structures also includes the control circuits (the "0" and "1" set inputs, the count input, etc.), which can be realized by means of AND and OR logic gates. In the simplest static flip-flop (Figure 3.39a), transistors VT5 and VT6 are used for the control.

Let the flip-flop be in the state where the voltage level at the Q output corresponds to "1", and at the $\overline{Q}$ output, is "0"; in this case, transistor VT1 is turned off and VT2 is turned on. When a "1" signal is fed to the gate of transistor VT5, transistor VT5 turns on, shunting the turned off transistor VT1. The voltage at the drain of transistor VT1 decreases, which leads to the cutting off transistor VT2 and the turning on of transistor VT1. As a result, the circuit shifts to the new state in which there is a "0" at the output Q and a "1" at the output $\overline{Q}$. To change the circuit to the initial state, it is necessary to feed a "1" signal to the gate of transistor VT6.

Two-stage clocked flip-flop devices consisting of a main and an auxiliary flip-flop are incorporated in IC series using p-channel MOS transistors along with combination circuits. The information entry in such flip-flops which have information and clock inputs is accomplished only by means of the enabling clock pulse.

In a push-pull two-stage RS flip-flop (Figure 3.39b), the main flip-flop which receives the information is formed by transistors VT1 - VT4, while the auxiliary flip-flop device which clamps the state is formed by transistors VT9 - VT12. The control is realized by means of AND gates formed by transistors VT5-VT8 and VT13-VT16.

We analyze the operation of the flip-flop. Let the main flip-flop be in the state where the voltage at point A corresponds to the "0" level and at point B it corresponds to the "1" level ($R = S = 0$). If in this case there is no clock pulse T_2, then there is the same probability at the state of the auxiliary flip-flop will be either $Q = 0$ or $Q = 1$. However, with the arrival of the first clock pulse T_2, the information will be rewritten into the auxiliary flip-flop from the main flip-flop and it is set to the $Q = 1$ and $\overline{Q} = 0$ state.

The appearance of the R or S information signals (when $T_1 = 0$) will not change the state of the flip-flop. However, if a $S = 1$ signal arrives at the gate of transistor VT7 and a clock pulse T_1 arrives simultaneously with it, the AND gate actuates (transistors VT7 and VT8), the voltage level at point B will change and

will correspond to "0", and to "1" at point A. Thus, the main flip-flop will shift to the new state, which with the arrival of the next pulse T_2 duplicates the state of the auxiliary flip-flop. Naturally the pulses T_1 and T_2 should be separated in time.

The schematic of a push-pull RS flip-flop (Figure 3.39b) is converted to a push-pull complementing flip-flop if the $\bar{Q}$ and the Q outputs are connected to the inputs of the main flip-flop (R and S respectively). In the absence of the count pulse T_1, with each arriving pulse T_2 the information will be rewritten from the main flip-flop into the auxiliary one (Figure 3.39c). With the first count pulse T_1 though, that AND gate actuates at both inputs of which there is a "1" signal, and the main flip-flop is set to the state which is the inverse of the auxiliary flip-flop. At the point in time, the rewrite of information into the auxiliary flip-flop is blocked, since $T_2 = 0$. The next pulse $T_2 = 1$ will set the auxiliary flip-flop to the state corresponding to the state of the main one.

3.6.3. Quasistatic and Dynamic Circuits

As was noted previously, the property of a MOS transistor of retaining the charge in the parasitic capacitance of the gates for a certain period of time is used in quasistatic and dynamic circuits. But in contrast to dynamic circuits, quasistatic flip-flops do not require the so-called "clock supply" during the information storage period. The clock supply is necessary when the information is entered and it is realized by means of clock pulses: phases having a width less than the time constant for charging and discharging the parasitic capacitances of the gates of the MOS transistor of the circuit. As compared to static type circuits, quasistatic and dynamic flip-flops make it possible to reduce the number of MOS transistor which are used by a factor of two to three times.

Two and three phase quasi-static D flip-flops have become the most widespread. We shall recall that D flip-flops, which are also called delay flip-flops, take the form of a device with two stable states and one information input. The truth table for a D flip-flop was given earlier (see Table 3.4).

We shall consider the operation of a two-phase quasistatic D flip-flop using MOS transistors (Figure 3.40) [1]. The circuit consists of three inverters: HE1 (VT2, VT3), HE2 (VT7, VT8), HE3 (VT10, VT11); three gates VT1, VT6, VT9; and a phase pulse driver $\Phi 2$ (VT4, VT5). Inverters HE1 and HE2 form a flip-flop circuit, one of the feedback circuits of which is looped through gate VT6 only where the signal $\Phi_2 = 1$ is present. Gate VT9 cuts off (with the $\Phi_2 = 0$ signal) or connects the output inverter HE3 to the flip-flop circuit (in the case of the $\Phi_2 = 1$ signal).

Without a clock pulse (the signals ($T_1 = \Phi_1 = 0$), gate VT1 is cut off regardless of the signal at its input. At the same time, the two other gates, VT6 and VT9, are turned on since the signal $F_2 = 1$. There will be a "1" level at the output of inverter HE1 and a "0" level at the output of HE2. The capacitance C_{load} which was previously charged through turned on gate VT9 and the load circuit of HE2 (VT7) is rapidly discharged through turned-on transistor VT8 and a level of Q = 1 is set at the flip-flop output.

To change the state of the flip-flop, it is necessary to feed a signal of D = 1 to its input. Then with the arrival of the clock pulse (the signals $T_1 = \Phi_1 = 1$), gate VT1 turns on. At the same time, gates VT6 and VT9 cut off (since the signal $F_2 = 0$), the feedback loop for the flip-flop is opened and the output inverter HE3 will be disconnected from the output from inverter HE2. With the action of the signal D = 1, which is fed through the turned-on gate VT1, a "0" level is set at the output of inverter HE1 and a "1" level is set at the output of inverter HE2. However, during the action of the clock pulse, the voltage level at the flip-flop output does not change (Q = 1), since the charge on C_{load} has still not had time to change substantially. With the completion of the clock pulse ($T_1 = \Phi_1 = 0$), gate VT1 cuts off, but since the signal $\Phi_2 = 1$, gates VT6 and VT9 turn on, which leads to a rapid charging of the capacitance C_{load} through the turned on gate V_9 and the load transistor of HE2 (VT7), as a result of which, the D flip-flop changes to the state Q = 0. Thus, following the completion of the clock pulse, at the input of the circuit D = 1 and at the output Q = 0.

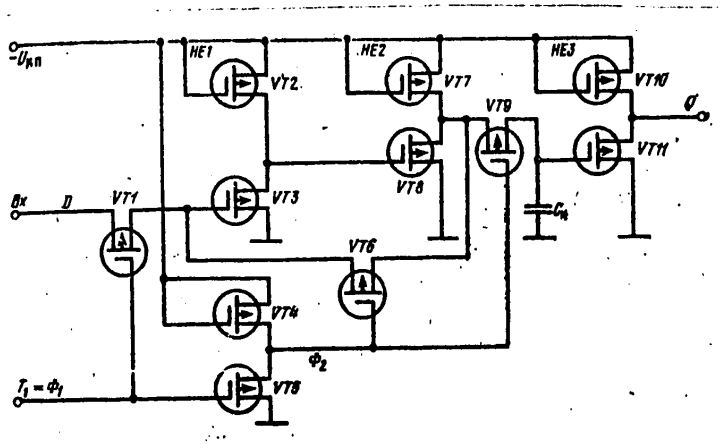


Figure 3.40. Schematic of a two-phase quasistatic D flip-flop using p-channel MOS transistors.

Quasistatic D flip-flops are frequently used to construct registers. In this case, the circuits which control the writing and shifts, as well as the phase drivers are incorporated in the IC series. This circumstance makes it possible to use a single cycle external signal similar to that which we had as the single cycle signal T1 for the two-phase D flip-flop (Figure 3.40) in quasistatic registers, which are multiphase systems. A drawback to quasistatic registers is the power consumption of the D flip-flops in the information storage mode. For this reason, dynamic registers using p-channel MOS transistors have become more widespread.

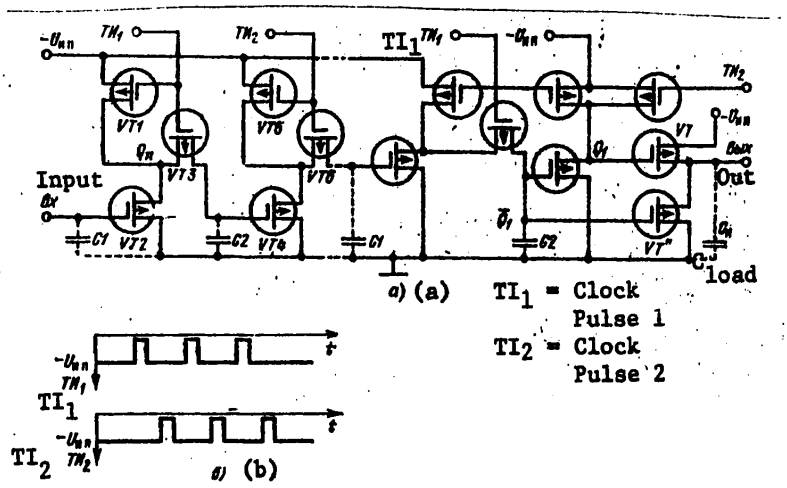


Figure 3.41. Schematic of a two cycle dynamic register using p-channel MOS transistors for n-digits (a) and the sequence of clock pulses (b).

Dynamic two-cycle and four-cycle flip-flops are used as shift registers and provide for the requisite delay in logic and arithmetic units of computers and digital automation equipment. We shall consider the operation of a two-cycle dynamic register using p-type MOS transistors (Figure 3.41) [1].

A register digit contains two inverters, using three transistors each (VT1 - VT3 and VT4-- VT6). The clock pulse TI_1 is fed simultaneously to the gate of the load transistor VT1 of the first inverter and the gate of gate VT3. The clock pulse TI_2 is fed t the gate of load transistor VT5 and simultaneously to the gate of the VT6 gate.

We shall analyze how information is written in as well as its shifting. Let a signal corresponding to "1" be fed to the input of the first low order digit. As a result, the parasitic capacitance C_1 is charged and transistor VT2 turns on. With the arrival of the clock pulse TI_1, transistors VTi and VT3 turn on and the parasitic capacitance C_2 is discharged through the turned-on transistor VT2. Upon the completion of the pulse TI_1, the charge corresponding to the "0" level is retained in capacitance C_2, as a result of which transistor VT4 will be cut off. The clock pulse TI_2 turns on transistors VT5 and VT6, and for this reason, a charging curcuit will be formed for the parasitic input capacitance of the next digit. Thus, over two clock pulses, the "1" signal which is fed to the input of the first digit proves to the rewritten into the input of the next digit.

We shall analyze the case where the input signal corresponds to the "0" level. In this case, transistor VT2 is cut off and with the arrival of the TI_1 pulse, capacitance C_2 will be charged through the circuit of turned on transistors VT1 and VT3, which provides for turning on transistor VT4. With the arrival of the TI_2 pulse, the capacitance C_1 of the second digit is discharged through turned on transistor VT4 down to the "0" level.

As a result, over the time of two clock pulses, the "0" signal which is fed to the input of the first digit will be rewritten into the input of the next, second digit. Since the clock pulses are fed to all of the register digits simultaneously, the information shift process runs in all digits simultaneously.

As can be seen from the schematic of the register shown in Figure 3.41a, the power consumption in each of the register digits occurs only at the moment of clock pulse arrival, when the load transistors VT1 and VT5 are turned on in each digit.

The width of the clock pulses is governed by the charging time of the parasitic capacitances (C_1, C_2,...) and amounts to 1 - 2 μsec, which assures a low average power consumption per digit (less than that of quasistatic registers by a factor of three to five times).

A high power output stage (transistors VT' and VT''), which provide for rapid discharging (through transistor VT'') or charging (through transistor VT'') of the load capacitance C_{load}, is inserted at the output of a dynamic resiters to obtain a good fan-out load capacity. The operational principle of a four-cycle dynamic register is similar to the operational principle of the two-cycle version, but four-cycle dynamic registers make it possible to obtain a higher working frequency for the circuit and a lower power consumption per digit.

3.6.4. The Operational Principle of Complementary MOS Transistor Integrated Circuits

As can be seen from the inverter circuit shown in Figure 3.36c, it is composed of MOS transistors of various types (complementary, CMOS transistors). The n-channel transistor is connected to the zero potential (to ground) while the p-channel transistor is connected to the positive power supply bus. Such a circuit provides for operation in a positive logic mode, i.e., the low signal level corresponds to the "0" output voltage while the high level corresponds to the "1" output voltage. The most widely used series of CMOS circuits operate in this mode.

Digital IC's based on CMOS structures have a number of advantages over p-channel MOS transistor circuits: they have a low power consumption in the static mode (at the level of units of microwatts), a relatively high speed, good noise immunity and a rather large load capacity [1]. The power consumed by a CMOS transistor circuit is expended primarily during the transient process in charging the output parasitic capacitances of the circuit and the internal capacitances of the transistor. For this reason, with an increase in the switching frequency of a circuit as well as with an increase in the equivalent output capacitance, the power consumption also rises, something which is modeled by the equation:

$$P_{dyn} = 2C_{load} f_w V_{cc}^2$$

where C_{load} is the equivalent load capacitance; f_w is the working frequency and V_{cc} is the supply voltage.

In the static mode, the power is governed by the power supply voltage and the leakage currents of the turned-off MOS transistor. Static, quasistatic and dynamic circuits can be designed around CMOS transistors just as in the case of p-channel MOS transistors.

We shall analyze the operation of the simplest static NAND and NOR positive logic circuits using CMOS transistors (Figure 3.42) [1]. As can be seen from these circuits, a parallel configuration of n-type MOS transistors and a series (tiered) configuration of p-type transistors are used for the realization of the NOR function. Moreover, each of the n-channel input transistors has the gate connected to a p-channel transistor. The p-channel transistors are connected in parallel and the n-channel transistors are connected in series to realize the NAND function.

When an X_1 signal corresponding to the "1" level is fed to the input of the NOR circuit, transistor VT1 turns on and VT4 turns off. As a result, the "0" level is produced at the circuit output. When a "0" signal is fed to both inputs, X_1 and X_2, transistors VT1 and VT2 turn off, but transistors VT4 and VT3 turn on, as a result of which, the voltage at the circuit output corresponds to "1" level, close to the supply voltage V_{cc}. Thus, the recharging of the load capacitance C_{load} is always accomplished through a turned-on p or n-channel transistor, something which increases the circuit speed. To reduce the dynamic power consumption, it is necessary to reduce the load capacitance C_{load}. The minimum supply voltage for a circuit using CMOS transistors is determined by the cutoff voltage $U_{off\ p}$ of the p-channel transistor, since it is greater than the voltage $U_{off\ n}$ of an n-channel transistor. The supply voltage is chosen greater than $U_{off\ p}$. This provides a circuit using CMOS transistors with a high level of noise immunity and good speed.

A comparison of the circuits of Figure 3.42 with similar designs using p-channel MOS transistors (Figure 3.38) shows that for the realization of the same functions, the CMOS transistor circuits are composed of a greater number of elements, something which can lead to drawbacks for them. But the increased operating speed and low power consumption assure their widescale application, especially for designing circuits with a high level of integration. In order to reduce the number of elements, a p-type load transistor is inserted in the CMOS transistor circuits (for positive logic circuits) (Figure 3.42c). The circuit realizes an OR-OR-NOT function and contains five MOS transistors [1]. We shall analyze its operation.

When $X_1 = 1$ and $X_2 = 0$, just as when $X_1 = 0$ and $X_2 = 1$, the pair of transistors of opposite conductivity will turn on (VT1, VT4 or VT2, VT3 respectively), something which provides for closing the current circuit through the load transistor VT5 to "ground". As a result, the voltage corresponding to the "0" level will appear at the circuit output. When $X_1 = X_2 = 1$ and $X_1 = X_2 = 0$, the upper pair of transistors (VT3, VT4) or the lower pair (VT1, VT2) is cut off, the current circuit is broken and the voltage at the circuit output corresponds to "1" level.

The consutrction of an OR-OR-NOT logic gate using p-channel MOS transistors requires seven transistors. Thus, the combining of CMOS transistors with a load transistor makes it possible to realize complex logic functions with a minimum of components.

Flip-flop circuits can be realized based on the simplest logic circuits using CMOS transistors. As an example, we shall consider the operation of a complementing flip-flop (Figure 3.42d).[1]. The circuit is composed of two D flip-flops: the main one which contains the HE1 and HE2 inverters and the inserted feedback gate B1, as well as the auxiliary flip-flop which contains the inverters HE3 and HE4 and the inserted gate B4. The main and auxiliary flip-flops are tied together through gates B2 and B3. The phase driver $\phi 1$, $\phi 2$ is designed around transistors VT1 and VT2.

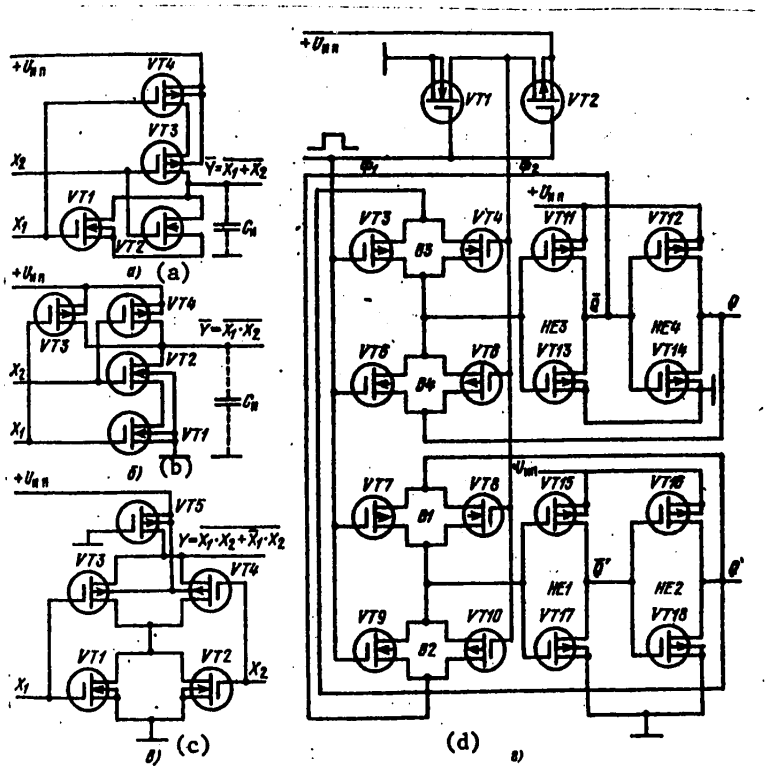


Figure 3.42. Circuits using CMOS transistors.

a. NOR;
b. NAND;
c. OR-OR-NOT;
d. Complementing flip-flop.

Let the main flip-flop be in the state Q' = 1 and $\overline{Q}$' = 0 when the clock pulse is a "0" (i.e., when $\Phi_1 = 0$, $\Phi_2 = 1$ and gates B1 and B3 are turned on, while gates B2 and B4 are turned off). Since gate B3 is turned on in this case, the voltage corresponding to the "1" levels (Q' = 1), in going to the gates of the HE3 inverter transistors, turns on the lower n-channel transistor and the auxiliary flip-flop is set to the $\overline{Q}$ = 0 and Q = 1 state.

However, if the clock pulse is a "1" ($\Phi_1 = 1$, $\Phi_2 = 0$), gates B2 and B4 turn on, while B1 and B3 turn off. The signal Q = 1 in going to the gate of the lower transistor of inverter HE3 through turned-on gate B4 keeps the inverter turned, and the state of the auxiliary flip-flop does not change ($\overline{Q} = 0$, Q = 1). At the same time, the level $\overline{Q} = 0$ turns off the lower and turns on the upper transistor of inverter HE1 through the turned-on gate B2, as a result of which the main flip-flop is set to the new state $\overline{Q}$' = 1 and Q' = 0. Following the completion of the clock pulse (the signals TI = 0, $\Phi_1 = 0$, $\Phi_2 = 1$), gates B1 and B3 are again turned on. The level Q' = 0 is fed through on gate B1 to the gate of the upper transistor of inverter HE1 and turns it on, maining the state $\overline{Q}$' = 1. Thus, the state of the main flip-flop does not change. At the same time, the level Q' = 0 turns off the lower and turns on the upper transistor of inverter HE3 through the turned-on gate B3, as a result of which the auxiliary flip-flop is set to the new state $\overline{Q} = 1$. Q = 0. Thus, with the arrival of each clock pulse, the state of the main flip-flop changes, while upon the completion of the clock pulse, this state is transfered to the auxiliary flip-flop.

The circuit of a static type flip-flop was treated above, however, quasistatic and dynamic flip-flops can be constructed with CMOS transistors, where these flip-flops are similar in terms of structure to the corresponding circuits using p-channel MOS transistors.

It should be noted that quasi-static and dynamic circuits (flip-flops and registers) using CMOS transistors make it possible to significantly reduce the number of elements as compared to similar static type circuits as well as significantly curtail the power consumption [1].

3.6.5. The Major Series of Integrated Circuits Using MOS Structures

Integrated circuits based on MOS structures, because of a whole series of advantages, are becoming increasingly widespread. Technological successes have made it possible in recent years to substantially increase their level of integration and operational speed, which has to a considerable extent governed their applications areas. In this sense, circuits based on CMOS transistors are to be singled out in particular, where these transistors make it possible to produce up to 10,000 elements on a chip. The production mastery of these circuits has made it possible to start the series production of compact and comparatively inexpensive microcalculators, memory matrices, electronic clocks and microprocessors.

The first series of IC's using MOS structures were made using "high voltage" p-channel MOS circuits. The K172 series is to be numbered among them, based on which an entire family of desk top electronic calculators was created. The

composition of the series was limited to four simple logic circuits (up to 30 elements per chip) and a two stage flip-flop with input logic. These circuits had a poor speed ($t_{del.prop.}$ = 1 μsec), a high power consumption (40 mW/gate) and high output voltage levels (in terms of the absolute value) (U^1_{out} = -7.5 volts; U^0_{out} - 2.3 volts) and were not compatible with TTL circuit levels.

Also of some interest is the 186 series which was among the first to be created, the complement of which even included a set of 4; 8, 21 and 64 bit quasistatic chip registers and a 90 bit dynamic shift register. The IC's of this series had a poor operational speed and large power consumption, as well as a high netative "1" level; however, a negative input voltage to positive output voltage converter circuit was incorporated in the series (the 186 PU1), which provided for interfacing to TTL circuits. The absence of combinatorial elements in the series somewhat limits its applications.

Defiecinecies in the initial series using p-channel MOS transistors were eliminated to a considerable extent with the series production mastery of IC's using CMOS structures: the 164, K176 and 564 series (analogs of the CD4000 and CD4000A). The IC's of these series have a dynamic power consumption of 20 mW/gate at a frequency of 1 MWz, while their static power consumption is measured in units of microwatts. The complement of the widely used series of IC's based on CMOS transistors is shown in Table 3.19 and the names of the analogs are given. As can be seen from Table 3.19, the complement of the CMOS series includes entire assemblies, besides the set of logic gates and flip-flops: registers, counters, memory circuits and level converters, which provide for joint operation with TTL integrated circuits. Data on the structural packaging of the indicated series and their temperature ranges are given in Table 3.20, while the main electrical operational parameters of the basic logic elements of the series indicated above using CMOS transistors are given in Table 3.21.

The application areas of integrated circuits included in the series of IC's with a CMOS structure are rather extensive. We shall consider several examples of K176 series IC applications to the construction of functional assemblies in equipment.

Thus, a four-bit register can be realized using two K176TM2 integrated circuits, two K176LA7 integrated circuits and one K176LA9 integrated circuits. Each bit of such a register consists of a D flip-flop and a distributor, the presence of which increases the functional capabilities of the register, making it a universal device. A bit in a push-pull shift register can be designed around the K176TM2 integrated circuit based on two single cycle D flip-flops.

Single cycle, series carry frequency dividers are simplest in terms of their circuit design realization. They are made using D flip-flops by connecting the outputs of the preceding bits to the inputs of the subsequent ones. The division factor of such a divider is $K_{div} = 2^h$, where h is the number of divider bits.

Single cycle divide-by-two and divide-by-eight frequency dividers (with series carry) can be designed around K176TM2 integrated circuits, but is more expedient

TABLE 3.19 The Composition of IC Series Based On CMOS Structures and Their Functional Analogs in the CD 4000 (RCA) and CD 4000A (RCA) Series

Functional Designation [1]	Subgroup, Kind and Ordinal Numbers of the Design (According to Function) [2]	Designation of the Functional Analog [3]	Number of the Outline Drawing in Appendix 3.1 [4]
Universal logic element (164, K176, 764)	LP1	07	-
Quad "exclusive OR" gate (164, K176, 564, 764)	LP2	30	3.3.1
Two 3NOR logic gates and a NOT gate (164, K176)	LP4	00	3.3.2
Quad 2NOR gate (164, K176, 564, 764)	LYe5	01	3.3.3
Two 4NOR logic gates (164, K176, 564)	LYe6	02	3.3.4
Quad 2NAND logic gates (164, K176, 564, 764, 765)	LA7	11	3.3.5
Two 4NAND logic gates (164, K176, 564, 764)	LA8	12	3.3.6
Three 3NAND logic gates (164, K176, 564, 764)	LA9	23	3.3.7
Three 3NOR logic gates (164, K176, 564, 764)	LYe10	25	3.3.8
Two 4NOR logic gates and a NOT logic gate (164, K176, 764)	LP11	-	3.3.9
Two 4NAND logic gates and a NOT logic gate (164, K176, 764)	LP12	-	3.3.10
A 9AND logic gate and a NOT logic gate (164, K176, 764)	LI1	-	3.3.11
Six gated NOT logic gates (564)	LN1	MS14502A	-
Two D flip-flops with "0" and "1" setting (164, K176, 564, 764, 765)	TM2	13	3.3.12
Four bidirectional switches (164, K176, 764)	KT1	16	3.3.13
Five inverting level converters (164, K176, 764)	PU1	-	3.3.14
Five bit counter (164, K176)	IYe2	TA-5971	3.3.15
18 bit shift register (164, K176)	IR10	-	3.3.16
4 x 10 decoder (164, K176, 564)	ID1	28	3.3.17
Dual four-bit static shift register (164, K176, 564)	IR2	15	3.3.18
Four bit full adder (164, K176, 564, 765)	IM1	08	3.3.39
Three AND-OR logic gates (164, K176)	LS1	-	3.3.20

[Table 3.19, continued]:

[1]	[2]	[3]	[4]
Six-bit binary counter (164, K176)	IYe1	24	3.3.21
Four-bit universal shift register (164, K176)	IR3	-	3.3.22
Two JK flip-flops (164, K176, 564)	TV1	027	3.3.23
16 bit main memory storage matrix (K176)	RM1	05	3.3.24
Eight-bit shift register (564)	IR6	34A	-
256-bit main memory with control circuit (K176, 564)	RU2	61	3.3.26
Decimal counter with decoder (K176)	IYe8	17	3.3.27
Two D flip-flops with "0" set (K176)	TM1	03	3.3.28
Six inverting level converters (K176)	PU2	09	3.3.29
Six noninverting level converters (K176)	PU3	10	3.3.30
Modulo 6 counter with decoder for data output to seven segment display (K176)	IYe3	-	3.3.31
Modulo 10 counter with decoder for data output to seven segment diaplay (K176)	IYe4	-	3.3.32
15-bit binary frequency divider (K176)	IYe5	-	3.3.33
Four-bit series-parallel register (564, 765)	IR9	35A	3.3.35
Three 3-input majority gates (564, 765)	LP13	-	3.3.36
Dual four-channel multiplexer (564, 765)	KP1	52A	3.3.37
Six NOT logic gates (563, 765)	LN2	49A	3.3.38
Four-bit bidirectional counter (564, 765)	IYe11	MS14516A	3.3.40
Quad AND-OR logic gate (564)	LS2	19A	3.3.41
Six level converters (564)	PU4	50A	3.3.42
Counter-divide-by-eight divider (564)	IYe9	22A	3.3.43
Quad D flip-flop (654)	TM3	42A	3.3.44
Quad RS flip-flop (564)	TR2	43A	3.3.45
Two four-bit counters (564)	IYe10	MS14520A	-
Four-bit comparator (564)	IP2	MS145585A	-
Quad bidirectional switch (564)	KT3	66A	-
Arithmetic logic unit (564)	IP3	MS14581A	-
Through carry circuit (564)	IP4	MS14582A	-
Eight channel multiplexer (564)	KP2	51A	-
12-bit comparator (564)	SA1	MS14531A	-
Triple majority multiplexer element (564)	IK1	-	-

[Table 3.19, continued]:

[1]	[2]	[3]	[4]
Multifunction register (564)	IR11	MS14580A	-

* * *

Note: Integrated circuits of the 164, K176 and 764 series are functional analogs of the CD4000 series IC's, while the IC's of the 654 series are analogs of the CD4000A series.

to construct group carry dividers (using cross-coupled shift register circuits) with a low division factor (of from 4 to 10) using K176 series integrated circuits. In such dividers, the input pulses are fed to a common bus for all of the digits; the arrival of the input pulses at the bit inputs of a given group is determined by the state of the control output of the previous group of digits.

Dividers using cross-coupled registers have an even division factor of $K_{div} = 2n$, where n is the number of bits.

By introducing additional feedback from the direct output of the highest order digit to the zero set input of the lowest order digit, one can produce an odd division factor: $K_{div} = 2n - 1$.

A series adder with carry storage can be realized using three K176LA7 integrated circuits and one K176TM2. The distributor for the input pulse train to four output buses is designed for use in multicycle electronic devices and can be constructed using K176LA7, K176LA9, K176TM2 and K176LYe5 integrated circuits. The operational synchronization of the digital information processing devices of such a pulse distributor is accomplished by means of introducing a clock generator, which provides for the generation of the clock pulse train and the multiplication of the pulses with the breakdown of the synchronized memory elements into groups. The number of memory elements in each group is governed by the fan-out factor of the clock pulse amplifiers of the multiplication circuitry.

For operation of the K176 series IC's with high power elements, it is expedient to use this series together with the circuit designed around the K149 series IC. The circuit is triggered from a power inverter, formed by the parallel connection of three K176LP1 IC inverters.

Circuits of the K176 series can be used in conjunction with K149 series microcircuits when triggering relays with current parameters of no more than 75 mA and voltage levels of no more than 15 volts, taking into account the permissible deviation in the power supply voltage. In the choice of the type of relay, it is necessary to take into account the change in the relay winding resistance as a function of temperature.

TABLE 3.20 Types of CMOS Series IC Packages

Series	Working Temperature Range, °C	Kind of Package	Designation of the Packages Used in the Series
164	-160 ... +85	Rectangular metal-glass	401.14-4
	-10 ... +70	Rectangular plastic	201.14-1
K176	-60 ... +25	Rectangular metal-glass	401.14-5
564		Rectangular metal-ceramic	402.16-1
		The same	402.16-3
		"	402.16-10
		"	402.16-16

When designing equipment around K176 series integrated circuits, one must consider the fact that the coupling capacitance between the wires connecting the transmitter microcircuits to the data receiver microcircuits is the load capacitance for the microcircuits which transmit the information, an increase in which leads to an increase in the dynamic current consumed by the microcircuits. In order to preclude the influence of crosstalk interference between individual conductors in asynchronous devices, the coupling capacitance should not exceed 100 pFd.

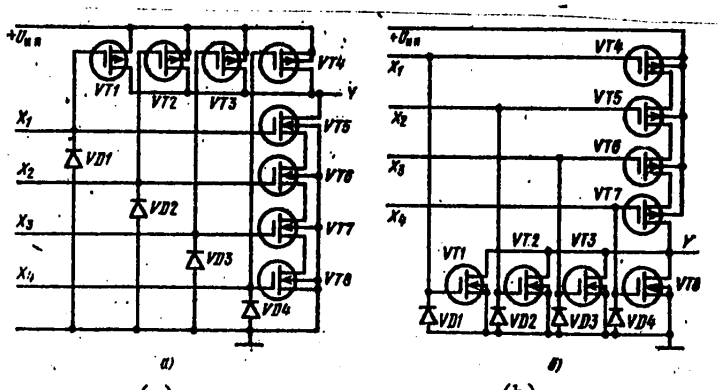
When designing equipment based on K176 series IC's, it is necessary to provide for protection against the intrusion of pulse interference into the "power" and "ground" buses, for which it is recommended that decoupling capacitors be installed in the power supply circuits: low frequency and high frequency capacitors. The types of capacitors and their capacitances are chosen depending on the equipment design.

The 5-bit counter (164IYe2 integrated circuit) and 18 bit shift register (164IR10 integrated circuit) included in the 164 series provides for operation at a frequency of 2.5 MHz. The ultimate permissible operational modes of the 164 series IC's in a temperature range of 160 to +85 °C are given below:

Maximum supply voltage, U_{ip}, volts	12 (for 3 seconds)
. . . . .	15 (for 5 seconds)[sic]
Maximum input voltage, $U_{in\ max}$, volts	15 (For 5 seconds)
Minimum input voltage, $U_{in\ min}$, volts	-0.5 (for 5 msec)
Maximum zero output current, $I^0_{out\ min}$, mA	1.0
The same for the one current, $I^1_{out\ max}$, mA	1.0
The lowest load resistance for which the maintenance of the "1" level is guaranteed, R_{load}, KOhms. . .	150

TABLE 3.21 Electrical Parameters of CMOS Series IC's

Parameters	Series 164	Series K176
Power supply voltage, V_{cc}, volts	9 ± 10%	9 ± 5%
The "0" input current, I^0_{in}, μA, no less than	-0.05	-0.1
The "1" input current, I^1_{in}, μA, no more than	0.05	0.1
"0" output voltage, U^0_{out}, volts, no more than	0.5	0.3
"1" output voltage, U^1_{out}, volts, no less than	7.7	8.2
Propagation delay time during turn-on, $t^{1,0}_{zd.r.}$, nsec, no more than	200 (when C_{load} = = 50 pFd)	250 (when C_{load} = 50 pFd)
Propagation delay time during turn-off, $t^{0,1}_{zd.r}$, nsec, no more than	200 (when C_{load} = = 50 pFd)	250 (when C_{load} = 50 pFd)
Current consumption with "0" at the input, I^0_{con}, μA, no more than	0.1	0.3
Current consumption with "1" at the input, I^1_{con}, μA, no more than	0.1	0.3
Static noise immunity, U_n, volts	0.9	0.9
Fan-out load factor, K_{out}	50	50



(a) (b)

Figure 3.43. Basic schematics of 164 (176) IC series for NAND (a) and NOR (b) gates.

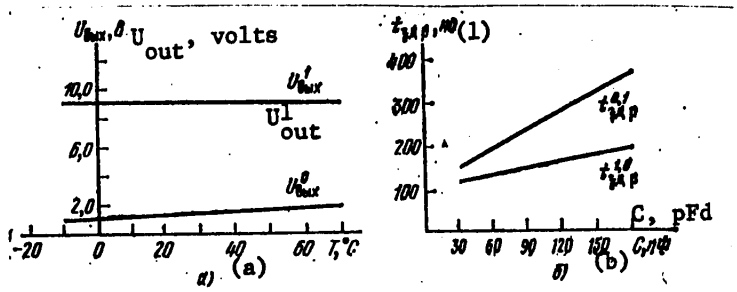


Figure 3.44. The functions $U_{out}(T)$ and the propagation delay time as a function of the load capacitance for K176TM2 series IC's.

Key: 1. Propagation delay time, nanoseconds.

Using the example of the 164 series, we shall consider the design principles for circuits using CMOS transistors and some of the specific features of their applications. As was shown above (Table 3.19), the complement of the series includes logic gates which perform NAND and NOR functions. The 164LA8 (Figure 3.43a) can be taken as the basic IC for the realization of the NAND function, while a 164LYe6 integrated circuit realizes a NOR function (Figure 3.43b). Practically all of the IC's of the 164 series are designed around these basic switches.

When the IC's of the 164 series are operated, the unused inputs in gates which realize the NOR function should be connected to the "ground" bus, while the circuit inputs which realize the NAND function should be connected to the supply bus. It is permissible to tie the unused inputs together with the used input of the same logic gate, but in this case, the fan-out factor of the preceding circuit driving the combined inputs is reduced by one. It is not permissble to tie the basic elements together at the outputs, with the exception of the base where the outputs of the basic elements are joined together (no more than four, all of the inputs of which are connected together. Operation of the integrated circuits with a supply voltage reduced down to 6 volts is permitted, however, in this case the electrical parameters may not conform to the values indicated in Table 3.21.

It is recommended that decoupling capacitors in the form of a set of two capacitors be inserted in the power supply circuits of IC's on printed circuit boards: low frequency capacitors (up to 20 KHz) designed for 2.2 μFd for each 50 IC's and high frequency capacitors (to 1.5 to 2 MHz) designed for 0.068 μFd for each 50 IC's.

We shall discuss the impact of temperature and load capacitance on CMOS transistor IC's using the example of the K176 series. The curves for the output voltage as a function of temperature for the K176TM2 integrated circuit (Figure 3.44a) show that U^1_{out} and U^0_{out} practically do not change with an increase in temperature, while the propagation delay time as a function of load capacitance for the K176TM2

IC (Figure 3.44b) show a greater dependence on load capacitance by the propagation delay time during cutoff, which with an increase C_{load} from 30 to 180 pFd more than doubles.

3.7. Integrated Circuits for Memories

The expansion of the applications areas of modern computer hardware has generated a rapid increase in the number of various classes of computers. The constant trend towards an increase in the complexity of the problem solved by computers in turn requires an increase in the volume and speed of the calculations, however, the speed of solving any problem with a computer is limited by the memory access time: the access time to the main memory (OZU). Memories using ferrites which underwent considerable development in first and second generation computers do not allow for a substantial reduction in main memory access time. Even with a reduction in the diameter of the ferrite cores down to 0.5 mm, a main memory access time of only 0.5 μsec can be obtained. At the same time, a ferrite memory which is fabricated by means of rather complex operations to thread the wires through the cores makes it difficult to assemble them and even makes such devices not technologically suitable for production. The development of microelectronics has made it possible to use semiconductor devices (bipolar transistors and MOS structures) for the construction of memories.

TABLE 3.22 Characteristics of Memories Based on Various Component Technologies

Type of Main Memory	Elements Used	Characteristics			
		Access Time, nsec	Typical Information Capacity, bits	Information Density, bits/cm^3	Power Consumption During Information Storage
Semiconductor	Bipolar Transistors	50...300	$10^3...10^5$	Up to 200	Yes
	MOS Structures	250...1,000	$10^3...10^6$	200...300	Yes
Magnetic	Ferrite Cores	350...1,200	$1-^6...10^8$	10...20	No

It can be seen from Table 3.22 in which the parameters and properties of main memories based on various component technology are compared [7] that it is expedient to design memories with an information capacity of less than 10^5 bits, but with a high operational speed, using bipolar transistors. Memories based on MOS structures have a capacity of $10^3...10^6$ bits with a moderate operational speed. Memories with a memory volume of more than 10^6 bits are constructed using ferrite cores, where

these memories have poor speed, but nonetheless the capability of storing data without consuming power. Considering the fact that the characteristics of memories based on MOS structures with respect to capacity, speed and power consumption are constantly being improved, one should anticipate their widescale development and applications in various computer classes in the upcoming years [7].

The use of semiconductor structures makes it possible to substantially increase memory speed, reduce the size and weight as well as increase operational reliability and eliminate matching elements between digital computer hardware and the memory through the application of a single type of component base in the various hardware [7].

In recent years, because of the improvement of bipolar IC's as well as the expansion of IC series using MOS transistors, static memory elements have been created (using bipolar structures as well as p-channel MOS transistors and CMOS transistors), as well as dynamic memories (using p-channel MOS transistors and MNOS structures) and memory elements based on "silicon on sapphire" structures. We shall treat the structures of each of these types of memory elements in more detail.

3.7.1. Memory elements Using Bipolar Structures

A static memory using bipolar structures (transistors) takes the form of a matrix of memory elements (ZE), each of which can be set in one of the stable states. Such an element is usually a flip-flop or a gate. Main memories with 1,024 bits with an access time of less than 100 nsec, equipped with control circuits, can be fabricated on a single bipolar IC chip. One of the major parts of a memory is the matrix-store, in which the information storage itself is realized. The construction (organization) of a matrix is governed by the manner of accessing (interrogating) the memory elements during read or write operations.

In the structural configuration of a matrix with word access and one decoding step (Figure 3.45a), one line forms a m bit word. The symbols A_1, A_2, ..., A_n in the schematic designate the address buses while P_1, P_2, ..., P_m designate the bit buses. As can be seen from the schematic, the address buses are electrically coupled to each memory element for one word, while the bit buses are coupled to the memory element for one bit of all words. When a signal corresponding to the "1" level is present on the adress bus A_i, the state of each of the memory elements in the word associated with adress A_i can be read from the bit buses, $P_1 \ldots P_m$. If it is necessary to write information into a selected address A_i, depending on the information code, a "1" or "0" signal is fed via the bit buses P_1, P_2, ..., P_m to each of the memory elements A_{i1}, A_{i2}, ..., A_{im}.

The control circuits for the matrix are not shown in the block diagram for the sake of simplicity (a decoder with address drivers, read and write amplifiers), which are incorporated in the IC's to reduce the number of package leads and are fabricated on a single chip along with the matrix circuit.

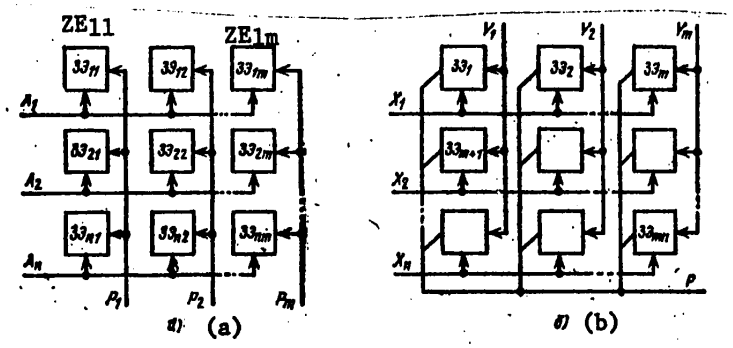


Figure 3.45. Structural configuration of a matrix with word access and single step decoding (a) and a dual coordinate matrix with two decoding steps (b).

Key: ZE = memory element [store location].

In the block circuit diagram of a dual coordinate matrix with two decoding steps (Figure 3.45b), the memory elements are selected by means of the address buses X_1, X_2, ..., X_n and Y_1, Y_2, ..., Y_m. When a signal corresponding to the "1" level is present on address buses X_1 and Y_1, only one memory element will be selected (ZE_1), from which one can read its state via the bit bus P which is common to all elements. When writing a "1" into the selected element via the bit bus, it is necessary to feed in a signal corresponding to the "1" level. This is the organization of a matrix with m-n single bit words.

The simplest memory element is an RS flip-flop, which can be constructed from two inverters (Figure 3.46a). The emitters 1 of the multi-emitter transistors VT1 and VT2 are connected to the address bus A_i, the potential on which in the steady-state is the lowest potential of the circuit. The bit buses P_i and P_j are connected to the emitters 2 of transistors VT1 and VT2 respectively.

A reference voltage common to all of the matrix memory elements is fed to the bit bus P_i. The relationship between the reference voltage, U_{ref}, the voltage U_{bit} which is fed to the bit bus P_j and the voltage U_a which is fed to the address bus, governs the operational mode of the memory element: write, read, and storage of the information. We shall analyze the operation of a memory element in each of the three modes.

The information storage mode is characterized by the relationship:

$$U_a < (U_{ref} = U_{bit}).$$

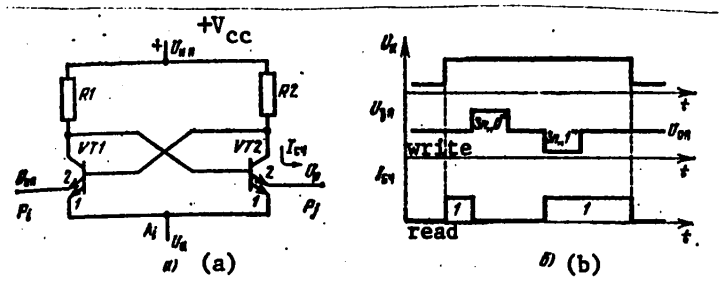


Figure 3.46. Circuit of a memory element using two TTL inverters (a) and the time diagram of its operation (b).

The circuit is in one of the stable states in which transistor VT2 or VT1 is turned on depending on what information was written in beforehand: "1" or "0". The current flows through emitter 1 of one of the transistors, while the emitters 2 are cut off.

We shall consider the read mode. Let a "1" have been written into the RS flip-flop. We shall assume that in this case transistor VT2 is turned on and VT1 is turned off. We take the presence of current in the turned-on transistor to be a "1". In order to relay this information to the bit bus, it is necessary to switch the emitter circuits: turn off the emitter 1 circuit and turn on the emitter 2 circuit, leaving the state of the flip-flop unchanged (following the change of the emitters, transistor VT2 is turned on and VT1 is turned off as before). For this, it is necessary to change the voltage on the address bus so that $U_a > (U_{bit} = U_{ref})$. In this case, the current flowing emitter 2 of turned-on transistor VT2 will flow to the bit bus P_j. The presence of current in the bit bus corresponds to a read "1", and the absence of current in the bit bus (with transistor VT2 turned off and VT1 turned on) defines a read "0".

The write mode depends on the state in which the memory element must be set. If the flip-flop is in state 1 (transistor VT2 is turned on and VT1 is turned off), then to write a "0", it is necessary to feed the potential U_{bit} which exceeds the reference level U_{ref} via the bit bus P_j. In this case the flip-flop shifts to the new state: transistor VT2 cuts off while VT1 turns on. Thus, the write "0" condition has the form: $U_a > (U_{bit} = U_{ref})$ and $U_{bit} > U_{ref}$ while the write "1" condition is $U_a > (U_{bit} = U_{ref})$ and $U_{bit} < U_{ref}$. The operational time diagram of such a memory element is shown in Figure 3.46b.

Thus, for such memory elements using bipolar transistors, the major parameters are the read current I_{sch} [I_r] and the write voltage U_{zp} [U_w].

The data sampling time from a small capacity memory using bipolar TTL circuits can amount to 30 to 40 nsec. An important parameter of the memory is the power consumption. It can be 0.5 to 1.5 mW/bit.

3.7.2. Memory Elements Using MOS Structures

Depending on the type of memory element, memories based on MOS structures can be either static or dynamic. In the first case, a static flip-flop using p-channel MOS transistors serves as the memory element; in the second case, the information is stored in the gate capacitance of an MOS transistor. Memories using MOS structures, just as bipolar transistor memories, can have either word by word or dual coordinate random access.

An exmpale of the simplest memory element circuit, a flip-flop for a word by word access memory, is shown in Figure 3.47a [5]. The flip-flop is formed by transistors VT1 ... VT4. The write and read flip-flop is controlled by means of transistor switches VT5 and VT6. The time diagrams for the operation of such a memory element are shown in Figure 3.47b. In the initial state, the voltage on both bit buses P1 and P^0 is equal to 0, and on the A word bus, the potential is equal to the circuit power supply voltage. In this case, transistors VT5 and VT6 are turned off, since the potential difference between the gates and the sources is less than the threshold voltage in terms of its absolute value. The flip-flop is in one of the stable states.

For example, let transistor VT3 be turned on and transistor VT1 turned off. When writing a "1", a negative signal is fed to the word bus, which changes the voltage on it to zero, and a positive signal is simultaneously fed to the bit bus P^1, which changes the voltage on it to the power supply voltage, V_{cc}. In this case, transistor VT5 turns on, since the potential difference between the gate andthe source becomes negative. The positive signal is fed to the drain of transistor VT1 and to the gate of transistor VT3. The pontential difference between the gate and the source of transistor VT3 becomes less than the threshold voltage, and this transistor turns off. After transistor VT3 turns off, transistor VT1 turns on and a positive voltage is established at its drain, which corresponds to "1" state. The voltage at the drain of transistor VT3 becomes equal to zero.

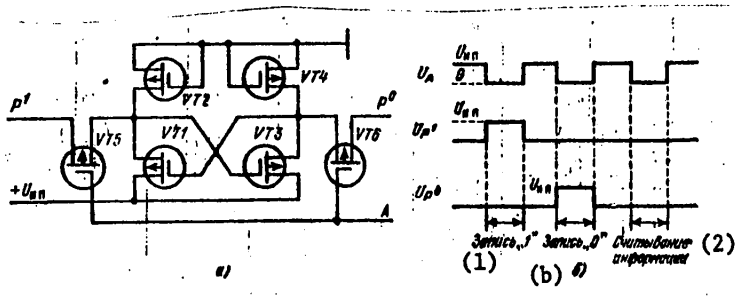


Figure 3.47. Schematic of a memory element for word access memories (a) and the timewise diagram of its operation (b).

Key: 1. "1" write;
2. Information read.

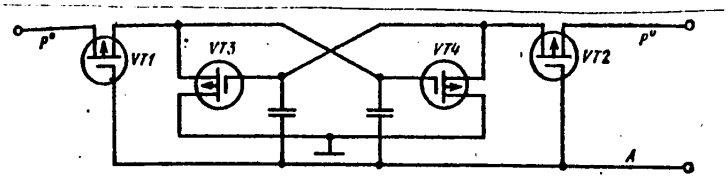


Figure 3.48. Schematic of a memory element for a dynamic memory using p-channel MOS transistor.

To write a "0" into the memory element, it is necessary to feed the voltage V_{cc} to the bit bus P^0 with a zero voltage on the word bus. In this case, the positive voltage, in going to the gate of transistor VT1 through turned-on transistor VT6, cuts off VT1, which leads to transistor VT3 turning on. To read the information previously written into the memory element, it is necessary to feed a negative signal only to word bus, changing the voltage on it to zero. In this case, transistors VT5 and VT6 are turned on and a current which is fed to the appropriate bit bus and then to the read amplifier flows through the transistor which is connected to the point of the flip-flop having a positive potential.

A schematic of a dynamic memory element using p-channel MOS transistors is shown in Figure 3.48 [7].

3.7.3. Memory Elements Using CMOS Transistors

The use of CMOS transistors in integrated circuits makes it possible to substantially reduce the power consumption and boost the speed of memories. A schematic of a memory element of the matrix of a main memory using CMOS transistors is shown in Figure 3.49. Information addressing and writing is accomplished by the direct feed of the logic levels via the X_i, Y_i and D_0, D_1 buses respectively. A memory element is selected by feeding the voltage corresponding to the "1" level via the X-Y buses. When writing a "1" into the selected element, the "0" level is fed on the D_1 bus and the "1" level on the D^0 bus. When writing a "0", a "1" level is fed on the D^1 bus and a "0" level on the D^0 bus. Voltage read is accomplished via the D^1 and D^0 buses; in this case, the read bus, Sch, is connected to "ground".

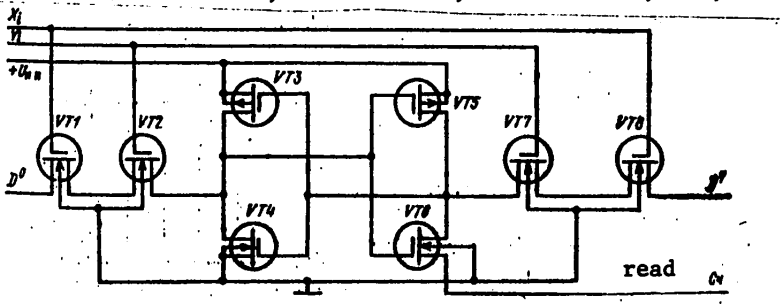


Figure 3.49. Schematic of a memory element using CMOS transistors.

3.7.4. Storage Elements Employing MNOS structures

In all the integrated circuits discussed above, employing bipolar and MOS [metal-oxide semiconductor] transistors, for the purpose of storing information in a storage element the existence of a supply voltage is obligatory. When the power is cut off information is lost. However in a number of cases it is necessary to cut off the power, and in addition the ability to store information with the power cutoff considerably reduces the mean power required by the storage unit.

An integrated semiconductor structure--an MNOS [metal-nitride-oxide semiconductor] transistor--makes it possible to design a storage unit which retains information when the power is cut off. In MNOS transistors, unlike ordinary MOS structures, between the silicon oxide (SiO_2) film and the metal gate electrode is placed a film of silicon nitride, Si_3N_4. The storage of charges in the region of the Si_3N_4-SiO_2 interface makes it possible to store information when the power is cut off for several years.

The film of SiO_2 prevents the transfer of charges in the absence of voltage in the gate or when it is below the threshold value. This capability of a storage element employing an MNOS transistor is responsible for longterm storage of information when the power is cut off.

Information is stored in a memory element based on an MNOS structure by supplying to the gate a certain voltage with a specific sign. When negative voltage of a specific critical magnitude is supplied, at the interface of the silicon nitride and silicon oxide films a charge originates, whose magnitude depends both on the amplitude and length of the voltage pulse.

With this is established a state with a high threshold voltage, $U_{por\ v}$. When positive voltage of a specific critical magnitude is supplied, at the interface a charge originates which lowers the threshold value to a magnitude of $U_{por\ n}$. The difference $U_{por\ v} - U_{por\ n} = \Delta U_{por}$ is called the interthreshold zone (fig 3.50).

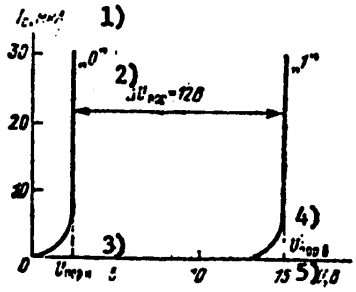


Figure 3.50. Characteristics of a Storage Element Employing an MNOS Structure

Key:
1. I_0, μA
2. $\Delta U_{por} = 12$ V
3. $U_{por\ n}$
4. $U_{por\ v}$, V
5.

When a negative voltage ($U_z = -28$ V) is supplied to the gate of an MNOS transistor, a state is established which is characterized by a high threshold voltage of $U_{por\ v} = 15$ V, corresponding to the "1" level, and with $U_z = +28$ V, a state is established with a low threshold voltage of $U_{por\ n} = 3$ V, corresponding to the "0" level. The existence of an interthreshold zone of $\Delta U_{por} = 12$ V makes it possible confidently to distinguish two states of the storage element. For the purpose of reading out stored information ("1" or "0") to the gate of the MNOS transistor it is necessary to supply a readout voltage, U_{sch}, satisfying the condition $U_{por\ n} < U_{sch} < U_{por\ v}$.

Thus, if $U_{sch} = -(3$ to $5)$ V is supplied, then a storage element in which a "1" ($U_{por\ v} = 15$ V) was entered beforehand will change to the conduction state. And if a "0" was entered beforehand ($U_{por\ n} = 3$ V), the storage element will not conduct. The readout signal can be separated by means of a not too high load resistance connected between the output of the storage element and the ground (in a PZU [permanent memory] with two-coordinate access), or can be determined by the presence of current in the output circuit (in a PZU with word-by-word access).

Information entered in a storage element employing an MNOS structure is stored for a long time when the power is cut off, although at the beginning of the storage period the interthreshold zone is somewhat reduced. The storage properties of MNOS structures are improved in multiple repetition of the readout-readin cycle, which has occasioned a tendency to use them for the purpose of creating permanent memories (PZU's), and not memories with random access. Able to serve as an example of these PZU's are series K519 microcircuits, representing memory matrices for 128 and 256 bits with electrical rewriting of information (fig 3.51). Let us discuss the operation of these circuits in different modes.

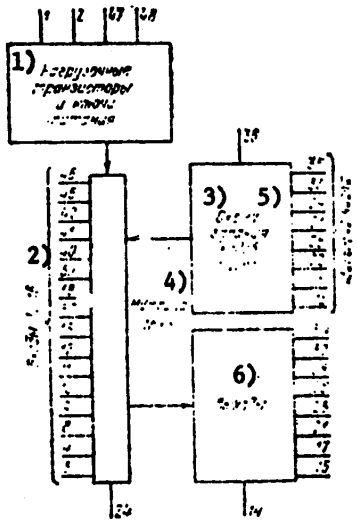


Figure 3.51. Functional Diagram of Type K519RYel Integrated Circuits

Key:

1. Load transistors and power switches
2. Inputs 1 to 16
3. Circuit for setting number codes
4. 16 X 8 matrix
5. Number code buses
6. Outputs

When a "0" is entered (erasure of information), to the "power readout" bus (lead 47) is supplied a -9 V voltage (the voltage in the remaining power buses (leads 1, 2 and 48) equals zero). To all the inputs (Vkh_1 to Vkh_{16}) is supplied a +48 V voltage, and to the "number code," "inhibit entry" (lead 36) and "select crystal" (lead 14), zero voltage. In the

"enter '1'" mode, to the "power readin" (contact 1), "reset readin" (contact 2) and "power readout" buses are supplied voltages of -48, -48 and -9 V, respectively; the voltages in the "reset readout" (contact 48) and "select crystal" buses equal zero. To the inputs (Vkh_1 to Vkh_{16}) is fed a -48 V voltage, and to the "number code" and "inhibit entry" buses, a -9 V voltage. During readout, to the "power readout" and "reset readout" buses are supplied respectively a voltage of -9 and -24 V (the voltage in the "power readin" and "reset readin" buses equals zero). To the inputs of the matrix (Vkh_1 to Vkh_{16}) is supplied a voltage of $U_{sch} = -7$ V, to the "number code" and "inhibit readin" buses, a zero voltage, and to the "select crystal" bus, a -9 V.

3.7.5. Storage Elements Based on "Silicon on Sapphire" Structures

One of the new trends in the creation of circuits for diode storage units is the employment of the technology conventionally called "silicon on sapphire" (KNS [SOS]). The utilization of thin single-crystal films of silicon grown on a sapphire substrate (a material having a crystal structure like that of silicon) makes it possible to produce devices with high radiation resistance, which is explained by the insensitivity of the dielectric substrate (sapphire) to radiation and the small areas of silicon p-n junctions. The area of the p-n junction in these devices is determined by the product of the thickness of the silicon film and the length of the junction line and equals $2 \cdot 10^{-5}$ to $8 \cdot 10^{-5}$ mm. This makes possible low junction capacitance and accordingly high speed of response (to 10^{-9} s).

The small area of the p-n junction makes it possible also to create devices by using the micropower integrated circuit variant. The data published testifies to the feasibility of creating permanent memories with the SOS technology with a high level of integration (of 5120 diodes on a single crystal) distinguished by an access time of 20 ns and dissipated power of 0.06 mW per diode. On the basis of these crystals it is possible to put together PZU's of different capacity, e.g., for 3200 single-bit words (one base crystal), 384 16-bit words (two base crystals) and 2048 20-bit words (nine base crystals). However, this trend for a number of reasons has not yet received sufficient development. The series K139 microcircuits based on SOS have a limited application.

3.7.6. Storage Elements Based on New Materials

Of great interest are developments of storage units based on new materials. An example of such a development is integrated circuits employing switches made of a vitreous semiconductor of the K524RP1 type (fig 3.52a), in the form of a storage matrix of a permanent reprogrammable memory (PPZU), with 256 bits (equivalent to this integrated circuit is a PPZU employing amorphous semiconductors of the C7010 type, made by the Nitron firm in the USA).

This circuit permits 100 rewrite cycles and makes it possible to store information for 10,000 h when the power is cut off. A structural diagram

for the rewriting of information is given in fig 3.52b. Information is read in successively into each storage element. Here the bit bus selected is grounded and to the selected number bus is supplied a plus readin pulse. When a "0" is read in, the $U_{vkh\ [input]}$ = 19 to 30 V , I_{vkh} = 3 to 7 mA , and $\tau_{i\ [pulse]}$ = 10 to 20 ms ; when a "1" is read in, U_{vkh} = 22 V , I_{vkh} = 70 to 100 mA , and τ_i = 3 to 10 μs . When a "1" is read in, readout can take place only 10 μs after termination of the readin pulse. The maximum permissible rewrite rate for a single storage element equals f_{max} = 5 Hz . The current for reading in a "0" is driven by oscillator G_0 through diode VD1 and clipping resistor R_0 (I_{vkh} = 11 mA). The current for reading in a "1" is driven by oscillator G_1 through diode VD2 (I_{vkh} = 100 mA). For the purpose of achieving consistent readin of a "0" and "1" a 16-fold repetition of the readin cycle is made possible.

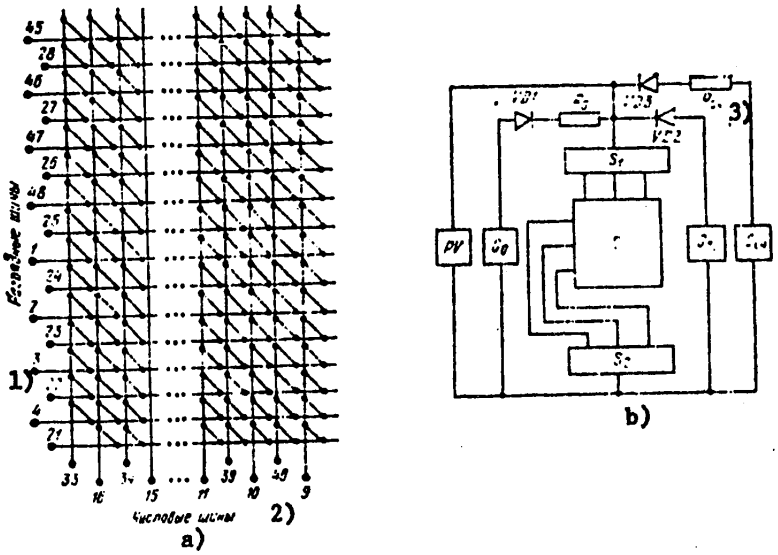


Figure 3.52. Schematic Diagram of Type K524RP1A Integrated Circuit (a) and Structural Diagram for Rewriting Information (b): D--type K524RP1A integrated circuit, S_1--switch for selection of number bus, S_2--switch for selection of bit bus, PV--voltmeter

Key:
1. Bit buses
2. Number buses
3. $R_{sch\ [readout]}$

When information is read out to the selected number bus, a plus pulse with $U_{sch} = 5$ V is supplied from oscillator G_{sch} through clipping resistor $R_{sch} = 6$ kΩ. Reading out can be performed by a pulse of any length greater than the length of $\tau_{sch} = R_{sch} \cdot 0.0035 \cdot C$ (where C is the capacitance of the matrix, equaling 100 pF). The pulse for reading in a "0" or "1," passing through the matrix's storage element (a diode made of a vitreous semiconductor), changes its resistance, which makes it possible in reading out information to produce at the output a voltage of a different magnitude, $U^0_{vykh\ [output]} = 2$ V, $U^1_{vykh} = 3.5$ V.

Able to serve as another example of a storage unit based on new materials is the type 307RV1 integrated circuit, representing the storage matrix of a PPZU with a capacity of eight bits, employing piezoelectric ceramics.

A schematic diagram of a type K307RV1 integrated circuit is shown in fig 3.53. A "1" is read in by supplying to leads 3 to 6 and 9 to 12 a -250 V pulse (τ_1 > 20 ms). A "0" is read in by supplying a 250 V pulse (τ_1 > > 20 ms). Leads 7(8) are hereby connected to ground. For the purpose of reading out recorded information it is necessary with leads 7(8) grounded to supply to leads 14(1) an excitation pulse of $U_{vozb\ [excitation]} \leq \pm 100$ V or $U_{vozb} \geq -50$ V. The read-out signal can have a polarity opposite to the polarity of the excitation pulse. Its magnitude is also determined by the magnitude of the excitation pulse with $U_{vozb} = 10$ V, $U^{1(0)}_{vykh} = \pm 80$ mV. Type K307RV integrated circuits make possible the storage of recorded information for 15 years with the supply voltage cut off. The maximum access rate is 100 kHz. At the present time work is being done to increase the capacity of the matrix to 256 bits.

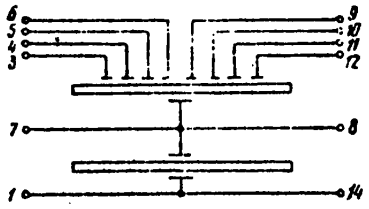


Figure 3.53. Schematic Diagram of K307RV1 Integrated Circuit

3.7.7. Major Series of Memory Unit Integrated Circuits and Their Functional Structure

As was demonstrated above, the key element of the matrix of a memory unit is a storage element, as which is used most often a flip-flop. But the

electrical parameters of a memory unit are not characterized only by the parameters of trigger circuits. The key characteristics of memory unit integrated circuits are the following: capacity, measured by the number of binary units of information (bits) which can be stored in the memory unit; speed of response, determined by the time for access to the memory unit* (speed of response can be characterized in addition by the readin time and readout time); and the power required by a single storage element (in mW per bit) or the power requirement of the entire integrated circuit of the memory unit as a whole. An important characteristic of memory unit integrated circuits is also the degree of integration, expressed as the number of elements or equivalent gates in the package.

The development of memory unit integrated circuits has been proceeding along two lines: Special series of memory units are being created, and memory units are being developed for the purpose of expanding previously developed digital series. For example, in recent years the TTL [transistor-transistor logic] and ESTL [electrical circuit - transistor logic] series of integrated circuits have been expanded, whose makeup includes OZU's [direct-access memory units] with a capacity of 64 bits and random access and control circuits (K155RU2 and K500RU148) and OZU's with a capacity of 256 bits and control circuits (K500RU410), and series of microcircuits employing CMOS [complementary MOS] transistors, whose makeup includes OZU integrated circuits with a capacity of 256 bits and control (564RU2 and K176RU2).

A list of special series of memory unit integrated circuits which have found application in computers for industrial purposes, used in different sectors of the national economy, and their characteristics are given in table 3.23. It should be emphasized that all memory unit integrated circuits developed in recent years contain, in addition to storage matrices, control circuits (decoders, output shapers, etc.), which has made it possible significantly to reduce the number of integrated circuits used for designing a memory unit, and at the same time to reduce its size, to simplify installation and accordingly to improve reliability. As is obvious from table 3.23, the majority of memory unit circuits have been developed on the basis of p-channel MOS technology, with which the unit cell of the memory unit is of small size.

The maximum capacity of OZU's and PZU's is 16 kbits. However in the immediate future must be expected the appearance of memory unit circuits with a capacity of 64 kbits. Of special interest are memory units executed according to the MNOS technology, since they make it possible to store information with the power cut off. For the 519RYe1 and 519RYe2 circuits shown in the table this time equals 2000 h. Great prospects in the area of improving the level of integration, reducing the required power and increasing speed of response are being opened up with further

*Here is meant the time from the instant the access signal is supplied to the instant of termination of the process of reading in or reading out information from the memory unit.

improvement of such circuitry and technological trends as CMOS, n-MOS and MNOS structures.

Table 3.23. List of Series of Memory Unit Integrated Circuits and Their Key Parameters

Условное обозначение микросхемы 1)	Функциональное назначение 2)	Технология 3)	Емкость (организация) бит 4)	Время цикла (считывание/запись), время выборки адреса, считывания информации, мкс 5)	Удельная мощность потребления, мВт/бит 6)	Условное обозначение корпуса 7)	Число элементов в кристалле 8)
КР541РУ1	9) Матрица-накопитель ОЗУ со схемами управления	МОП р-канал 10)	256 (256×1)	11) $t_{ц\,сч}$=1,0 12) $t_{ц\,зп}$=1,0	32) (при обращении) 0,1 (при хранении) 33)	402.16-1	1861
КР541РУ2	Матрица-накопитель ОЗУ со схемами управления	МОП р-канал	1024 (1024×1)	13) $t_{ц\,сч}$=0,7 $t_{ц\,зп}$=0,5 14)	0,1 (при обращении) 0,14 (при хранении)	405.21-1	5326
КР541РУ2	ОЗУ со схемами управления 15)	КМОП 16)	256 (256×1)	17)	0,05	238.16-1	2244
КР541РУ3А КР541РУ3Б	ОЗУ со схемами управления	КМОП	256 (256×1)	$t_{ц\,сч}$=2,5 18) $t_{ц\,зп}$=3,5 (при $C_н$=5пФ)	0,1 (при обращении) 0,005 (при хранении)	402.16-11	2107
КР541РУ4	Матрица-накопитель ПЗУ с электрическим перепрограммированием 19)	МНОП 20)	128 (16×8)	$t_{ц\,сч}$=0,25	0,17 (при обращении) 0,017 (при хранении)	211.18-1	451
КР541РУ5	Матрица-накопитель ПЗУ со схемой частичной дешифрации и электрической перезаписью информации 21)	МНОП	256 (64×4)	$t_{ц\,сч}$=0,3	0,015	241.16-1	923
КР541РУ6	ПЗУ с плавкой перемычкой адреса, потенциальными усилителями и схемой управления 22)	МОП р-канал 23)	1536 (512×8)	$t_{ц\,сч}$=1,3	0,25	402.24-2	1530
КР541РУ7 КР541РУ7А КР541РУ7Б КР541РУ7В КР541РУ7Г	ОЗУ со схемами управления (статического типа) 24)	МОП n-канал	4096 (4096×1)	$t_{ц\,сч}$=0,1 $t_{ц\,сч}$=0,08 $t_{ц\,сч}$=0,07	0,175 (при обращении) 0,045 (при хранении)	210А.22-1	19136
КР541РУ8 КР541РУ8А	ОЗУ динамического типа 25)	МОП р-канал	1024 (1024×1)	$t_{ц\,сч}$=0,65 $t_{ц\,зп}$=0,9	0,1	366.24-1	3485
КР541РУ9 КР541РУ9Б	ОЗУ со схемами управления	МОП n-канал	1024 (1024×1)	$t_{ц\,сч}$=0,45 $t_{ц\,сч}$=0,35	0,33	201.16-11	7142
КР541РУ10 КР541РУ10Б	ОЗУ со схемами управления (динамического типа)	МОП n-канал	16К (16384×1)	$t_{ц\,зп}$=0,29 $t_{ц\,зп}$=0,26	0,04 (при обращении) 0,005 (при хранении) 0,03 (при обращении) 0,004 (при хранении)	210А.16-2	41372
КР541РУ11 КР541РУ11Б	ОЗУ со схемами управления	МОП р-канал	1024 (1024×1)	$t_{ц\,зп}$=0,07 $t_{ц\,зп}$=0,05	0,3 (при обращении)	201А.16-2	7129
КР541РУ12 КР541РУ12Б КР541РУ12В	ОЗУ	ИЛ 26)	4096×1 2×4×1	$t_{ц\,зп}$=0,180	0,13 0,2 0,26	405.21-2	19230
КР541РТ1А КР541РТ1Б	Матрица-накопитель постоянного перепрограммируемого ЗУ 27) 28)	с плавкими связями полупроводник	128 256	$t_{вс}$=5 Гц перезапись 29)		214.45-1	256 512
КР541РП1 КР541РП1Б	Матрица-накопитель ПЗУ со схемами управления, с электрической перезаписью информации (число циклов перезаписи — 30)	ИЛ	2048 1024	$t_{ц\,зп}$=5 мкс $t_{др}$=3000 ч 31)	0,15 0,3	405.21-2	7138 3994

[Key on following page]

Key:

1. Conventional designation of microcircuit
2. Functional purpose
3. Technology
4. Bit capacity (layout)
5. Cycle (readout/readin), readin, address access, and information readout time, μs
6. Specific power requirement, mW/bit
7. Conventional designation of package
8. Number of elements in crystal
9. OZU storage matrix with control circuits
10. p-channel MOS
11. Readout cycle time
12. Readin cycle time
13. Address access time
14. Readin time
15. OZU with control circuits
16. CMOS
17. Readout access time
18. With $U_{i.p}$ [supply voltage] = 5 V
19. PZU storage matrix with electrical reprogramming
20. MNOS
21. PZU storage matrix with partial decoding circuit and electrical rewriting of information
22. PZU with complete address decoding, output amplifiers and "integrated circuit selection" control circuit
23. p-channel MOS
24. OZU with control circuits (of the dynamic type)
25. Dynamic type OZU
26. I^2L [integrated injection logic]
27. Storage matrix of permanent reprogrammable memory unit
28. Vitreous semiconductor
29. Rewrite f = 5 Hz
30. PZU storage matrix with control circuits and electrical rewriting of information (number of rewrite cycles--10^4)
31. Storage time equals 2000 h
32. In access
33. In storage

3.8. Prospects for the Development of Digital Integrated Circuits

Each of the types of digital integrated circuits discussed above (bipolar TTL and ESTL and circuits employing MOS structures, such as p-channel, CMOS, MNOS and SOS) has its advantages and disadvantages, which govern their area of application. Bipolar integrated transistors are suitable for the commutation of relatively high currents, because of which integrated circuits employing these transistors are distinguished by high speed of response, whereby the stray capacitances of interconnections between packages have little influence on the operating speed.

By means of connecting many bipolar integrated circuits, each of which is of moderate complexity, it is possible to create high-speed equipment components. For the purpose of designing computers and components of discrete automatic devices TTL circuits are now used most extensively. Ultrafast equipment is being designed with integrated circuits of the ESTL type.

MOS transistors, because of their practicality, make it possible to achieve considerably greater packaging density of switching circuits in

the integrated structure than do bipolar isolated by a p-n junction or a film of SiO_2. Circuits utilizing MOS transistors arranged on a single crystal can equal whole functional units. This has determined their extensive application in electronic calculators, memory units and microprocessors.

In turn, the steadily increasing requirements from the viewpoint of improving speed of response, reducing the required power and reducing the dimensions and cost of equipment have entailed a quest for new methods making it possible both to improve the operating characteristics of MOS transistors and to increase the functional packaging density of elementary switching circuits made out of bipolar transistors. Let us discuss in greater detail new technological trends in the fabrication of digital integrated circuits.

3.8.1. Integrated Injection Logic

As a development of the very first switching circuit--a direct coupling transistor logic (TLNS) circuit--in recent years has appeared integrated injection logic (abbreviated IIL or I^2L). By means of circuits of the I^2L type it has been possible to overcome the traditional disadvantages of bipolar integrated circuits, i.e., their low packaging density and high dissipated power per gate. In terms of packaging density I^2L circuits even surpass MOS circuits (it is possible to package more than 200 gates on an area of 1 mm^2), and in terms of levels of dissipated power are comparable to CMOS circuits. The high speed of response characteristic of bipolar integrated circuits is furthermore maintained (the propagation delay time per gate reaches 5 ns). The best known variants of base inverter circuits utilizing injection logic of the I^2L type and I^2L type with Schottky diodes are shown in fig 3.54.

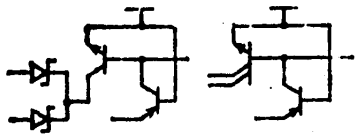


Figure 3.54. Base Inverter Circuits of the I^2L Type

The not too high dissipated power of I^2L circuits is explained by the absence of resistors. The injection of carriers into the area of the transistor's base is accomplished by means of active current generators designed from p-n-p transistors. The high speed of response with low required power is explained by the insignificant stray capacitances, the absence of charge accumulation and the very small difference in logical levels. Gates included in the circuit can be arranged along the injection buses, which

simplifies the topology. In addition, on a single crystal it is possible to unite without difficulty both digital I^2L and analog circuits.

As can be assumed, I^2L circuits with Schottky diodes will make it possible to achieve even higher speed of response (delay time of 0.1 ns) without increasing the power requirement.

3.8.2. MOS Circuits with n-Channels

The restrictions on speed of response characteristic of p-channel MOS circuits can be eliminated by means of n-channel MOS structures. The mobility of electrons in silicon is greater than the mobility of holes, which can make possible a two- to threefold greater switching speed in MOS circuits with an n-channel than in circuits with a p-channel. The latest achievements in technology have made it possible to eliminate the disadvantages of the first n-channel circuits. Utilization of the method of ion implantation and the application in load circuits of a structure with depleted and not enriched channels have made it possible to lower the supply voltage to 5 V, which makes these circuits compatible in terms of electrical levels with TTL's. The use of a separate bias voltage for the substrate has made it possible to increase the threshold voltage, which at the original stage was impermissibly low.

In table 3.24 are given comparative characteristics of the most well known classes of digital integrated circuits, which demonstrate that for the purpose of designing digital equipment integrated circuits of the I^2L, CMOS and n-MOS types would most convenient. Integrated circuits of the CMOS type have already become widespread. The striving for a fundamental improvement in the packaging density of bipolar integrated circuits, as well as for an increase in the speed of response of MOS circuits began after the invention of microprocessors.

Table 2. Key Characteristics of Classes of Digital Integrated Circuits

Characteristics	p-MOS	n-MOS	CMOS	TTL	ESTL	I^2L
Area required for a single gate (10^{-3} mm^2)	5 to 7	3.7 to 5	6.25 to 18.7	12.5 to 37.5	12.5 to 31	2.5 to 3.7
Delay originating in one gate, ns	>100	40 to 100	15 to 50	3 to 10	0.5 to 2	>5
Static dissipated power, mW	2 to 3	0.2 to 0.5	<0.001	1 to 3	5 to 15	<0.2
"Power X speed of response" indicator, pJ	200	10 to 50	3	10	10	<1

[Table continued on following page]

Number of diffusion and ion doping processes	2	3	4	4	4 to 5	3 to 4
Number of masking steps	5	6	7	7	8 to 9	5 to 7

At the present time microprocessor circuits based on I^2L are being developed. In particular, the type K586IK1 integrated circuit (an analog of the type SBP-0400 integrated circuit) represents a microprocessor on a single crystal with an operation execution cycle period of 1 μs and a total power requirement of 150 mW. Also being developed are single-crystal central processors (similar to the Intel type 8080 integrated circuits) utilizing n-channel technology.

A few words should be said about trends in the further development of MOS structures, in particular, DMOS (an MOS transistor fabricated by the method of double diffusion) and VMOS (an MOS transistor with a V-shaped groove). Both these structures make it possible to reduce the length of the channel in an MOS transistor. In DMOS structures this is achieved by carrying out two successive diffusions of impurities with opposite types of conduction. The drift region proves to be depleted and the switching time with such a short channel is considerably reduced.

In VMOS devices the thickness of the source-drain gap is determined by the thickness of the epitaxial or diffusion layer revealed in anisotropic etching. As the result of etching, in diffusion or epitaxially grown films are formed V-shaped grooves which reveal a thin layer with a new formed surface. The substrate becomes the source and the upper diffusion region the drain. The gate is created on the beveled side of the etched groove by means of oxidation and the deposition of a film. Examples of discrete VMOS transistors are devices of the KP901 to K904 type, which have high operating voltages (30 to 100 V), a gain slope of 30 to 100 mA/V, and a drain current of 0.1 to 1 A.

In both designs of these promising MOS structures control of the gain-source distance is accomplished by technological methods and does not depend on the capabilities of photolithography, as in all other methods of fabricating devices. As the result of utilizing the above-mentioned methods it is possible to create MOS devices with a switching delay on the order of 1 ns with voltages of 5 V. This speed of response is comparable to the fastest series of TTL circuits.

In addition to bipolar and MOS circuits, in recent years have appeared devices with charge coupling (PZS's), which combine in themselves two important functional properties--the ability to store information (represented by the charge of mobile carriers), and the ability to transmit it directionally.

The key merits of PZS's as compared with bipolar and MOS circuits are the following: a high degree of integration (up to 150,000 bits/cm^2), high speed of response (dozens of MHz in ordinary PZS's with surface charge transfer and dozens of GHz in PZS's with an ion doped recessed channel), a low power requirement (5 to 10 μW/bit) and basic design and technological simplicity.

However, PZS's require special circuits for linking with bipolar and MOS integrated circuits, which can be numbered among their disadvantages. PZS's come under the heading of devices of the dynamic type and for their operation are required oscillators which form trains of clock pulses. Already created and having found commercial application are shift registers and memory units with random access employing PZS's. For example, the K534IR1 type integrated circuit is in the form of a shift register with a capacity of 16,384 bits with an information transmission rate of 8 Mbits/s, a maximum clock pulse frequency of 2 MHz and a power requirement in the storage mode of 30 μW/bit.

It is to be expected that after the mastery in production of circuits utilizing PZS's they will find extensive application in equipment.

3.9. Microcalculators

As was indicated above, at the present time integrated circuits employing CMOS transistors have become widespread. The complementary technology makes it possible to produce circuits with a high level of integration (up to 10,000 elements on a crystal) and a low static power requirement (to single numbers of microwatts per switch). The increase in the functional complexity of CMOS integrated circuits has made it possible to create in a single crystal complete digital devices of the processor type, and this, in turn, has served as the basis for the development of small electronic keyboard computers (EKVM's)--so-called "pocket" EKVM's, or, in other words, microcalculators.

As an example let us discuss the design principle of a microcalculator of the "Elektronika B3-04" type (fig 3.55).

The input unit is designed for transmitting to the keyboard computer raw data and commands from the keyboard unit. Information in the form of a decimal code enters the decoder input, where it is converted into binary coded decimal code and the coding of commands is carried out.

The synchronization unit generates the necessary trains of pulses controlling the operation of all the keyboard computer's units. It consists of a master oscillator and a set of delay lines (with logical feedback).

The programmable unit generates the required sequence of microcommands depending on the operation key pressed on the input unit.

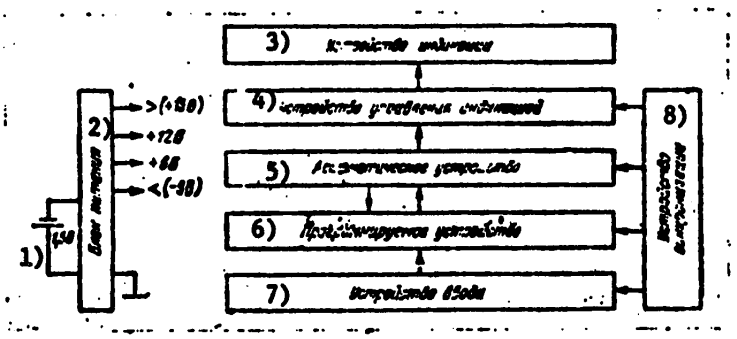


Figure 3.55. Structural Diagrams of "Elektronika B3-04" Type Electronic Keyboard Computer

Key:

1. 1.5 V
2. Power supply
3. Display
4. Display control unit
5. Arithmetic unit
6. Programmable unit
7. Input unit
8. Synchronization unit

The arithmetic unit (AU) makes possible performance of addition, subtraction, multiplication and division operations. It consists of a binary coded decimal sequential adder-subtractor operating in 8-4-2-1 code, dynamic information storage registers and circuits for controlling copying of information and addition.

The display control unit is designed for outputting raw data and the results of computations to the display. The display itself is designed in a keyboard computer of the B3-04 type on the basis of liquid crystals and serves the purpose both of visually monitoring raw data and of registering the results of computations.

The power supply transforms the voltage of the d.c. (1.5 V) chemical element into the following series of voltages: +6 V (for powering the logic section of the computer, which performs all arithmetic operations), +6, +12, +15 and -9 V (for powering the display). This computer has its own synchronizer. The frequency of the master oscillator is f_0 = 100 kHz , and the clock frequency equals $f_t = f_0/3$.

A list of the integrated circuits which are used in a keyboard computer of the B3-04 type and their electrical parameters are presented in table 3.25. The system for controlling the display is executed with integrated circuits of the K145AP1, K145AF1 and K145PP1 type. The K145IP1 circuit enables the performance of all arithmetic operations and conversion of the

data and operation code into binary coded decimal code, and also converts it into the segment code required for the display control system. The K145IP2 integrated circuit serves the purpose of storing operands and results of an operation.

Table 3.25. Integrated Circuits with Which a Keyboard Computer of the "Elektronika B3-04 Type is Designed, and Their Electrical Parameters

Conventional designation of integrated circuit	Functional purpose	Number of elements in crystal	Conventional designation of package	Electrical parameters		
				U_{vkh}, V	U_{vykh}, V	P_{pot}, mW
K145AP1A	Shaper of pulses for controlling segments	378	No GOST*	9.2	9.2	6.6 10.6
K145AF1	Digit selector	12	Ditto	-	18	7
K145PP1A K145PP1B	Display control circuit	642	"	4.6	9.2	6.6 10.6
K145IP1A K145IP1B	Processor	3400	"	4.4	4.6	3.3 5.3
K145IP2A K145IP2B	Storage register	1492	"	4.6	4.6	3.3 5.3
K145PN1	Voltage transformer	4	401.14-2	-	-	5

Note: For the K145PN1 integrated circuit U_{st} = 12 to 13.5 V with $I_i \leq$ $\leq$ 1.5 mA .

The structural diagram for control of the display is illustrated in fig 3.56. It is organized according to the matrix method with the display bits divided into even and odd, which has made it possible to unite like segments of adjacent display bits (1r and 2r, 3r and 4r, 5r and 6r, and 7r and 8r) and to reduce twofold the number of display leads. The "K"

*Not specified in an All-Union State Standard.

(constant) and "-" segments are connected to the common buses of the odd and even bits, respectively. The digit selector generates commands for lighting the even and odd digits.

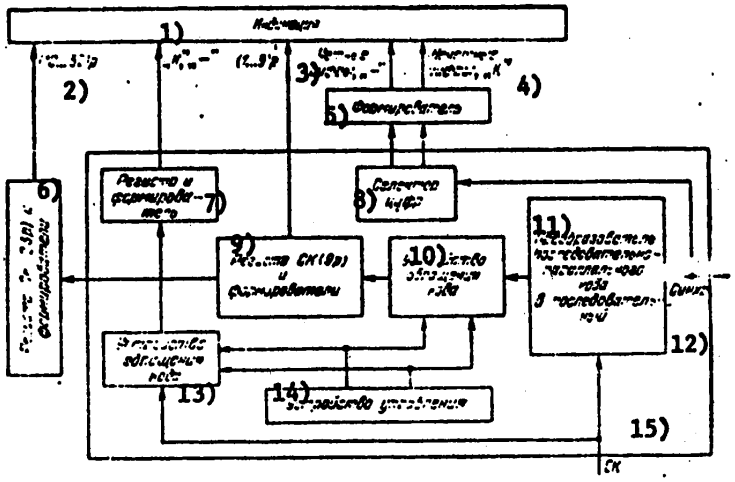


Figure 3.56. Control of Display

Key:

1. Display
2. (10 to 32)r
3. Even digits
4. Odd digits
5. Shaper
6. Segment code (23r) register and shapers
7. Register and Shaper
8. Digit selector
9. Segment code (9r) register and shapers
10. Code access unit
11. Converter of series-parallel code into series
12. Synchronization
13. Code access unit
14. Control unit
15. Segment code

A structural diagram of an integrated circuit of the K145UP1 type is shown in fig 3.57. Its operating half consists of a collection of the following units: an adder-subtractor, a data and command code storage register, a unit for correcting pseudosums and determining the position of the decimal point, a unit for recoding data represented in the decimal system into binary coded decimal code, a unit for coding information for outputting it to segmented displays, a unit for generating control pulses. The operating part performs the processing of information, such as addition, subtraction,

multiplication, division, computation with a constant and code conversion. Here information is circulated through a programmable logic matrix.

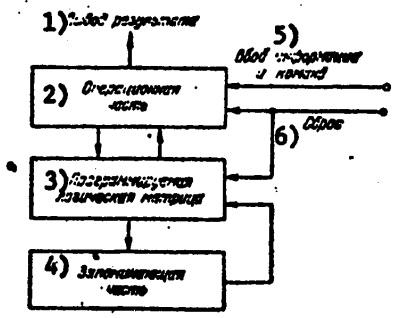


Figure 3.57. Structural Diagram of Processor Employing Integrated Circuits of the K145IP1 Type

Key:

1. Output of result
2. Operating section
3. Programmable logic matrix
4. Storage section
5. Entry of information and commands
6. Reset

The programmable matrix consists of a set of AND and OR gates and can be divided into the following three sections: a switching circuit for the circulation of information in the execution of decisions and coding, an analysis circuit (two dynamic trigger circuits), and a circuit for controlling the storage section.

The storage section is a set of eight dynamic trigger circuits making possible the storage of micro-operations. Micro-operations are formed in relation to the information entered into the keyboard computer, the state of analysis circuits, and the previous micro-operation.

The integrated circuits developed for keyboard computers of the "Elektronika B3-04" type are whole units, implementing, as was demonstrated above, not individual logic functions, but complex arithmetic and logic operations and making it possible to perform the four arithmetic operations and operations with a constant. Other keyboard computers have also been created, developed on the basis of series K145 CMOS integrated circuits (table 3.26).

3.10. Microprocessors

The increase in the degree of integration of integrated circuits and the improvement of their technical and economic characteristics have made it possible with high results to utilize computing equipment in many new areas--from units of industrial equipment and monitoring and test

equipment to cash registers and keyboard computers. The process of the spread of this computer technology has been accelerated considerably with the employment of microprocessors (MP's). In terms of architectural and structural solutions, MP's are similar to the processors of "big" computers the processing of information in which is performed according to a program (or microprogram).

Table 3.26. List and Structural Makeup of Keyboard Computers Developed on the Basis of Series K145 Integrated Circuits

Type of keyboard computer	Conventional designation of integrated circuit used	Functional purpose	No of elements in crystal	Conventional designation of package
B3-18	K145IP12	Processor, I/O control unit for single-crystal engineering calculator	16,000	244.18-1
B3-21	K145IK501 K145IK502 K145IK503	Operating unit whose control PZU is programmed to perform functions in keeping with its design	9,800	244.48-1
	K145IR1	Dynamic shift register for 1024/1008 bits	6,167	209.24-1
	K165GF2	Four-phase pulse clock	188	301.12-1
B3-30	K145IP14-K	Processor, I/O control unit for single-crystal microcalculator utilizing six basic arithmetic operations and a display with field effect liquid crystal indicators	6,000	

The very name "microprocessor" refers to the execution of the processor by employing one or more crystals of a semiconductor microcircuit. Microprocessors are playing the role of the major functional units of a new class of computers, so-called microcomputers, whose distinctive feature is that they are implemented with integrated circuits of improved degrees of integration (the third and fourth). These integrated circuits perform certain simple operations by means of a special-purpose control program (single-program operating mode).

Microcalculators became the preparatory stage in the development of MP's and microcomputers. It is precisely in them that the topological,

circuitry and architectural solutions were worked out which were later widely employed in the creation of the first MP's. Along with program MP's (controlled by microprograms) in recent years integrated circuits have appeared with increased functional complexity, performing different kinds of logical or mathematical processing of information. The algorithm for their operation is determined not by a program but by a functional circuit. These integrated circuits can be called special-purpose microprocessors. In modern microcomputers these special purpose MP's enable the performance of input/output operations concomitantly with the operation of the main MP. However, most widespread have become microprocessors for a broad purpose--controlled by programs or microprograms--which will be discussed below.

3.10.1. Characteristics of a Microprocessor

A microprocessor is a data processing unit consisting of operating and control sections, which can be supplemented with a permanent memory (PZU), which serves the purpose of programming. Thus, an MP is a general-purpose digital electronic unit whose function is assigned by programming.

The first MP's consisted of a single crystal, but experience in using them demonstrated that for the purpose of creating a self-contained system it is necessary to add to such an MP an entire series of digital integrated circuits. Most convenient to use proved to be families of MP's compatible with one another, making up a configuration. These MP configurations (sets) have created the conditions for designing future digital devices by employing new architectural principles, among which can be named the mainline method of organizing different levels of the digital structure, enabling add-on capabilities for computer equipment, a multiprocessor structure, microprogram control of processors, self-containment of peripherals and standardization of a system's units. Practically all modern MP's are developed in configurations. The employment of program facilities in place of the switching of units for the purpose of altering the behavior of a processor has been conducive to considerable improvement in the efficiency of a system.

A typical operating program for an MP consists of a sequence of commands and instruction words, stored in the permanent memory with which the MP is supplied, to the processor. Usually these are programmable PZU's (PPZU's), which make it possible easily to rewrite, which in turn makes it possible sufficiently simply by means of software to enable a microprocessor to be used under new conditions of application, without resorting to individual extensive changes in hardware. Supplying a standard MP with a PZU which can be programmed in different ways makes it possible quickly to develop new designs.

The operating section of an MP enables logical processing of information circulating in the MP itself. These are operations by means of which computations are performed (binary addition, right and left shifts,

complements, etc.). The control section of an MP decodes instruction words and forms signals required for the performance of a specific operation. Each instruction word represents a short program consisting of elementary operations whose sequence is called a microprogram. The sequence of instruction words in keeping with which the control section of the MP operates is called the program. The program is written in the PZU, in which are stored both microprograms and control programs for solving a specific problem. Almost all models of MP's have a fairly great number of supplementary internal registers which serve the purpose of reducing the time for the execution of operations and of forming addresses of greater length than the basic bit configuration of the processor.

In many MP's there is a register sink storage which is used for storing subprograms and tables of interrupts and data. The sink storage consists of a group of connected registers and a counter which serves the purpose of selecting the appropriate register. Registers are cleared in an order which is the reverse of that in which they are filled, which makes it possible to reduce the number of program exchanges between the registers and the main memory, the capacity of the memory required and the time for processing arrays. Information can be processed simultaneously or sequentially.

In supplying MP's with interrupt facilities the possibility appears of combining arithmetic operations and input/output operations, which increases the processor's operating speed. In addition, the operating speed can be increased by the employment of new circuitry design principles based on new technological structures. Whereas the first MP's were developed by employing p- and n-channel MOS transistors with not too high operating speed, in recent times have appeared microprocessors utilizing bipolar integrated structures (I^2L and ESL), which have made possible a considerable increase in operating speed.

Generally an MP, even with the existence of a PZU with an entered control program, is still not a computer, and for the purpose of converting it into a microcomputer it is necessary to furnish it with input/output circuits which control the peripheral equipment. But the capabilities inherent in an MP make it possible to use it in all equipment in which by means of digital equipment it is possible to enable the performance of broad tasks relating to the processing of information according to a preset program. The number of different operations which can be performed by a microprocessor in some models reaches 100, whereby operations are provided for with a double word length and byte-by-byte processing of information.

In recent times, in addition to MP's with a fixed list of instruction words, have appeared MP's with microprogram control, making it possible to change the list of instruction words and control algorithms. With this the flexibility of the processor is increased and the implementation of relatively complex microcommands, e.g., such as a Fourier transform, is simplified. However, for the effective utilization of microprogram control it is necessary that the operating speed of the microcommand storage

be five to 10 times greater than the operating speed of the instruction word storage, since each instruction word is made up of a number of sequentially executed microcommands. The appearance of large-capacity fast PZU's will further the extensive introduction of microprogram control in the structure of MP's.

One important characteristic of MP's influencing their area of application is the word length. MP's in wide use at the current time are divided into three groups: 4-, 8- and 16-bit. The first are used chiefly in microcalculators and automatic cash registers and accounting machines, and the second in data processing systems, and the third in broad-application microcomputers.

As already mentioned above, one of the most important parameters of an MP is its operating speed. The mastery by industry of various circuitry trends has made it possible already today to reach an operating speed of from dozens of thousands to one million to three million brief "register-to-register" operations per second. In particular, for MP's implemented on the basis of p-MOS circuits--80,000 operations/s, n-MOS circuits--400,000 operations/s, CMOS circuits--400,000 operations/s, I^2L circuits--500,000 to 600,000 operations/s, TTLSh [transistor-transistor logic with Schottky diodes] circuits--1.2 million operations/s, and ESTL circuits--3.0 million operations/s.

On the basis of the distinctive features of the design of computers using enhanced-integration integrated circuits (fourth generation computers) and of the thesis of the universality of the employment of MP's for the optimal implementation on their basis of a broad range of computer hardware, it is possible to formulate specifications for microprocessor configurations:

The implementation of an extensive set of information processing algorithms. For this must be accomplished microprogram control, the capability of arbitrarily increasing the bit configuration, the number of general purpose registers, and the microcommand format, and of specialization of a configuration with regard to its basic purpose, and ensurance of functional completeness of a configuration.

Standardization and unification of the architecture, which will make it possible to orient a configuration toward a unified advanced structural design principle for computer hardware. For fourth generation computers this principle can be the reduction of the entire diversity of computer hardware structures to the structure of a processor executed on the basis of functionally complete modules united via mainlines and controlled by means of microprograms. The most constructive concept in the architecture of MP's at the present time is the digital module arrangement accompanied by appropriate alteration of the number of microcommands.

3.10.2. Medium Operating Speed Microprocessor Configuration

A typical microprocessor configuration (MK) enabling the design of digital computer hardware with broad functional capabilities and unified software (fig 3.58) includes hardware and microprogram software. The microprogram software implements a system of instruction words in the form of microprograms, each of which consists of a sequence of microcommands. For the purpose of simplifying the development and debugging of microprograms, they are divided into addressing and operating. This makes it possible to provide the capability of expanding the system of instruction words, economizes on the capacity of the memory, and increases the efficiency of computing facilities.

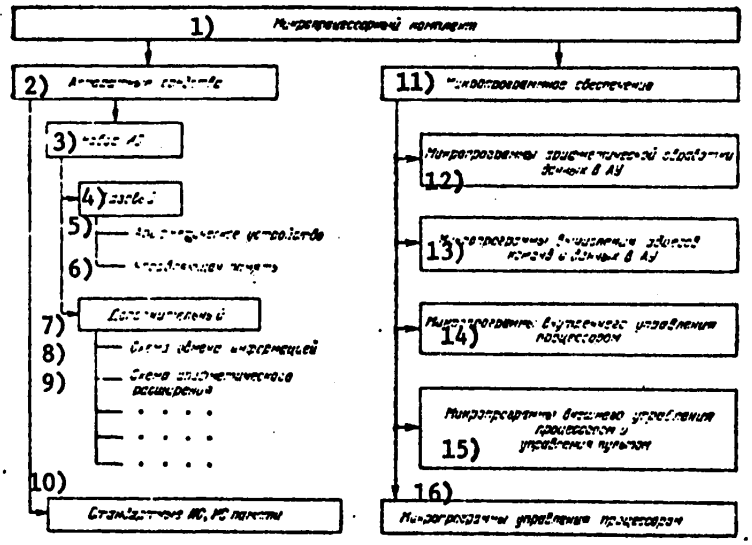


Figure 3.58. Typical Structure of Microprocessor Configuration

Key:

1. Microprocessor configuration
2. Hardware
3. Set of integrated circuits
4. Basic
5. Arithmetic unit (AU)
6. Control storage
7. Supplementary
8. Information exchange circuit
9. Arithmetic expansion circuit
10. Standard integrated circuits, storage integrated circuits
11. Microprogram software
12. Microprograms for arithmetic processing of data in the AU
13. Microprograms for computing addresses of instructions and data in AU

[Key continued on following page]

14. Microprograms for internal control of processor
15. Microprograms for external control of processor and controlling console
16. Microprograms for control of processor

The hardware of a typical microprocessor configuration can be divided into basic and supplementary. The minimal (basic) set of integrated circuits makes it possible to construct various digital computer hardware (TsVS). Included in this set are the circuitry of the arithmetic unit and the control storage. The expanded supplementary set of integrated circuits makes it possible to construct digital computer hardware in the most efficient way and contains a circuit for the exchange of information, a circuit for arithmetic expansion, a circuit of bilateral amplifiers, etc. The structure of the supplementary configuration can vary depending on the distinctive features of the digital integrated circuits designed. As an example let us discuss a microprocessor configuration based on series K587 and K530 integrated circuits (table 3.72).

Table 3.27. Functional Structure of Microprocessor Configuration Based on Series K587 and K530 Integrated Circuits

Conventional designation and description of microcircuit	Technical characteristics	Purpose
	Basic Configuration	
K587IK2 (arithmetic unit)	Four-bit, self-contained microprogram controlled asynchronous digital data processing module	Receipt, direct-access storage, processing and readout of digital and instruction information Designing operating units of digital computer hardware with different bit configurations which are multiples of four
K587RP1 (microprogram control unit)	Self-contained asynchronous former of sequences of 14-bit parallel codes with an information capacity of 64 logical products	Designing microprogram control units with different information capacities, Microcommand generator. Designing very simple digital control circuits (in self-contained mode)
K587IK1 (data exchange unit)	Eight-bit, self-contained microprogram controlled asynchronous	Organization of intra- and extra-processor parallel and sequential exchange of data of different bit

[Continued on following page]

	module for processing and commutating digital information	configurations (multiples of eight), organization of interconnection (interfacing) of processors and channels, designing interrupt units. Used in controllers of peripheral units and for controlling OZU's
K587IK3 (arithmetic expander)	Eight-bit self-contained microprogram controlled asynchronous hardware multiplication module	Performance of hardware multiplication of two operands, shifts, and retrieval of bit codes (operands are whole numbers without a sign or whole numbers in complement form with a sign in the high-order bit); matrix expansion of a bit configuration which is a multiple of eight is possible
	Supplementary Configuration	
K530AP2 (integrated circuits of bilateral amplifier-shapers)	Self-contained asynchronous four-bit bilateral transceiver of digital information	Synchronous and asynchronous transmission of binary information through two-way communications lines; matching of logic levels of TTL and CMOS integrated circuits. Communications line add-on

Note: K587IK1, K587IK2, K587IK3 and K587RP1 microcircuits are made with CMOS structures in a cermet 429.42-1 package, and the K530AP2 microcircuit is based on TTL with Schottky diodes in a 402.16-16 package.

The arithmetic unit (a K587IK2 type integrated circuit) contains 2500 CMOS transistors and includes the following functional units: a parallel arithmetic-logic unit, a block of general-purpose registers, a shifter unit, a state register, an operating register, a microcommand register, three four-bit channels, exchange circuits, an instruction word decoder and a synchronization unit. The arithmetic unit makes it possible to increase the bit configuration to 32 bits, has 168 types of microcommands and makes possible a microcommand execution cycle of 2 μs with a required static power of 10 mW.

The microprogram control unit (a K587RP1 type integrated circuit) contains 6000 CMOS transistors and includes the following functional units: a permanent memory of the "programmable logical matrix" type, a programmable layer of inverters, 13- and 3-bit input registers, a 5-bit sequencing address register, an output microcommand register, a data exchange circuit and a synchronization unit. The microprogram control unit has the following characteristics: number of logical products 64, bit configuration for

input 18 bits, bit configuration for output 14 bits, microcommand access cycle 1.5 μs with required static power of 10 mW. The data exchange unit (a type 587IK1 integrated circuit) contains 3500 CMOS transistors and includes the following functional units: three 8-bit channels, exchange circuits, a trap circuit, 8-bit registers, a logic unit, a commutator, a mode register, a state mask register, a state formation circuit, a microcommand register, a microcommand decoder, a synchronization unit, an original setting circuit, and an expansion flip-flop. The data exchange unit makes it possible to increase the bit configuration to 32 bits, enables the commutation of three mainlines and has 60 types of microcommands. The microcommand execution cycle is 1.5 μs with a required static power of 10 mW.

The arithmetic expander (a 587IK3 type integrated circuit) is constructed with 4500 CMOS transistors and unites the following functional units: two 8-bit channels, a 5-bit channel, an exchange circuit, a 7-bit microcommand register, two 8-bit operand storage registers, two 8-bit operation result storage registers, a 2-bit name code register, a 3-bit position code register, a setting flip-flop, a microcommand decoder, a multiplication unit, a summation unit, a bit code retrieval unit, a state formation unit, a synchronization unit, and an original setting circuit. The arithmetic expander makes it possible to increase the bit configuration to 64 bits, has 64 types of microcommands, has a microcommand execution cycle of 2 μs with a required power of 10 mW.

On the basis of the microprocessor configuration of integrated circuits discussed above can be constructed different computer units of the required bit configuration, microcomputers, and special-purpose computing devices.

In fig 3.59 is shown the structural diagram of a microprocessor implemented with three integrated circuits of the configuration presented above and a conventional illustration of one of the microprocessor's units, the AU. The purpose of the AU's leads is shown in table 3.28. The structural layout of a 16-bit increased-operating-speed microprocessor system (fig 3.60) includes the following: eight type K532IK4 integrated circuits, two type K588RP1 integrated circuits (with unified "stitching"), and 11 series K564 integrated circuits of types TM3, KT3, LYe5, LA7, LA8, TR2 and ID1. The distinctive features of the structure of this microprocessor system are parallel execution of a command in two AU's--an operating (OAU) and indexing (IAU)--whereby the OAU performs operations on operands and the IAU simultaneously prepares the address for operands and instruction words; combining of retrieval from the memory of the next instruction word with fulfillment of the current instruction word; separate address and data buses; and unified addressing of memory cells and registers of external units.

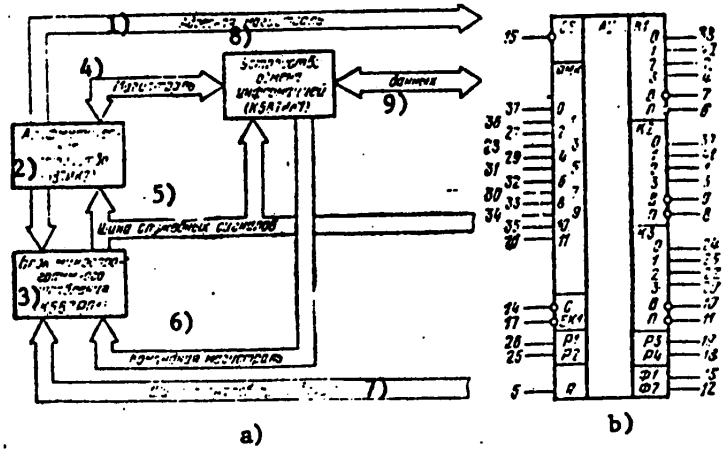


Figure 3.59. Structural Diagram of Microprocessor (a) and Conventional Graphic Representation of Arithmetic Unit (b)

Key:

1. Address mainline
2. Arithmetic unit
3. Microprogram control unit
4. Mainline
5. Working signal bus
6. Instruction word mainline
7. Interrupt signal bus
8. Data exchange unit
9. Data

Table 3.28. Purpose of Leads

Contact	Designation	Description
15	CS	Inputs for permitting reception and performing microcommands
14	C	
37,36,27,28, 29,31,32,30, 33,34,35,16	PMK_0 to PMK_{11}	Inputs of bits of microcommand register
17	EK_1	Input for permitting operation for first information channel
26	P_1	Input of state code of carry circuit to low-order bit
5	R	Input for setting unit to original state
38.40,2,4	Kl_0 to Kl_3	Inputs/outputs of bits of information channel Kl
6	Kl_p	Input/output of signals for termination of reception and outputting information through channel Kl

[Continued on following page]

7	$K1_v$	
39,41,1,3	$K2_0$ to $K2_3$	Inputs/outputs of bits of information channel K2
8	$K2_v$	Input/output of signals for termination
9	$K2^p_v$	of reception and outputting information through channel K2
24,23,22,20	$K3_0$ to $K3_3$	Inputs/outputs of information channel K3
21		Common
11	$K3_v$	Input/output of signals for termination
10	$K3^p_v$	of reception and outputting information through channel K3
19	P_3	Output of state code of carry circuit from high-order bit
		Input/output of state code of carry circuit of:
25	P_2	Low-order bit
18	P_4	High-order bit
13	F_1	Input/output of signal regarding termination of execution of operation
12	F_2	Synchronization input/output
42	$U_{1\ p}$	Power supply

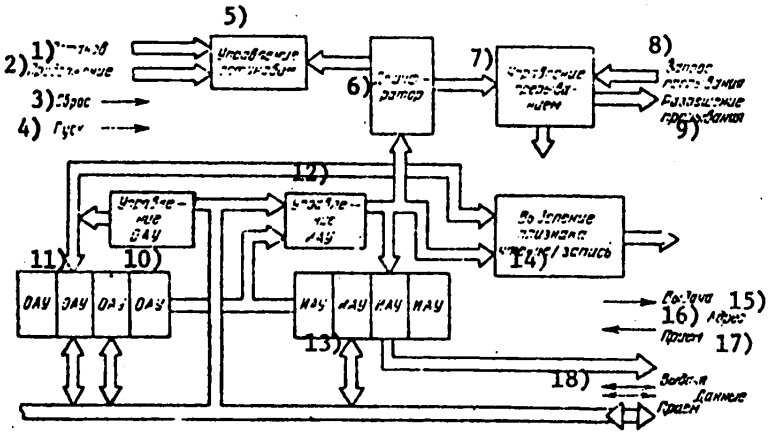


Figure 3.60. Structural Diagram of 16-Bit Microprocessor System Based on a Microprocessor Configuration (MK) Consisting of Series K532, K588 and K564 Integrated Circuits

[Key on following page]

Key:

1. Stop
2. Continue
3. Reset
4. Start
5. Control stop
6. Decoder
7. Control interrupt
8. Interrupt interrogation
9. Interrupt permission
10. Control OAU
11. OAU
12. Control IAU
13. IAU
14. Separation of read/write operation
15. Output
16. Address
17. Reception
18. Data

The key characteristics of the system are as follows: Bit configuration of instruction words, data and addresses--16 bits; number of program accessible registers of processor in OAU--eight operating registers, one working register and one result indicator register, in IAU--eight indexing registers, including an address counter and sink address indicator; number of instruction words distinguished by operation code or type of addressing--about 200; addressing takes place through indexing registers (IR's). Types of data addressing: direct (operand in second word of instruction); according to indexing register, IR; according to indexing register with a consecutive increment; with a preliminary decrement; with modification by the second word of the instruction and with modification by other IR's. In the system there is a single-level vector interrupt and interrupt lock-out. Operating speed for key instructions of the "add register to register" type is 250,000 operations/s, and for instructions of the "add register to memory cell" type, 100,000 operations/s.

The existence of microprograms makes it possible to realize added capabilities (by employing additional circuits), such as a pulsed interrupt with a fixed input address, direct access from an external unit to the memory and access to the memory from the console by employing the processor. A summary of OAU and IAU instructions is given in table 3.29.

The MK's discussed above, based on series K587 integrated circuits, make possible an operating speed of computing operations of the register-register type of 250,000 operations/s with a static power requirement of 10 mW per microcircuit.

3.10.3. Improved Operating Speed Microprocessor Configuration

When it is necessary to improve the operating speed of digital computing systems it is possible to recommend a microprocessor configuration utilizing series K589 and K556 integrated circuits, designed on the basis of transistor-transistor logic with Schottky diodes (TTLSh) (table 3.30). The key electrical parameters of microcircuits of this MK are given in table 3.31. Constructionwise series K589 and K556 integrated circuit MK's have plastic cases (table 3.32).

Table 3.29. List of OAU and IAU Instructions and Their Conventional Designations

1) Команды ОАУ			
2) пересылки, установки	3) смешанные	4) унарные	5) бинарные
(A/P_a)→A, $P_б$	*2 (A*1→$P_б$)	A(A/P_a)+1→A/A,P_a)	(A/P_a)*1$P_б$→A,$P_б$
(M МБ)→A (A/P_a)→A,(M/МБ)	A+P_a+P→A AP_a—3м→A	(M/МБ)+1→A A+1→A, (M/МБ)	A*1$P_б$→A (M/МБ)*1$P_б$→A
РП(→ | ←)A	A+P_a→A	P_a+1→A,P_a,(M/МБ)	A*1 $P_б$→(A/A, $P_б$), (M/МБ)
E→A, РП (0, —1) →A (0, 1) →T		*2(A/P_a)→A	

6) Команды НАУ		
пересылки, установки	7) условные переходы	8) системные
K→P_a	9) Условный переход по (T) →(0, 1)	10) Разрешение/запрещение прерывания
P_a+K→P_a	Конец цикла 12)	Останов 11)
13) P_a(→ | ←) стек // P_a(+1—)1→P_a		

Conventional designations and abbreviations: → --allocation operator; | --exclusive OR; A --OAU storage cell (working register); R_a and R_b -- operating register No a and b (a, b = 0 to 7); R_v --indexing register No v (v = 10 to 17); RP --result indicator register, consists of four flip-flops: R , Z , P and M ; Zm --borrow, Zm = 1 - R ; M --mainline; |←) MB --exchange of M with rearrangement of bytes; Ye --4-bit constant from instruction word field; K --second word of instruction; sink--region of memory addressed through address indicator has been drained; *1--general designation of the operations + (addition), - (subtraction), ∧ (logical multiplication), V (logical addition) and + [as published]

[Continuation and key on following page]

(non-equivalence); *2--general designation of the operations inversion, LL/LP (logical shift left/right by one bit) and TsL/TsP (cyclic shift left/right one bit).

Key:
1. OAU instruction words
2. Copying, setting
3. Mixed
4. Unary
5. Binary
6. IAU instruction words
7. Conditional transfers
8. System
9. Conditional transfer with regard to
10. Interrupt permission/inhibition
11. Stop
12. End of cycle
13. Sink

Table 3.30. Structure of Improved Operating Speed MK Utilizing Series K589 and K556 Integrated Circuits

Description	Type	Analog
Microprogram control unit	K589IK01	3001 Intel
Central processor element	K589IK02	3002 Intel
Accelerated carry circuit	K589IK03	3003 Intel
Multimode buffer register	K589IR12	3212 Intel
Priority interrupt unit	K589IK14	3214 Intel
Bus shaper	K589AP16	3216 Intel
Bus shaper with inversion	K589AP26	3226 Intel
Programmable permanent memory	K556RYe4	-

Table 3.31. Key Electrical Parameters of MK Microcircuits Employing Series 589 Integrated Circuits

Parameter	K589IK01	K589IK02	K589IK03	K589IR12	K589IK14	K589AP16	K589AP2
Maximum static power requirement, $P_{mW, not\ max}$, mW, not greater than	900	950	650	650	650	650	650
"0" output signal, U^{0}_{vykh}, V, not >	0.5	0.5	0.5	0.5	0.5	0.5 (outputs C_1 to C_4) 0.7 (outputs B_1 to B_4)	0.5 0.7

[Continued on following page]

"1" output signal, U^1_{vykh}, V, not <	2.4	2.4	2.4	3.65	2.4	3.65 (outputs C_1 to C_4) 2.4 (outputs B_1 to B_4)	3.65 2.4
Length of cycle, t_{ts}, ns	≥85	≥100	-	-	≥80	-	-
Pulse length, τ_i, ns	≥30	≥33	-	≥25	≥20	-	-
Time of delay in propagation of signal from input X_i to output Y_i, $t_{zd\ r.sr}$, ns	16 to 30	14 to 48	-	20	15 to 100	≤25 to 30	≤25
Group carry time, $t_{p\ g}$, ns (typical)	-	-	10	-	-	-	-
Ripple-through carry, $t_{p\ s}$, ns (typical)	-	-	13	-	-	-	-

[Continued on following page]

Notes: 1. Values of static parameters are indicated in the temperature range of T = -10 to +70°C and with a power supply voltage of 5 V ± 5 percent. 2. Values of dynamic parameters are indicated at T = 25°C and at the nominal voltage of the power supply.

Table 3.32. Types of Series K589 Cases

Type of integrated circuit	Conventional designation of case
K589IK01	230.40-1
K589IK02	247.28-1
K589IK03	247.28-1
K589IR12	239.24-2
K589IK14	239.24-2
K589AP16	238.16-2
K589AP26	238.16-2
K556RYe4	238.16-2

The MK discussed is intended for designing high-speed controllers (control units) with different types of organization, having a control pulse output rate of up to 10 MHz. With it it is possible to construct micro- and minicomputers for different purposes with a number of operations of the register-register type of up to one million operations/s. Let us briefly consider each of the integrated circuits included in the structure of this MK.

The microprocessor controller (BMU) controls the sequence for accessing microinstructions from the microprogram memory, which is constructed as a main memory, read-only memory or programmable ROM, as well as the carry and forward and return shift data from the central processor unit; and in conjunction with the priority interrupt controller provides the interrupt capability. The microprocessor controller executes the following functions: receives the 8-bit instruction operation code, the 9-bit microprogram memory address, the return address which feeds 7-bit microprograms from the memory; performs 11 control functions for the next microinstruction address, including three flag signal branch functions (flags); performs eight control functions for display logic (control of the flags), including four flag set and four flag feed functions; it has outputs with three states and an open collector.

The microprocessor controller controls the sequence for selecting microinstructions from the microprogram memory and three flag registers, which are used for organizing conditional branches in accordance with indicators generated by the CPU or other devices, as well as for the storage and subsequent output of these indicators.

Also included in the functions performed by the microprocessor controller are the servicing of the microinstruction address register, the selection of the next microinstruction based on the contents of the microinstruction register, data decoding and checking for data incoming from several input trunks for the determination of the sequence of microinstruction execution; the storage and checking of data transmitted from the CPU data file; the control of the shift and transmission of input data to the CPU data array; the control of microprogram level interrupts; direct addressing of standard ROM's and PROM's as well as the capability of addressing microinstructions.

A block diagram of the microprocessor controller (a K589IK01 integrated circuit) (Figure 3.61) includes a nine-bit microinstruction address register (RAMK) and the corresponding trunks; a four-bit instruction code register (RK) and two flag registers. The conventional designation of the microprocessor controller is shown in Figure 3.62, while the functions of its leads are given in Table 3.33.

The logic for the next microinstruction address of the microprocessor controller provides for the execution of unconditional and conditional branch functions. These functions are used to realize unconditional or conditional branch operations as part of each microinstruction (each microinstruction usually contains a branch operation field which defines the branch instruction and consequently, the next microinstruction address).

To minimize the number of leads of the microprocessor controller and simplify the logic for the next address, the address file array of microprograms is set up as a two dimensional (matrix) array. Each address of a microinstruction corresponds to a matrix element at the intersection of a particular row and column. Thus, a 9-bit microinstruction address is defined by two addresses: the row address (the five high order digits) and the column address (the four low order digits). Consequently, the address matrix can contain a maximum of 32 row addresses and 16 column addresses: 512 addresses in all.

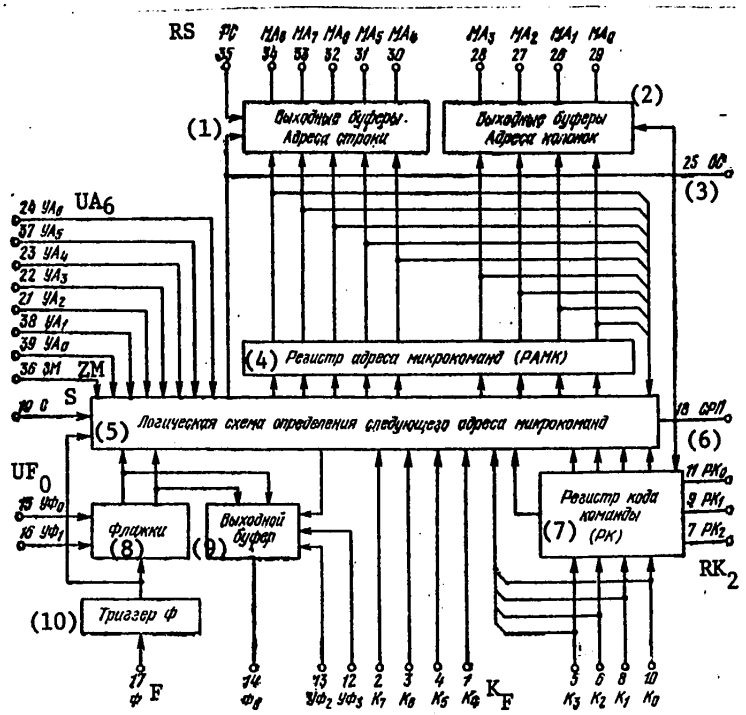


Figure 3.61. Block diagram of a microprocessor controller (K589IK01 integrated circuit).

Key:
1. Output buffers for the row addresses;
2. Output buffers for the column addresses;
3. Common gating input;
4. Microinstruction address register (RAMK);
5. Logic circuitry for determining the next microinstruction address;
6. Interrupt enable gating output;
7. Instruction code register (RK);
8. Flags;
9. Output buffer;
10. Flip-flop F;
[See Table 3.33 for lead functions]

The next-address logic of the microprocessor controller makes extensive use of this two dimensional addressing scheme. For example, one can unconditionally branch the the control by means of one function from any point in the matrix defined by its own row and column to another point in the matrix with a new value of the row and column. However, it is impossible to branch the control to any point in the address matrix. In fact, for each given address (matrix element), there exists a fixed subset of microinstruction addresses which can be selected as the next

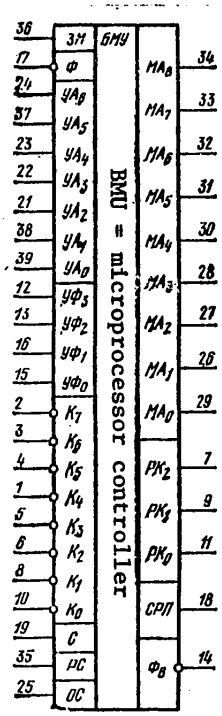


Fig. 3.62. Schematic symbol of BMU and designation of the leads (K589IK01 IC).

address. These addresses, to which branching is possible, are called the branch set. Each type of branch function of the microprocessor controller has its own set of branches (Table 3.34).

The 10 diagrams shown in Figure 3.63 illustrate the set of branches for the 11 functions of the microprocessor controller. The branch functions are located at address 342 (shown with an X). The addresses, one of which can be chosen as the next address, are indicated by the black squares.

The logic scheme for feeding flags to the microprocessor controller provides for storing the current value of the tag fed to the input F as well as feeding it out to the output F_V (Table 3.33). The two different groups of control functions for the flags are called the flag output and set instructions.

The flag circuitry contains three flip-flops, designated as the C flag, Z flag and a simple latch flip-flop, F, which stores the current state of the indicator fed to the input F. The flag circuit can be used in conjunction with the carry and shift circuits of the CPU array for the realization of arithmetic and shift microinstructions. The flag control functions and load functions are shown in Tables 3.35 and 3.36 respectively.

We analyze the branching instructions of the microprocessor controller. The branching functions of the microprocessor controller are chosen depending on the signals at the seven input buses UA_0 ... UA_6. Using the leading edge of the sync signal, the nine bit microinstruction address generated by the next address logic is loaded into the microinstruction address register. This microinstruction address is fed out from the microinstruction address register to the microinstruction memory via the nine output buses MA_0 ... MA_8. The outputs of the microinstruction addresses are broken down into the row and column address outputs as follows: MA_8 ... MA_4 are the row addresses and MA_3 ... MA_0 are the column addresses.

Corresponding to each address control function is its own combination on the functional input buses UA. From 3 to 5 bits of this code combination define the kind of function. The format and coding of the functions are given in Table 3.34. A detailed description of each of the 11 branch functions follows below. The following symbols are used to indicate the addresses of the rows and columns: *STRn* is the five-bit address of the next row; *KOLn* is the four-bit address of the next column; *n* is the decimal number of the row or column.

We shall analyze the unconditional branches of the microprocessor controller. The current microinstruction address, i.e. the contents of the microinstruction address register prior to the arrival of the leading edge of the sync pulse train, and some of the bits from the code on the UA buses, is used to generate the next microinstruction address in accordance with an unconditional branch operation.

TABLE 3.33 Designation of the Leads of the Microprocessor Controller

Contact	Designation	Function	Type of Output	Active Logic Level
1...4	$K_4...K_7$	Inputs for the first part of an instruction	-	"0"
5,6,8,10	$K_0...K_3$	Inputs for the second part of an instruction	-	"0"
7,9,11	$RK_2...RK_0$	Register second bit outputs	Open collector	-
12,13	UF_3, UF_2	Control inputs for flag entry and storage	-	"1"
14	F_v	Indicator output	Three states	"0"
15, 16	UF_0, UF_1	Inputs for the control of flag feed-out	-	"1"
17	F	Indicator [tag] input	-	"0"
18	SRP	Interrupt enable gating output	Conventional output	"1"
19	S	Synchronization input	-	"1"
20	-	Common	-	-
21...24, 37...39	$UA_0...UA_6$	Control inputs for the microinstruction address register	-	"1"
25	OS	Common gating input	-	"1"
26...29	$MA_0...MA_3$	Outputs for the microinstruction address column	Three states	-
30...34	$MA_4...MA_8$	Outputs for the microinstruction row address	Three states	-
35	RS	Enable input for generating the row address	-	"1"
36	ZM	Input for loading the microinstruction address	-	"1"
40	-	Power	-	-

TABLE 3.34 Address Control Functions for the Microprocessor Controller (K589IK01 Integrated Circuit)

Symbol Обозначение	Name Название	(1) Состояние управляющих входов							(2) Адрес следующей строки					(3) Адрес следующей колонки			
		yA_6	yA_5	yA_4	yA_3	yA_2	yA_1	yA_0	MA_8	MA_7	MA_6	MA_5	MA_4	MA_3	MA_2	MA_1	MA_0
ICC	(4) Переход в текущей колонке	0	0	y_4	y_3	y_2	y_1	y_0	y_4	y_3	y_2	y_1	y_0	M_3	M_2	M_1	M_0
IZR	(5) Переход в нулевую строку	0	1	0	y_3	y_2	y_1	y_0	0	0	0	0	0	y_3	y_2	y_1	y_0
ICR	(6) Переход в текущей строке	0	1	1	y_3	y_2	y_1	y_0	M_8	M_7	M_6	M_5	M_4	y_3	y_2	y_1	y_0
ICE	(7) Переход в текущей колонке в группе адресов строк	1	1	1	0	y_2	y_1	y_0	M_8	M_7	y_2	y_1	y_0	M_3	M_2	M_1	M_0
IFL	(8) Переход по содержимому триггера Φ	1	0	0	y_3	y_2	y_1	y_0	M_8	y_3	y_2	y_1	y_0	M_3	0	1	Φ
ICF	(9) Переход по содержимому триггера C	1	0	1	0	y_2	y_1	y_0	M_8	M_7	y_2	y_1	y_0	M_3	0	1	C
IZF	(10) Переход по содержимому триггера Z	1	0	1	1	y_2	y_1	y_0	M_8	M_7	y_2	y_1	y_0	M_3	0	1	Z
IPR	(11) Переход по содержимому регистра команд	1	1	0	0	y_2	y_1	y_0	M_8	M_7	y_2	y_1	y_0	PK_3	PK_2	PK_1	PK_0
ILL	(12) Переход по левым разрядам регистра команд	1	1	0	1	y_2	y_1	y_0	M_8	M_7	y_2	y_1	y_0	0	1	PK_3	PK_2
IRL	(13) Переход по правым разрядам регистра команд	1	1	1	1	1	y_1	y_0	M_8	M_7	1	y_1	y_0	1	1	PK_1	PK_0
IPX	(14) Переход по разрядам команды K_4—K_7	1	1	1	1	0	y_1	y_0	M_8	M_7	M_6	y_1	y_0	K_7	K_6	K_5	K_4

Notes: Y_i [U_i] are the data on the YA_i [UA_i] bus; K_i are the data on the i-th K bus; M_i are the data in the i-th bit of the microinstruction address register; F, C and Z are the contents of the F, C and Z flip-flops respectively; RK_i are the data in the i-th bit of the instruction register (RK).

Key:
1. State of the control inputs;
2. Address of the next row;
3. Address of the next column;
4. Branch in the current column;
5. Branch to the zero row;
6. Branch in the current row;
7. Branch in the current column in the group of row addresses;
8. Branch in accordance with the contents of flip-flop F;
9. Branch in accordance with the contents of flip-flop C;
10. Branch in accordance with the contents of flip-flop Z;
11. Branch in accordance with the conents of the instruction register;
12. Branch in accordance with the left bits of the instruction register;
13. Branch in accordance with the right bits of the instruction register;

[Key to Table 3.34, continued]:

14. Branch in accordance with the K_4 - K_7 instruction bits.

TABLE 3.35. Flag Control Functions

Type	Designation	Function	UF_1	UF_0
Input to the flag feed circuit	SCZ	Set the C and Z flags in accordance with the F output	0	0
	STZ	Set the Z flag in accordance with the F input	0	0
	STC	Set the C flag in accordance with the F input	1	0
	HCZ	Store the C and Z flags	1	1
			UF_3	UF_2
Output of the flag feed circuit	FFO	Feed "0" to the F_V output	0	0
	FFC	Feed flag C to the F_V output	0	1
	FFZ	Feed flag Z to the F_V output	1	0
	FFI	Feed "1" to the F_V output	1	1

TABLE 3.36 Load Function

ЗМ ZM	(1) Адрес следующей строки					Адрес следующей колонки (2)			
	MA_8	MA_7	MA_6	MA_5	MA_4	MA_3	MA_2	MA_1	MA_0
0	See Table 3.34 см. табл. 3.34								
1	0	K_8	K_9	K_1	K_0	K_7	K_6	K_5	K_4

Key: 1. Address of the next row;
2. Address of the next column;

ZM = microinstruction address load input.

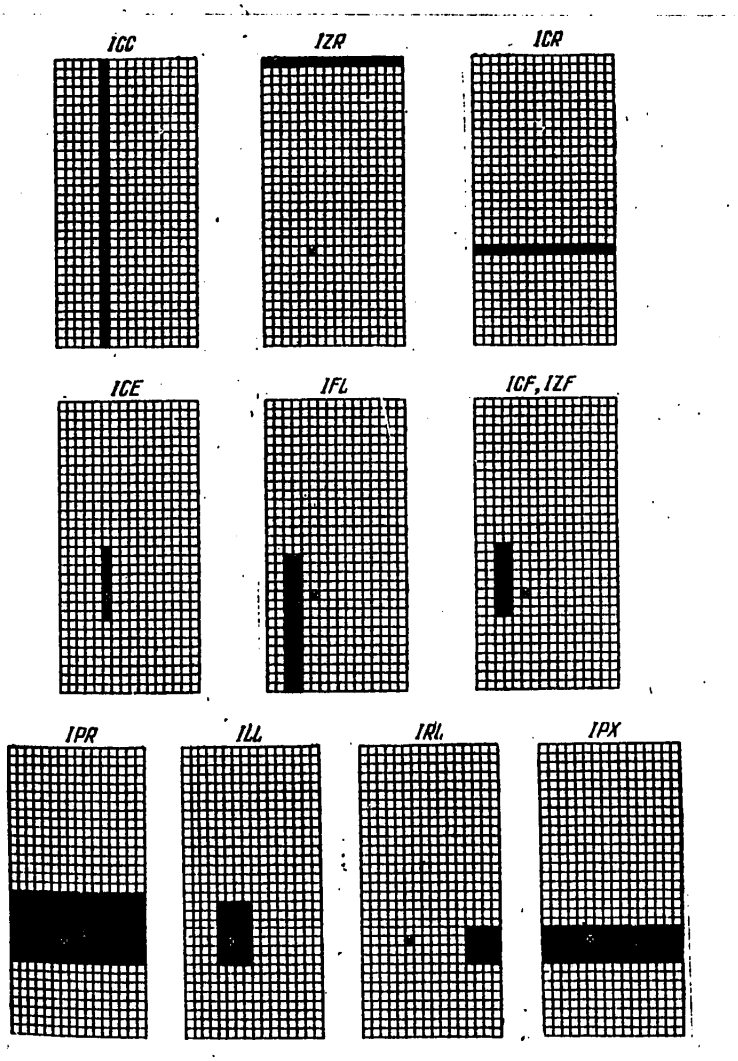


Figure 3.63. Diagrams of the address control function branches.

The unconditional branches and their characteristics are enumerated below.

ICC: branch in the next column; the UA_0 ... UA_4 are used to specify the next microinstruction address; the current column is defined by the MA_0 ... MA_3 outputs;

IZR is the branch to the zero row; the UA_0 ... UA_3 bases are used to specify the next microinstruction address in the STR_0 row;

ICR is a branch in the current row; the UA_0 ... UA_3 buses are used to specify the next microinstruction address in the current row, which is defined by the MA_4 ... MA_8 outputs;

ICE is a branch in the current column in the group of row addresses and the feeding of the RK [instruction code register] contents to the RK_0 ... RK_2 outputs; the UA_0 ... UA_2 buses are used to specify the next microinstruction address in the group of row addresses defined by the contents of buses MA_7 and MA_8; the current column is defined by the contents of the MA_0 ... MA_3 buses. The synchronous output feed of the contents of the RK instruction code register to the RK_0 ... RK_2 outputs is accomplished at the same time.

We shall analyze the flag conditional branches of the microprocessor controller. A portion of the address of the current microinstrucation, the contents of the selected flag (or flip-flop F) and some of the code bits on the UA buses are used to generate the next microinstruction address in accordance with the contents of the flag flip-flops. The conditional branches and their characteristics are enumerated below.

IFL is a conditional branch based on the contents of flip-flop F. The contents of the UA_0 ... UA_3 buses are used to specify the next microinstruction address located in the current of row addresses, which is defined by the contents on the MA_8 bus. If the current microinstruction address belongs to the group of columns KOL_0 ... KOL_7, defined by the contents on the MA_3 bus, then the next microinstruction address, depending on the contents of the flip-flop F, will be found in columns KOL_2 or KOL_3. If the bus MA_3 defines the association of the current address with the group of columns KOL_8 ... KOL_{15}, then the next microinstruction address, depending on the contents of flip-flop F, will be located in columns KOL_{10} or KOL_{11}.

ICF is a conditional branch based on the contents of flag C. The contsnts of the buses UA_0 ... UA_2 are used to specify the next microinstruction address located in the current group of row addresses, defined by the contents on the MA_7 and MA_8 buses. If the current microinstruction address belongs to the KOL_0 ... KOL_7 group of columns, defined by the contents on the MA_3 bus, then the next microinstruction address, depending upon the value of flag C, be located in column KOL_2 or KOL_3. If bus MA_3 defines the association of the current address with the group of columns KOL_8 ... KOL_{15}, then the next microinstruction address, depending on the value of the flag C will be located in column KOL_{10} or KOL_{11}.

IZF is a conditional branch based on the contents of flag Z. It is the same as the branch in accordance with the contents of flag C, but depends on the value of the flag Z.

We shall consider the conditional branches in accordance with the contents of the K_4 ... K_7 buses and the instruction register. The data on the K_4 ... K_7 buses, a part of the current microinstruction address and several bits of the code on the UA buses are used to generate the next microinstruction address in accordance with the contents of the K_4 ... K_7 buses. The data stored in the instruction register, part of the current microinstruction address and several bits of the code on the UA buses are used to generate the next microinstruction address in accordance with

the instruction register RK. The characteristics of these branches are given below.

IPR is a conditional branch in accordance with the contents of the instruction register RK. The UA_0 ... UA_2 buses are used to specify the row of the next microinstruction address, which is found in the current group of row addresses defined by the contents of buses MA_7 and MA_8. Four bits stored in the RK instruction register are used to specify the column address of the next microinstruction.

ILL is a conditional branch in accordance with the left bits of the instruction register. Buses UA_0 ... UA_2 are used to specify the row address of the next microinstruction, which is found in the current group of row addresses, defined by the contents on the MA_7 and MA_8 buses. The contents on the RK_2 and RK_3 are used to specify the column address of the next microinstruction.

IRL is a conditional branch in accordance with the right bits of instruction register RK. The information on the UA_0 and UA_1 buses is used to specify the row address of the next microinstruction, which is located in the current group of addresses of the row defined by the contents of the MA_7 and MA_8 buses. The information on the RK_0 and RK_1 buses is used to specify the address of the column of the next microinstruction.

IPX is a conditional branch in accordance with buses K_4 ... K_7 and the loading of the instruction register RK. The data on buses UA_0 and UA_1 are used to specify the row address of the next microinstruction which is located in the current group of row addresses determined by the information on buses MA_6 ... MA_8. The code on the K_4 ... K_7 buses is used to specify the column address of the next microinstruction. Moreover, the information from the K_0 ... K_3 buses is written into the instruction register using the leading edge of the sync pulse train.

We shall analyze the flag control functions. The type of flag control functions in the microprocessor controller is selected depending on the signals at the four input buses, designated UF_0 ... UF_3.

The data at the input is stored in the F flip-flop during the low level sync series ("0"). The contents of the F flip-flop are loaded into the C and/or Z flip-flop based on the leading edge of the synchronization pulse.

SCZ sets the C and Z flags in accordance with the F input (rewrites the signal from the input F). The value of the F input is assigned to both flags.

STZ sets the Z flag in accordance with the F input. The value of the F input is assigned to the flag Z. The C flag does not change.

STC sets the C flag in accordance with the F input. The value of the F input is assigned ot the flag C. The Z flag does not change.

HCZ stores the C and Z flags. The value of the C and Z flags does not change.

The flag feed control functions given below define the value of the signal which is fed out to the "flag output" line F_V.

FFO feeds "0" to the output F_V. A "0" is set at the F_V output.

FFC feeds the C flag to the F output. The contents of flag C is produced at the F output.

FFZ feeds flag Z to the F_V output. The contents of flag Z appears at the F_V output.

FFI feeds the value "1" to the F_V output. A "1" is set at the output.

We shall analyze the load function and the interrupt gating. The signal corresponding to the multiprocessor controller load function is fed to the input bus for loading the microinstruction, ZM. If the "1" level appears on the microinstruction load bus, then with the appearance of the leading edge of the sync series pulse, the data is loaded from the K_0 ... K_7 buses into the microinstruction address register (RAMK). The contents of the K_4 ... K_7 buses are loaded into the microinstruction address register flip-flop with the MA_0 ... MA_3 outputs, while the contents of the K_0 ... K_3 buses are loaded into the microinstruction address register flip-flops by the MA_4 ... MA_7 outputs. The highest order digit MA_8 of the microinstruction address register is set to "0". In this case, the digits of the microinstruction address register specify one of 16 possible column addresses by means of outputs MA_0 ... MA_3. Correspondingly, the microinstruction address register bits from the outputs of MA_1 ... MA_7 specify one of the first 16 row addresses. The interrupt enable gating is fed from the microprocessor controller to the corresponding output line, designated as the SRP. The active state (high level) is set on the line in the case where upon the ICC branch instruction control is transfered to column *KOL*15.

Usually, the signal from the SRP [interrupt enable gating] bus of the microprocessor controller is fed to the input SRP bus of the priority interrupt controller (BPP). The priority interrupt controller can respond to the interrupt by feeding a "0" level out to the RS [row address enable output] of the microprocessor controller, which blocks the feed of the next selected row address from the microprocess controller. Then, during the feed-out of the new address of the microinstruction to the row address line, one can supply the address from without, avoiding the multiprocessor controller, something which makes it possible for the microprogram to shift over to the input of the interrupt processing program. The changed row address which is transmitted to the address lines of the microinstruction memory, does not influence the contents of the microinstruction address register. Thus, the next branch function will employ the row address in the microinstruction address register, and not the changed row address. We will note that the load function always blocks the branch functions on the UA_0 ... UA_6 buses. However, it does not block the output enable for the contents of the instruction register to the RK_0 ... RK_2 buses as well as the receive enable in the instruction register from the contents of the K_4 ... K_7 buses when the ICE and IPX functions respectively are present on the UA buses. Morever, enabling of the interrupt gating and all of the flag control functions are not inhibited via the microinstruction load bus/

The Central Processor Unit (CPU). This unit takes the form of a two-bit processor section of a data processor; it has 40 types of microinstructions and provides for

the execution of the following functions: arithmetic operations in a complentary binary code, AND, OR, NOT and exclusive OR logic functions, positive (+ 1) and negative (- 1) increments, shifts to the left and to the right, checking a word, portion of a word or single bit for "0", and generating accelerated carry signals. The block diagram of the CPU (Figure 3.64) includes the arithmetic logic unit (ALU), the fast-access memory (R_0, ... R_9, T), a storage register - the accumulator (AS), the memory address register (RA) and the microfunction decoder. The CPU has three types of input data buses (M_1, M_0; V_1, V_0; K_1, K_0), and two types of output data buses (A_1 A_0; D_1, D_0) with three stable states. We shall analyze the operation of a CPU which performs the arithmetic, logic and register functions of a two bit microprogram central processor.

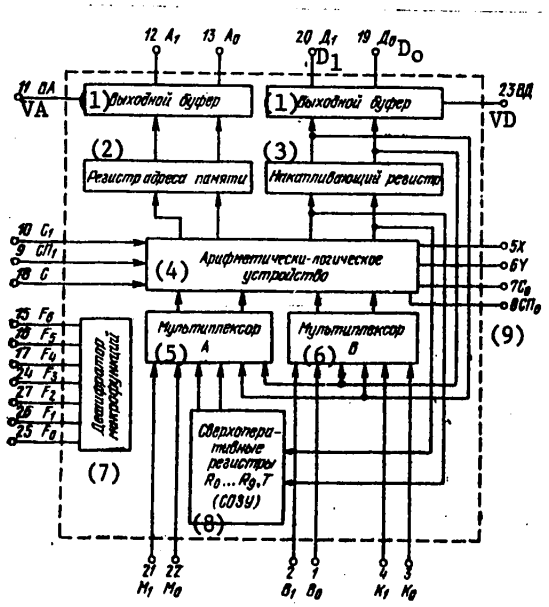


Figure 3.64. Block diagram of the central processor unit (K589IK02 integrated circuit).

Key: 1. Output buffer;
2. Memory address register;
3. Accumulator;
4. Arithmetic logic unit;
5. Multiplexer A;
6. Multiplexer B;
7. Microfunction decoder;
8. High speed registers R0 ... R_g T (SOZU) [fast-access store];
9. Shift to the right output.

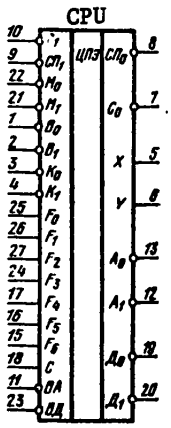


Figure 3.65. Circuit symbol for the CPU (K589IK02 IC) and the designation of the leads.

[See Table 3.37 for key].

Data from external sources (peripherals, memories) is fed to the CPU via one of three input buses. Data are transmitted from the CPU to peripherals via one of two output buses. The data are stored inside the CPU in one of eleven registers of a fast-access store (SOZU) or in an accumulator register. Data is fed from the input buses, the registers and the accumulator to the arithmetic logic unit through two internal multiplexers, A and B. The additional inputs and outputs serve to propagate the carry, shifts and selection of a microinstruction. The schematic symbol for the CPU is shown in Figure 3.65 while the designation of the leads is given in Table 3.37. The information existing on the seven input bus lines for the microinstructions, designated F_0 ... F_6, are decoded inside the CPU for the selection of the arithmetic logic unit functions, the generation of the fast access store address as well as for the control of multiplexers A and B.

The input bus M is intended for transmitting data from the peripheral main memory to the CPU. The data are fed from bus M through the internal multiplexer to the arithmetic logic unit input. The input bus B is intended for transmitting data from the peripheral input-output systems to the CPU. Data are also fed from bus B to the input of the arithmetic logic unit through the multiplexer, but independently of bus M. The breakdown into two buses provides for relatively low loading of the memory buses even in the case where a large number of input-output peripherals are connected to bus B. In another usage variant, the input buses B can be connected by external wiring to one of the output buses to obtain a shift by several bits operation (for example, by one byte). In this case, the input-output units are switched by external circuits to the M inputs.

The fast-access store contains 11 registers, designated as R_0 ... R9 and T. The signal from the fast-access store output is fed through an internal multiplexer to the input of the arithmetic logic unit, and in turn, from the output of the arithmetic logic unit to the fast-access store input.

There is an independent register, the accumulator, to store the results of arithmetic logic unit operations in the CPU. The accumulator output is coupled through an internal multiplexer to the arithmetic logic unit input, and moreover, the output of the accumulator is connected to an output buffer (having three states) for output to the D output bus. The D bus is usually employed to transmit data to the external main memory or to input-output peripherals.

Multiplexers A and B select one of the two arithmetic logic unit inputs depending on the data on the microinstruction bus. The data on bus M, the output of the fast-access store and the accumulator are fed to the inputs of multiplexer A.

TABLE 3.37 Designation of the CPU Leads

Contacts	Designation	Function	Type of Output
1,2	V_0, V_1	External bus inputs	-
3,4	K_0, K_1	Masking bus inputs	-
5,6	X, Y	Accelerated carry output	Two states
7	C_0	Carry output	Three states
8	SP_0	Shift to the right output	The same
9	SP_1	Input for the shift to the right	-
10	S_1	Carry input	-
11	VA	Address enable input	-
12,13	A_1, A_0	Memory address output	Three states
14		Common	-
15...17	F_6...F_4	Microinstruction code input	-
24...27	F_3...F_0	The same	-
18	S	Synchronization input	
19, 20	D_0, D_1	Information output	Three states
21, 22	M_1, M_0	Information input	-
23	VD	Data enable input	-
28		Power	-

Note: The output and input data at the X, Y, F_0...F_6 leads is represented in a direct code, and at the remaining leads, in an inverse code. The high level voltage corresponds to a logic "1".

The data of bus B, the accumulator and the bus K data are fed to the inputs of multiplexer B. The data at the selected input of multiplexer B is always logically multiplied by the contents of the corresponding K input to provide for flexible masking and bit checking capability.

The arithmetic logic unit is capable of performing arithmetic and logic operations, including binary addition in a complementary code, +1 and -1 operations, bitwise logic addition and multiplication, bitwise "exclusive NOR" operations and bitwise logic complementing. The results of an arithmetic logic unit operation can be written into the accumulator or into one of the fast access store registers. To perform shift to the right operations, there are individual "right shift input" (SP_1) and "right shift output" (SP_0) leads. The carry input and output lines

(S_1 and S_0) are intended for providing normal series carry propagation. The data at the S_0 and SP_0 outputs are fed through two buffers, which have three states each, where output either to S_0 or only to SP_0 is enabled. Moreover, the standard outputs for the high speed carry circuits X and Y make it possible to obtain a high speed carry for any word length.

The capability of masking the arithmetic logic inputs by means of bus K considerably increases the universality of the arithmetic logic unit. During nonarithmetic operations, the carry circuits are used to obtain the logic assembly (OR) of all of the word bits for the purpose of analyzing the operation result for "0" or of one of the registers (for example, the ANP or ORR microinstructions).

Thus, the CPU provides for flexible checking of bit contents. Bus K is also used during arithmetic operations to mask portions of the field being processed. A supplemental function of bus K is the transmission of constants from the microprogram to the CPU.

A separate arithmetic logic output goes to the memory address register (RA) and from it, to the output bus A through an output buffer with three states. Usually, register RA and bus A are used for transmitting addresses to a peripheral main memory. The register RA and bus A may also be used for selecting a peripheral when performing input-output operations.

A microinstruction is fed to the CPU F inputs in each microcycle. The microinstruction decoded, the multiplexers select the operands and the arithmetic logic unit performs the requisite operation. Using the negative edge of the sync pulse, the result of an arithmetic logic unit operation is either placed in the accumulator or written into the selected register of the fast-access store. Moreover, the result of an arithmetic logic unit operation is written into the RA register in some operations. A new microinstruction can be fed in only using the positive edge of the sync pulse. In the case of external control of the CPU sync signal, the sync pulse may be omitted in the microcycle, and since the carry, shift and high speed carry circuits are not synchronized, their outputs may be used in this cycle to perform a number of data checks in the accumulator and the fast access store. The contents of the registers do not change in the case of operations in the absence of the sync signal.

(1) Группа функций (F-группа)	F_1	F_2	F_3
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

TABLE 3.38 Microinstrion F-Group Formats

Key: 1. Group of functions (F-group).

TABLE 3.39 The Microinstructiion R-Group Format

Группа регистра (R-группа)	Регистр (2)	F_3	F_2	F_1	F_0
(1)	R_0	0	0	0	0
	R_1	0	0	0	1
	R_2	0	0	1	0
	R_3	0	0	1	1
	R_4	0	1	0	0
1	R_5	0	1	0	1
	R_6	0	1	1	0
	R_7	0	1	1	1
	R_8	1	0	0	0
	R_9	1	0	0	1
	T	1	1	0	0
	AC	1	1	0	1
2	T	1	0	1	0
	AC	1	0	1	1
3	T	1	1	1	0
	AC	1	1	1	1

Key: 1. Register group (R-group);
2. Register.

The contents of the microinstruction being executed are defined by the functional group (F group) and the register group (R group) whicb are specified by the F bus code; the F group is determined by the three high order digits of the data ($F_4 \ldots F_6$), while the R group is determined by the four low order bits ($F_0 \ldots F_3$).

R group 1 includes the registers $R_0 \ldots R_9$, T and AS, and is designated by the symbol R_n. R group 2 and R group 3 contain only the register T and the accumulator (AS). The formats and coding of the F and R groups are given in Table 3.38 and Table 3.39 respectively.

Two additional microinstructions relative to the result in the case of "0" and "1" at the inputs of the K bus are given when considering the CPU microinstruction following the overall functional description of an operation. In the majority of cases, setting the signals at the K bus inputs to "1" and "0" is either the accessing or the absence of accessing of the accumulator respectively in the given microoperation. The mnemonic symbols for the microoperations are included in each description as reference data. A mnemonic may be used as a microassembler language. A listing of microinstruction is given in Table 3.40. The execution of microinstructions for the "all zeros" and "all ones" states of the K bus is illustrated in Table 3.41.

An example of the decoding of the instruction indicated in Table 3.40, for the case of the F group = 0 and R group = 1: logic multiplication of the accumulator contents by the K bus data, the addition of the result to the contents of register R_n and by the value at the carry input S_1, as well as the writing of the results into R_n and the accumulator.

An example of the decoding of an operation in accordance with the mnemonics ILR and ALR, indicated in Table 3.41: for the case of the ILR mnemonic and the K = 00 state of the K bus, the addition of the contents R_n to the value at the S_1 input and the loading of the result into the accumulator and R_n; for the case of the ALR mnemonic and the K = 11 state of the K bus, the addition of the contents of the accumulator and S_1 to the contents of R_n and the placement of the result in the accumulator and R_n. If the accumulator address is indicated in the address portion of the microinstruction, then the accumulator contents are shifted one bit to the left. The circuit for combining central processor units together (K589IK02

TABLE 3.40 Listing of CPU Microinstructions

F-группа / F-group	R-группа / R-group	Instruction Инструкция	
0	1	$R_n+(AC\wedge K)+C_1\to R_n$, AO	
	2	$M+(AC\wedge K)+C_1\to AT$	
	3	$AT_0\wedge(\overline{B_0\wedge K_0})\to C\Pi_0$ $[AT_0\wedge(B_0\wedge K_0)]\vee[\overline{AT_1}\vee(B_1\wedge K_1)]\to AT_0$	$C\Pi_1\vee[(B_1\wedge K_1)\wedge AT_1]\to AT_1$
1	1	$K\vee R_n\to PA$	$R_n+R+C_1\to R_n$
	2	$K\vee M\to RA$	$M+K+C_1\to AT$
	3	$(\overline{AT}\vee K)+(AT\wedge K)+C_1\to AT$	
2	1	$(AC\wedge K)-1+C_1\to R_n$	
	2	$(AC\wedge K)-1+C_1\to AT$	
	3	$(B\wedge K)-1+C_1\to AT$	
3	1	$R_n+(AC\wedge K)+C_1\to R_n$	
	2	$M+(AC\wedge K)+C_1\to AT$	
	3	$AT+(B\wedge K)+C_1\to AT$	
4	1	$C_1\vee(R_n\wedge AC\wedge K)\to C_0$	$R_n\wedge(AC\wedge K)\to R_n$
	2	$C_1\vee(M\wedge AC\wedge K)\to C_0$	$M\wedge(AC\wedge K)\to AT$
	3	$C_1\vee(AT\wedge B\wedge K)\to C_0$	$AT\wedge(B\wedge K)\to AT$
5	1	$C_1\vee(R_n\wedge K)\to C_0$	$K\wedge R_n\to R_n$
	2	$C_1\vee(M\wedge K)\to C_0$	$K\wedge M\to AT$
	3	$C_1\vee(AT\wedge K)\to C_0$	$K\wedge AT\to AT$
6	1	$C_1\vee(AC\wedge K)\to C_0$	$R_n\vee(AC\wedge K)\to R_n$
	2	$C_1\vee(AC\wedge K)\to C_0$	$M\vee(AC\wedge K)\to AT$
	3	$C_1\vee(B\wedge K)\to C_0$	$AT\vee(B\wedge K)\to AT$
7	1	$C_1\vee(R_n\wedge AC\wedge K)\to C_0$	$R_n\mp(AC\wedge K)\to R_n$
	2	$C_1\vee(M\wedge AC\wedge K)\to C_0$	$M\mp(AC\wedge K)\to AT$
	3	$C_1\vee(AT\wedge B\wedge K)\to C_0$	$AT\mp(B\wedge K)\to AT$

Примечание. Знак $\mp$ обозначает операцию «исключающее ИЛИ—НЕ»

Note: The $\overline{+}$ indicates an "exclusive NOR operation.

integrated circuits) to construct devices having a capacity of 2_n bits is shown in Figure 3.66.

The high speed carry circuit (SUP) is intended for generating the group carries in the case where it is used jointly with CPU's. One high speed carry circuit and eight CPU's make it possible to set up a 16 bit adder. The high speed carry circuit has 17 information inputs, 8 information outputs and 1 control input, which makes it possible to control the output of the highest order carry, shifting it to the third state.

TABLE 3.41 The Execution of Microinstructions for the "All Zeros" and "All Ones" States of the K Bus

K=00		Мнемоника Mnemonic	K=11		Мнемоника Mnemonic
$R_n+C_1\to R_n$, AC $M+C_1\to AT$ $AT_0\to C\Pi_0$ $C\Pi_1\to AT_1$	$AT_1\to AT_0$	ILR ACM SRA	$AC+R_n+C_1\to R_n$, AC $M+AC+C_1\to AT$		ALR AMA
$R_n\to RA$ $M\to PA$ $\overline{AT}+C_1\to AT$	$R_n+C_1\to R_n$ $M+C_1\to AT$	LMI LMM CIA	$11\to PA$ $11\to PA$ $AT-1+C_1\to AT$	$R_n-1+C_1\to R_n$ $M-1+C_1\to AT$	DSM LDM DCA
$C_1-1\to R_n$ $C_1-1\to AT$ см. CSA		CSR CSA	$AC-1+C_1\to R_n$ $AC-1+C_1\to AT$ $B-T+C_1\to AT$		SDR SDA LDI
$R_n+C_1\to R_n$ см. ACM $AT+C_1\to AT$		INR INA	$AC+R_n+C_1\to R_n$ см. AMA $B+AT+C_1\to AT$		ADR AIA
$C_1\to C_0$ $C_1\to C_0$ см. CLA	$0\to R_n$ $0\to AT$	CLR CLA	$C_1\vee(R_n\wedge AC)\to C_0$ $C_1\vee(M\wedge AC)\to C_0$ $C_1\vee(AT\wedge B)\to C_0$	$R_n\wedge AC\to R_n$ $M\wedge AC\to AT$ $AT\wedge B\to AT$	ANR ANM ANI
см. CLR см. CLA см. CLA			$C_1\vee R_n\to C_0$ $C_1\vee M\to C_0$ $C_1\vee AT\to C_0$	$R_n\to R_n$ $M\to AT$ $AT\to AT$	TZR LTM TZA
$C_1\to C_0$ $C_1\to C_0$ см. NOP	$R_n\to R_n$ $M\to AT$	NOP LMF NOR	$C_1\vee AC\to C_0$ $C_1\vee AC\to C_0$ $C_1\vee B\to C_0$	$R_n\vee AC\to R_n$ $M\vee AC\to AT$ $B\vee AT\to AT$	ORR ORM ORI
$C_1\to C_0$ $C_1\to C_0$ $C_1\to C_0$	$\overline{R}_n\to R_n$ $\overline{M}\to AT$ $\overline{AT}\to AT$	CMR LCM CMA	$C_1\vee(R_n\wedge AC)\to C_0$ $C_1\vee(M\wedge AC)\to C_0$ $C_1\vee(AT\wedge B)\to C_0$	$R_n\mp AC\to R_n$ $M\mp AC\to AT$ $B\mp AT\to AT$	XNR XNM XNI

The schematic symbol for the high speed carry circuit (K589IK03 integrated circuit) and the designation of its leads are shown in Figure 3.67. The state of each of the eight cutputs of the high speed carry circuit is described by the following logic equation:

$$\overline{C_n+1} = X_0Y_0 + Y_0\overline{C}_n$$
$$\overline{C_n+2} = X_1Y_1 + Y_1Y_0X_0 + Y_1Y_0\overline{C}_n$$
$$\overline{C_n+3} = Y_2X_2 + Y_2Y_1X_1 + Y_2Y_1Y_0X_0 + Y_2Y_1Y_0\overline{C}_n$$

$$\overline{C_n + 4} = Y_3X_3 + Y_3Y_2X_2 + Y_3Y_2Y_1X_1 + Y_3Y_2Y_1Y_0X_0 + Y_3Y_2Y_1Y_0\overline{C}_n$$

$$\overline{C_n + 5} = Y_4X_4 + Y_4Y_3X_3 + Y_4Y_3Y_2X_2 + Y_4Y_3Y_2Y_1X_1 + Y_4Y_3Y_2Y_1Y_0X_0 + Y_4Y_3Y_2Y_1Y_0\overline{C}_n$$

$$\overline{C_n + 6} = Y_5X_5 + Y_5Y_4X_4 + Y_5Y_4Y_3X_3 + Y_5Y_4Y_3Y_2X_2 + Y_5Y_4Y_3Y_2Y_1X_1 + Y_5Y_4Y_3Y_2Y_1Y_0X_0 + Y_5Y_4Y_3Y_2Y_1Y_0\overline{C}_n,$$

$$\overline{C_n + 7} = Y_6X_6 + Y_6Y_5X_5 + Y_6Y_5Y_4X_4 + Y_6Y_5Y_4Y_3X_3 + Y_6Y_5Y_4Y_3Y_2X_2 + Y_6Y_5Y_4Y_3Y_2Y_1X_1 + Y_6Y_5Y_4Y_3Y_2Y_1Y_0X_0 + Y_6Y_5Y_4Y_3Y_2Y_1Y_0\overline{C}_n,$$

if the "1" level is set at the RP [?carry register?] input;

$\overline{Cn + 8}$ in the third state, if the "0" level appears at the RP input.

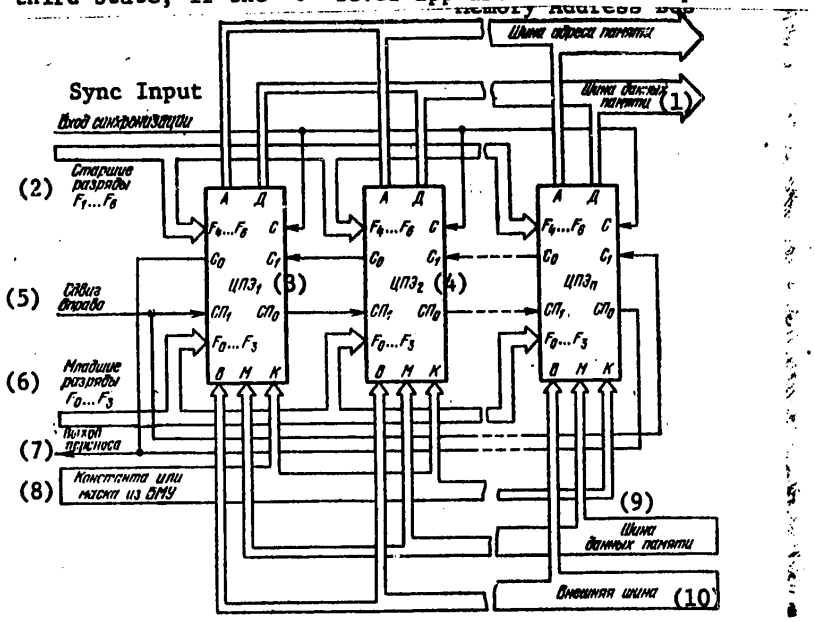
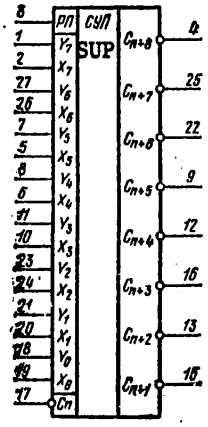


Figure 3.66. Schematic showing the combining of CPU's (K589IK02 integrated circuits) to construct devices having 2n digits.

Key: 1. Memory data bus;
2. High order bits, $F_1 \ldots F_6$;

[Key to Figure 3.66, continued]:

3. $TsPE_1$ = central processor unit 1 [CPU 1];
4. CPU_2;
5. Shift to the right;
6. Low order bits, $F_0 \ldots F_3$;
7. Carry output;
8. Constant or mask from the microprocessor controller;
9. Memory data bus;
10. External bus.



Designation of High Speed Carry Circuit Leads

Назначение выводов СУП

Pins	(1) Обозначение	(2) Наименование	Тип выхода	Level Уровень активности
1,2,5...8, 10,11, 18...24,25, 24,26,27	$X_0 \ldots X_7$ $Y_0 \ldots Y_7$	Входы групповых переносов (3)	Type Output	„1"
3	РП	Вход разрешения переноса C_{n+8} (4)	—	„0"
4	C_{n+8}	Выходы переноса Carry Outputs	Три состояния (8)	„0"
9,12,13 15,16, 22,26	$C_{n+1} \ldots C_{n+7}$		Два состояния (5)	—
28	—	Pwr. Питание	—	—
17	C_n	(6) Вход переноса	—	„0"
14	—	(7) Общий	—	—

Figure 3.67. Schematic symbol for the high speed carry circuit (K589IK03 integrated circuit) and the designation of the leads. [SUP = high speed carry circuit].

Key: 1. Designation;
2. Function;
3. Inputs for the group carries;
4. C_{n+8} carry enable input;
5. Two states;
6. Carry input;
7. Common;
8. Three states.

A variant for high speed carry circuit use (K589IK03 integrated circuit) in conjunction with a CPU (K589IK02 integrated circuit) is shown in Figure 3.68.

The multimode buffer register (MBR) is a universal eight bit register, consisting of D flip-flops and output buffer circuits with three stable states. It has built-in selective logic and an independent separate D flip-flop for generating a central processor interrupt query. One or sveral MBR's can be used to realize

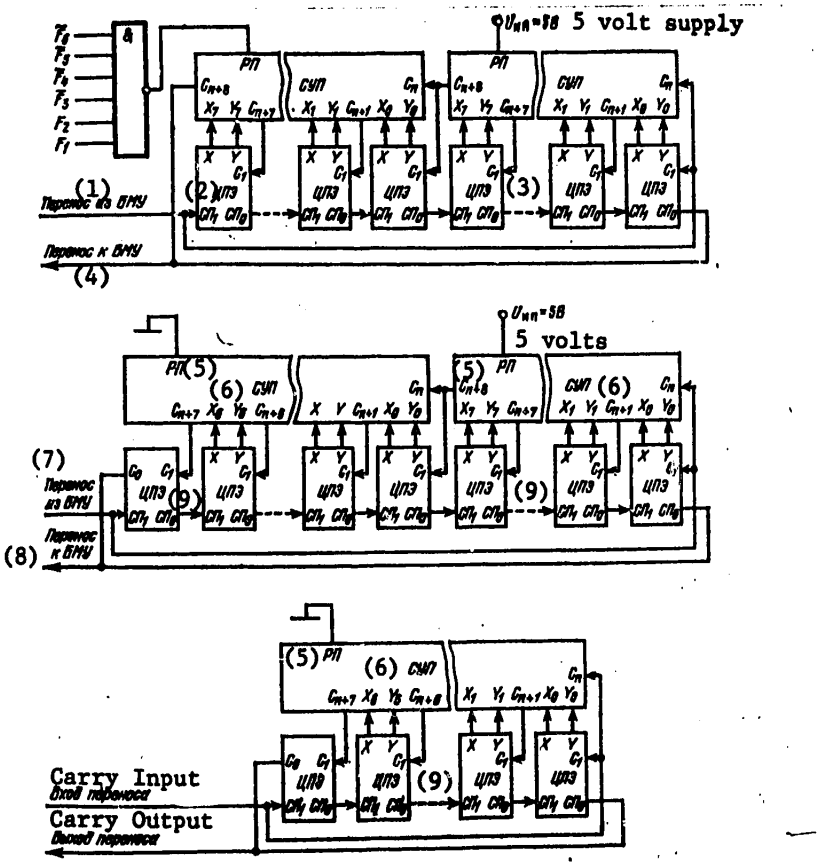


Figure 3.68. Examples of high speed carry circuit applications (K589IK03 integrated circuit) in conjunction with CPU's (K589IK02 integrated circuits).

Key: 1. Carry from the microprocessor controller;
2,3. CPU's;
4. Carry to the microprocessor controller;
5. Carry register;
6. High speed carry circuit;
7. Carry from the microprocessor controller;
8. Carry to the microprocessor controller;
9. CPU's.

Figure 3.69. Schematic symbol for the multimode buffer register (K589IR12 integrated circuit) and the designation of the leads. [MBR = multimode buffer register].

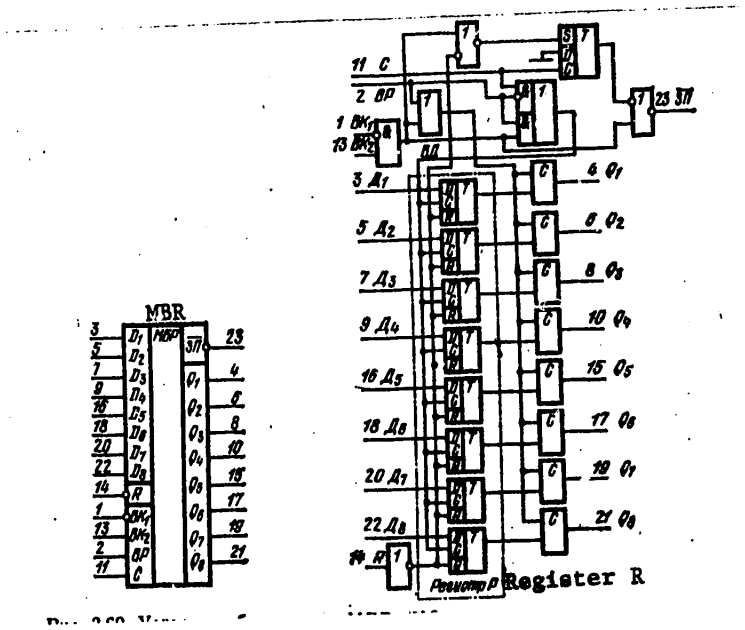


Figure 3.70. Block diagram of the multimode buffer register (K589IR12 integrated circuit).

many types of interfaces and auxiliary units, such as simple data registers, buffer registers with data gating, multiplexers, bidirectional bus drivers, interruptible input-output channels, etc. The circuit schematic symbol of an MBR (K589IR12 integrated circuit) is shown in Figure 3.69, while the designation of its leads is given in Table 3.42. We shall analyze MBR operation in accordance with the block diagram of it shown in Figure 3.70.

The information D flip-flops repeat the input data at the high logic level of the input signal S, and the input information is written in at the low logic

TABLE 3.42 Designation of the Multimode Buffer Register Leads

Pins	Designation	Function	Type of Output	Level
1, 13	VK_1, VK_2	Chip selection inputs	-	"0" (VK_1); "1" (VK_2)
2	VR	Mode selection input	-	-
3, 5, 7, 9, 16, 18, 20, 22	$D_1 \ldots D_8$	Information inputs	-	-
4, 6, 8, 10, 15, 17, 19, 21	$Q_1 \ldots Q_8$	Information outputs	Three states	-
11	S	Strobe input	-	"1"
12	-	Common	-	-
14	R	Zero set input	-	"0"
23	$\overline{ZP}$	Interrupt query output	Two states	-
24	-	Power	-	-

level of the signal at the S input. The outputs of each information flip-flop are connected to the inverting output buffer switches, which have three stable states. The internal bus for data output (VD) gates each output buffer. When voltage is present on the VD bus, the output buffers are unblocked and the data is fed to the output of the corresponding output data line ($Q_1 \ldots Q_8$).

The inputs VK_1 and VK_2 control the chip selection. When a "0" voltage is present at the VK_1 input and a "1" appears at the VK_2 input, the unit selection is enabled.

The VR (mode select) input defines one of two operating modes. When there is a "0" signal at the mode select input, the device operates in an input mode. The output buffers are turned on in this mode. When a unit is selected, the right-in control is realized using the S input signal. When there is a "1" signal at the mode select input, the device operates in an output mode, in this case, the output buffers are turned on regardless of the selection of a unit. Thus, the writing of information into the register and output from the register are accomplished in accordance with the following formulas:

$$ZP = C \wedge BP \vee \overline{BK_1} \wedge BK_2 \wedge BP \quad \text{(write into the register)}$$

$$VD = BP \vee \overline{BK_1} \vee BK_2 \quad \text{(information output from the register).}$$

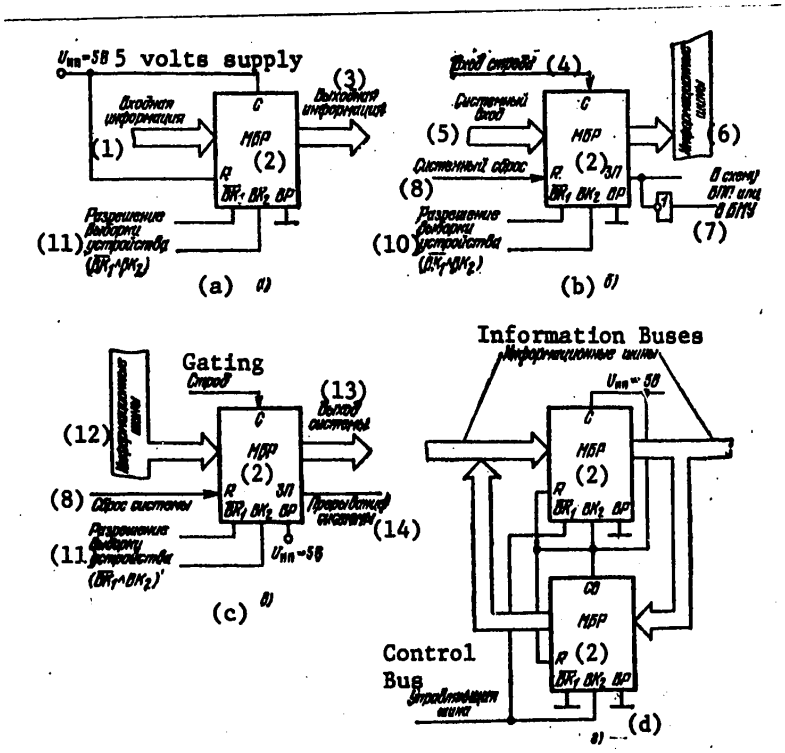


Figure 3.71. Examples of multimode buffer register applications (K589IR12 integrated circuit).

a. Input buffer;
b. Interrupt controller;
c. Output buffer;
d. Bidirectional data transmission.

Key: 1. Input information;
2. Multimode buffer register;
3. Output information;
4. Gating input;
5. System input;
6. Information buses;
7. To the priority interrupt or microprocessor controllers;
8. System reset;
9. Supply voltage = 5 volts;
10,11. Unit selection enable;
12. Information buses;
13. System output;
14. System interrupt.

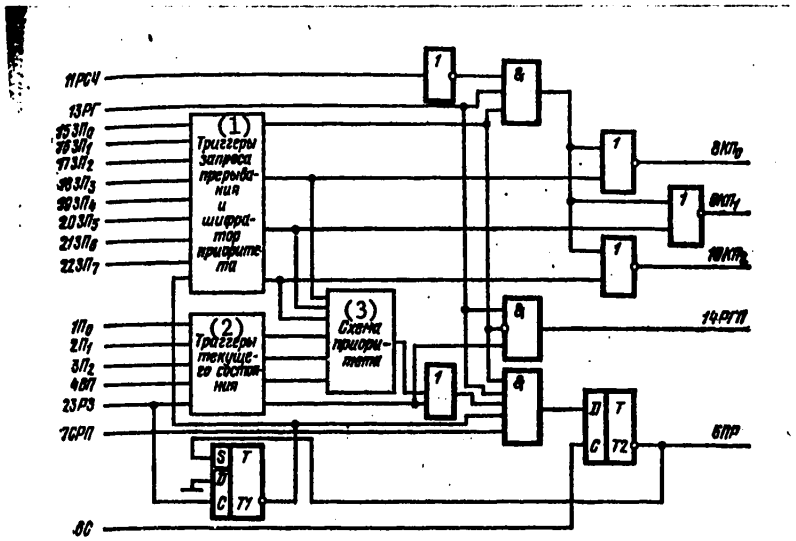


Figure 3.72. Block diagram of the priority interrupt controller (K589IK14 integrated circuit).

T1 = Interrupt blocking flip-flop;
T2 = Interrupt flip-flop;

Key: 1. Priority coder and interrupt query flip-flops;
2. Current state flip-flop;
3. Priority circuit.

The interrupt query flip-flop serves to generate the interrupt query signal in the processor system. When the system is set to the initial state by the "zero set" low level signal, the interrupt query flip-flop is set to "1", i.e., the given device does not require an interrupt. Simultaneously, the register R is set to "0" by this same signal. The interrupt query flip-flop output is joined together via an OR to the output of the device select logic circuit. It is assumed that the MBR is in the interrupt state when a "0" corresponds to the output of the ZP [register entry], which makes it possible for a direct connection to the query input (the active one is low level) of the priority interrupt unit. When working in the input mode (i.e., the low level appears at the mode select input), the input signal S writes the information into the data register and sets the interrupt query flip-flop to "0". The interrupt query flip-flop is set to "1" given the condition that a device is selected (an interrupt signal is generated in the same way at the ZP output). Thus, the interrupt conditions are as follows: ZP = $= \overline{BK_1} \wedge BK_2 \vee C$. The interrupt signal reset is accomplished in accordance with the following formula:

$$\text{Register entry reset} = R \vee \overline{\overline{BK_1} \wedge BK_2} = \overline{R} \vee BK_1 \vee \overline{BK_2}$$

Examples of multimode buffer register applications (K589IR12 integrated circuit) are shown in Figure 3.71.

The priority interrupt controller (BPP) provides for interrupting the task being performed. The interrupt system, which is designed using the BPP, provides for the following capabilities: eight separate interrupt levels for each block, programmable priority, expansion capability of the 8K interrupt levels (K is the number of priority interrupt blocks) and automatic generation of the interrupt vector.

TABLE 3.43 Designation of the Leads of the Priority Interrupt Controller

Pins	Designation	Function	Type of Output	Level
1, 2, 3	$P_0...P_2$	Priority level input	-	0
4	VP	Priority level selection input	-	0
5	PR	Interrupt output	Open collector	0
6	S	Synchronization input	-	1
7	SRP	Interrupt enable gating input	-	1
8, 9, 10	$KP_0...KP_2$	Interrupt mode output	Open collector	0
11	RSCh	Enable input for reading the interrupt code	-	0
12	-	Common	-	-
13	RG	Interrupt group enable output	-	1
14	RGP	Interrupt group enable input	Two states	1
15...22	$ZP_0...ZP_7$	Interrupt inhibit inputs	-	0
23	RZ	Write enable input	-	0
24	-	Power	-	-

The block diagram of the priority interrupt controller (K589IK14 integrated circuit) (Figure 3.72) includes the following: an eight bit register for interrupt queries with an encoder; a three bit current priority register; a three bit priority coder with open collector outputs; and an eight level priority comparator. The schematic designation of the priority controller (K589IK14 integrated circuit) is shown in Figure 3.73, while the designation of its leads is given in Table 3.43.

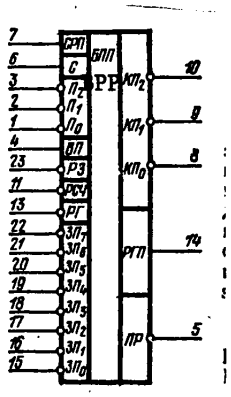


Figure 3.73. Schematic designation of the priority interrupt controller (K589IK14 integrated circuit).

We shall analyze the operation of the priority interrupt controller in accordance with the block diagram shown in Figure 3.72.

To determine interrupt queries, the priority interrupt unit is gated at the end of the execution of each instruction. At this point in time, if an interrupt query is confirmed in the priority interrupt controller, the microprocessor controller shifts over to the microprogram for interrupt processing. Interrupt queries pass through the interrupt memory in the processor and the priority coder to the priority comparator. The interrupt queries are fed from the output of the priority coder to the priority comparator. This value is compared in the priority comparator with the current priority of the priority interrupt controller (the priority level of the priority interrupt controller which is stored in the current state register). A query, which is received during the action of the interrupt gating (SRP), in conjunction with the sync pulse causes the interrupt confirmation flip-flop to be set in the "active interrupt" state (during the execution cycle for one microinstruction), sets the PR [interrupt output] (low level) signal and the interrupt inhibit flip-flop to the "1" state. Based on the PR signal, an interrupt instruction is generatted in the processor which can transmit the control directly to the input of the interrupt servicing routine.

The microprogram which is usually a part of this routine reads the signal level interrogating the interrupt from the $КР0$ ... $КР_2$ interrupt code output buses. The information on the query level which is stored in the interrupt query memory can be transmitted to any of the input information buses of the processor in accordance with the signal fed to the RSCh [interrupt code read enable] input. When the interrupt processing program has determined the query level, it usually rewrites this level back into the current priority register of the priority interrupt controller. In this case, the interrupt inhibit flip-flop is set to "1" and any of the subsequent queries at the given or lower priority level are blocked.

The input to the macrolevel interrupt processing program can be accompanied by an interrupt vector which is generated in accordance with the information on the query level, in accordance with which the subroutine address corresponding to this level is generated. The exiting of such a macroprogram is usually accompanied by the restoration of the previous contents of the current priority memory.

The interrupt group enable input and the interrupt group enable output can be used when connecting several priority interrupt controllers in series, where each priority interrupt controller can inhibit the interrupt for all subsequent controllers.

The interrupt confirmation flip-flop is set to the active state (low level) by the positive leading edge of the sync pulse, if the following conditions are met:

a) The active query level ($ZP_0 \ldots ZP_7$) is higher than the current status $P_0 \ldots P_2$;

b) A "1" signal is present at the SRP [interrupt enable gating] input;

c) A "1" signal is present at the RG [interrupt group enable output] input;

d) The interrupt inhibit flip-flop is reset.

The interrupt output signal asynchronously sets the interrupt inhibit flip-flop to the "1" state and delays the query signals in the interrupt query memory until the sending of new information on the current priority ($P_0 \ldots P_2$, VP [priority level selection] in accordance with the RZ [write enable input] signal) in the current priority register. The interrupt inhibit flip-flop is reset upon the completion of the sending operation. During this process, there can be a "1" at the interrupt group enable output only in the case where the following conditions are met:

a) There is a "1" at the RG input;

b) The current priority does not belong to the given group of levels (is determined in accordance with VP [priority level selection] signal);

c) There are no interrupt queries at the given level.

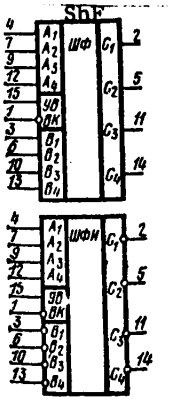


Figure 3.74. Circuit schematic designations of the ShF [bus driver] (K589AP16 IC) and the ShFI [inverting bus driver (K589AP46 IC).

The interrupt code outputs $KP_0 \ldots KP_2$ and the interrupt PR take the form of an open collector, something which makes it possible to combine them.

The noninverting and inverting bus drivers are parallel bidirectional signal drivers for the control of the trunks (buses) in digital computers and take the form of four-channel switchers, which have one bus in each channel just for the reception of the data, one bus just for the output and one bidirectional feedout and receive bus. The information passes through noninverting bus drivers without being changed, and is inverted in inverting bus drivers. The schematic symbols for the noninverting bus driver (K589AP16 IC) and inverting bus driver (K589AP26 AC) are shown in FIgures 3.74, while the designation of their leads is given in Table 3.44 and their block diagrams in Figure 3.75.

Data output control logic is provided to control the operating mode and direction of data transmission in noninverting and inverting bus drivers; this logic is desgined around two dual input AND logic gates. The drivers provide for the transmission of information when there is an "0" at the chip selection input, VK. In the case of a "1" signal at the chip select input, the drivers are in the turned-off state and the outputs have

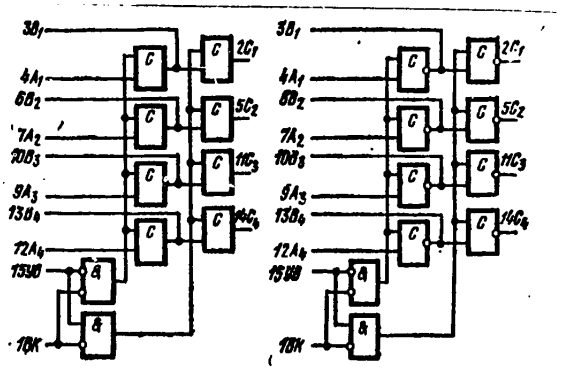


Figure 3.75. Block diagrams of the bus driver (K589AP16 IC) and inverting bus driver (K589AP26 IC).

a high output impedance (the third state). When an "0" signal is present at the VK input, the data output via the C and B buses is controlled by the signal at the control input for the data feedout, UV. If a "0" signal is present at the UV input, then data transmission is turned on from the A inputs to output B. In the case of a "1" signal at the UV input, the data is transmitted from the B inputs to the C outputs.

TABLE 3.44. Designation of the Leads of the Inverting and Noninverting Bus Drivers

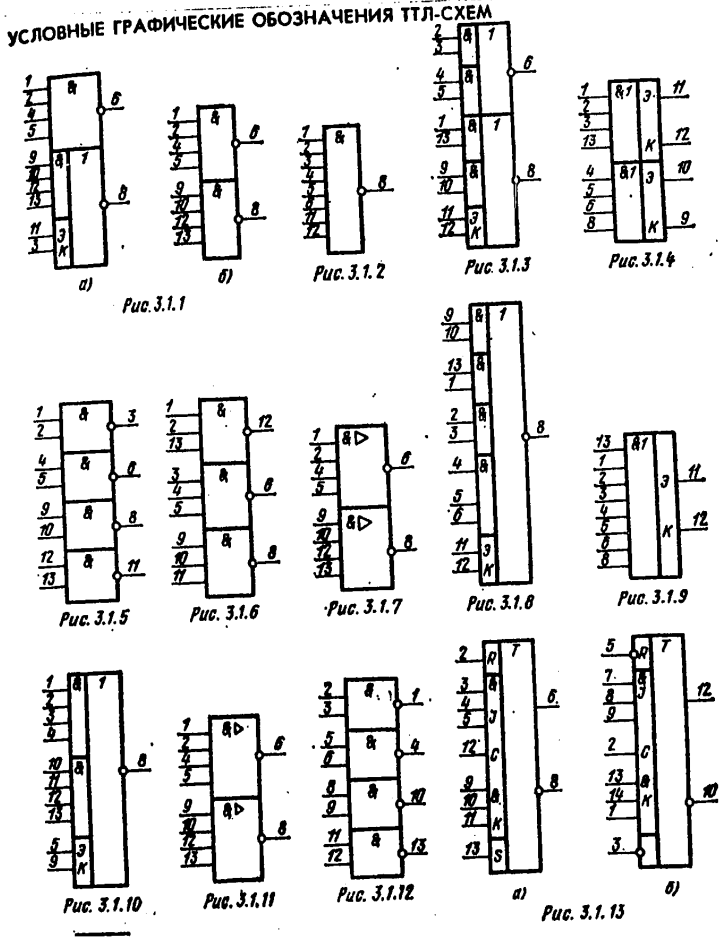
Pins	Designation	Function	Type of Output	Level
1	VK	Chip selection input	-	"0"
2, 5, 11, 14	$C_1 \ldots C_4$	Information output	Three states	-
3, 6, 10, 13	$V_1 \ldots V_4$	Bidirectional data transmission inputs/outputs	The same	-
4, 7, 9, 12	$A_1 \ldots A_4$	Information inputs	-	-
8	-	Common	-	-
15	UV	Control input for information output	-	-
16	-	Power	-	-

[Table 3.44, continued]:

Data Transmission Logic

Logic State at the Inputs		Direction of Data Transmission	Outputs in the Turned-Off State
VK	UV		
0	0	From input A to output B	C
0	1	From input B to output C	B
1	1	No transmission	C, B

Schematic Circuit Symbols for TTL Circuits:



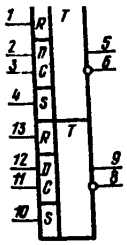


Рис. 3.1.14

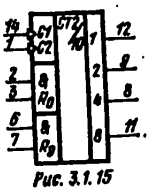


Рис. 3.1.15

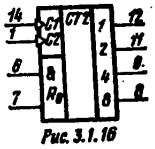
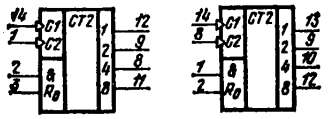


Рис. 3.1.16



а) б)

Рис. 3.1.17

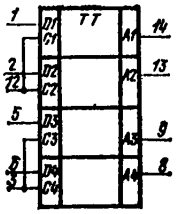


Рис. 3.1.18

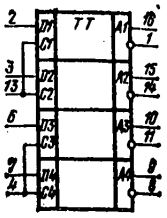
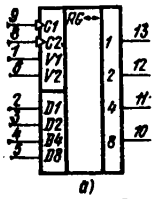


Рис. 3.1.19



а) б)

Рис. 3.1.20

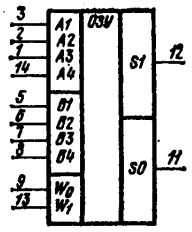


Рис. 3.1.21

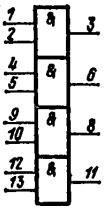


Рис. 3.1.22

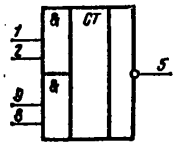


Рис. 3.1.23

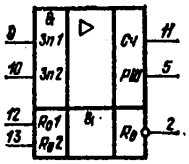


Рис. 3.1.24

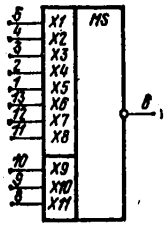


Рис. 3.1.25

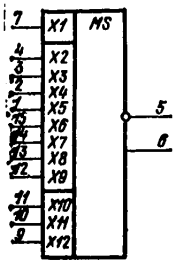


Рис. 3.1.26

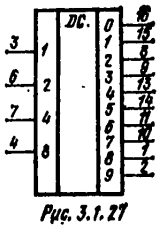


Рис. 3.1.27

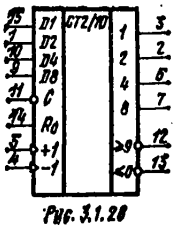


Рис. 3.1.28

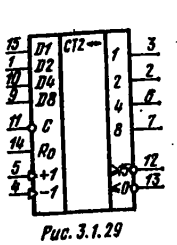


Рис. 3.1.29

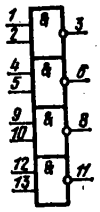


Рис. 3.1.30

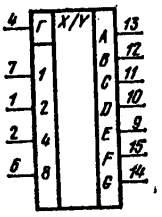


Рис. 3.1.31

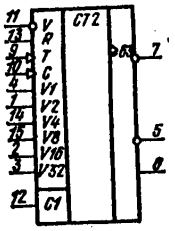


Рис. 3.1.32

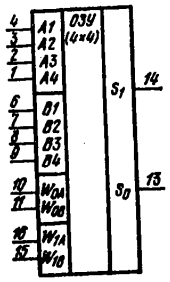


Рис. 3.1.33

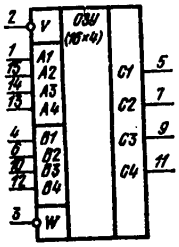


Рис. 3.1.34

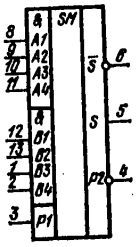


Рис. 3.1.35

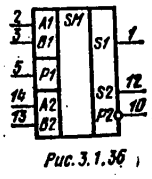


Рис. 3.1.36

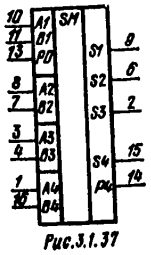


Рис. 3.1.37

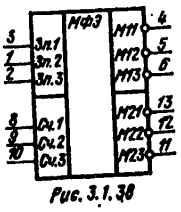


Рис. 3.1.38

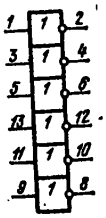


Рис. 3.1.39

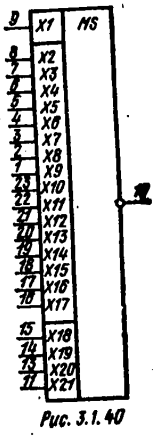


Рис. 3.1.40

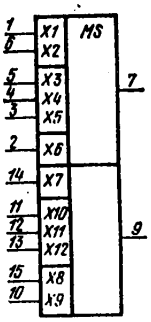


Рис. 3.1.41

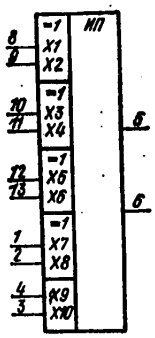


Рис. 3.1.42

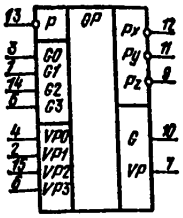


Рис. 3.1.43

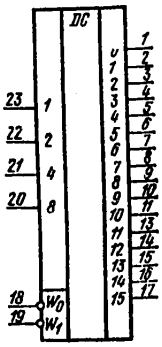
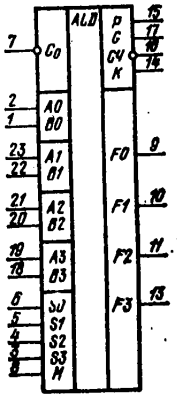
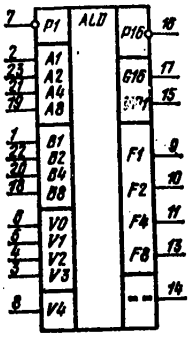


Рис. 3.1.44



а)



б)

Рис. 3.1.45

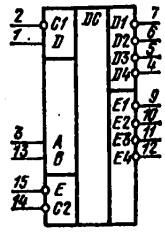


Рис. 3.1.46

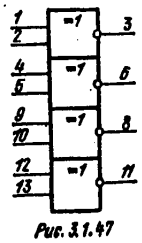


Рис. 3.1.47

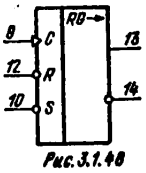


Рис. 3.1.48

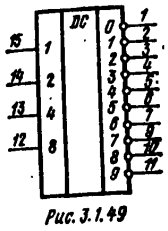


Рис. 3.1.49

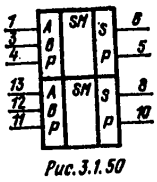


Рис. 3.1.50

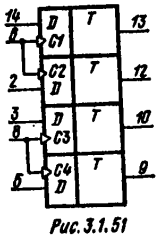


Рис. 3.1.51

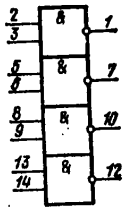


Рис. 3.1.52

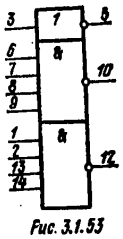


Рис. 3.1.53

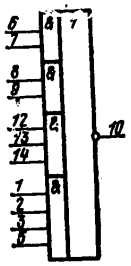


Рис. 3.1.54

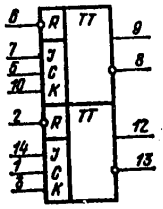


Рис. 3.1.55

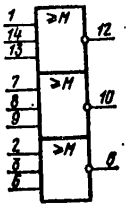


Рис. 3.1.56

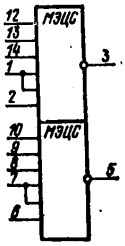


Рис. 3.1.57

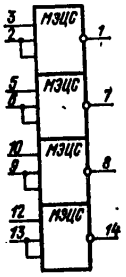


Рис. 3.1.58

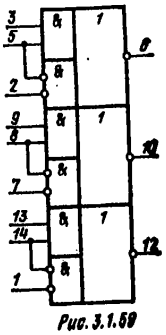


Рис. 3.1.59

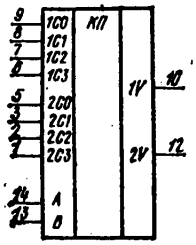


Рис. 3.1.60

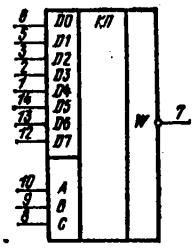


Рис. 3.1.61

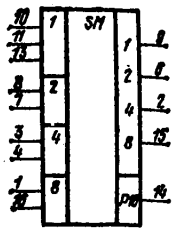


Рис. 3.1.62

Circuit Symbols for Emitter Coupled Transistor Logic Circuits

УСЛОВНЫЕ ГРАФИЧЕСКИЕ ОБОЗНАЧЕНИЯ ЭСТЛ-СХЕМ

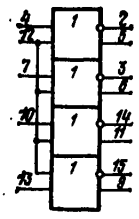


Рис. 3.2.1

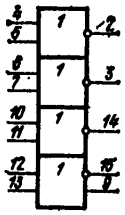


Рис. 3.2.2

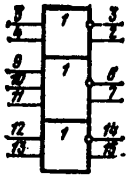


Рис. 3.2.3

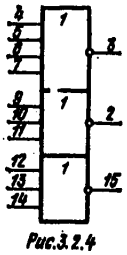


Рис. 3.2.4

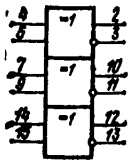


Рис. 3.2.5

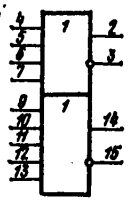


Рис. 3.2.6

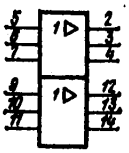


Рис. 3.2.7

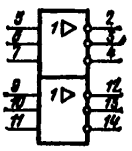


Рис. 3.2.8

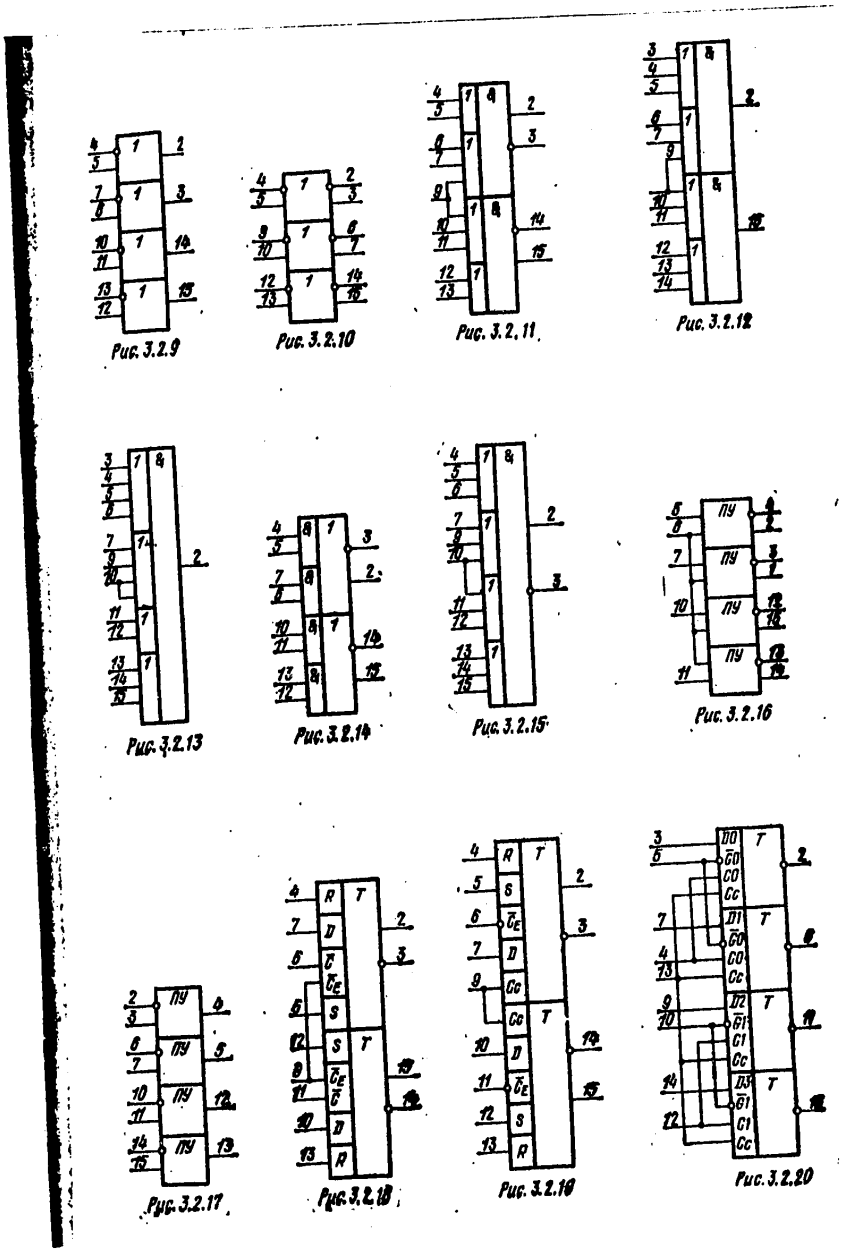


Рис. 3.2.9

Рис. 3.2.10

Рис. 3.2.11

Рис. 3.2.12

Рис. 3.2.13

Рис. 3.2.14

Рис. 3.2.15

Рис. 3.2.16

Рис. 3.2.17

Рис. 3.2.18

Рис. 3.2.19

Рис. 3.2.20

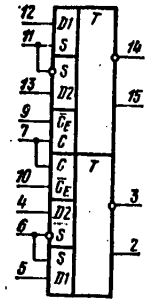


Рис. 3.2.21

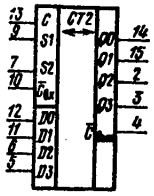


Рис. 3.2.22

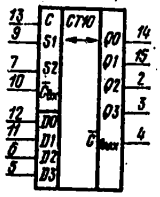


Рис. 3.2.23

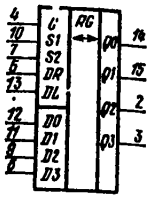


Рис. 3.2.24

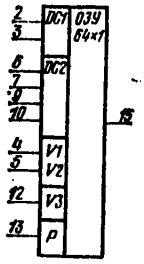


Рис. 3.2.25

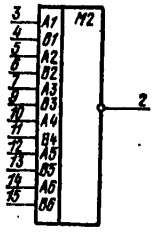


Рис. 3.2.26

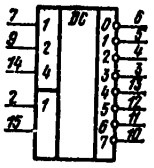


Рис. 3.2.27

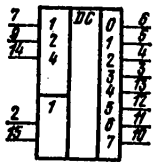


Рис. 3.2.28

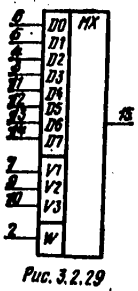


Рис. 3.2.29

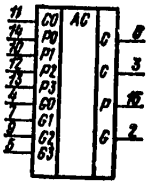


Рис. 3.2.30

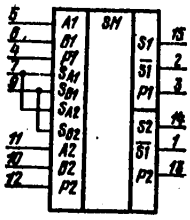


Рис. 3.2.31

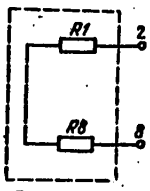


Рис. 3.2.32

192

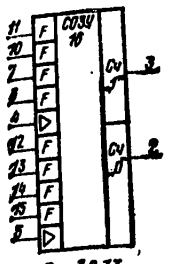


Рис. 3.2.33

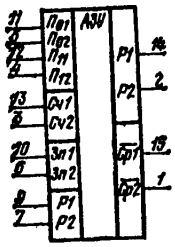


Рис. 3.2.34

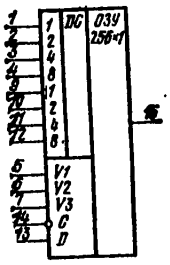


Рис. 3.2.35

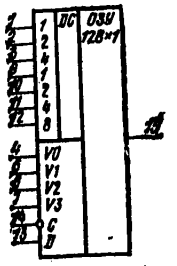


Рис. 3.2.36

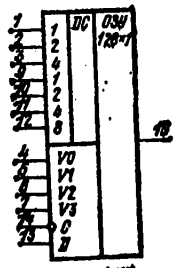


Рис. 3.2.37

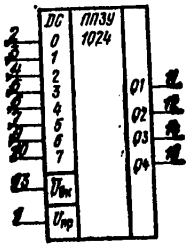


Рис. 3.2.38

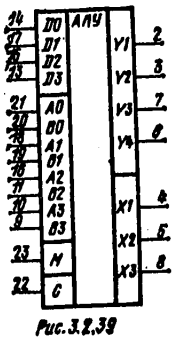


Рис. 3.2.39

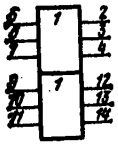


Рис. 3.2.40

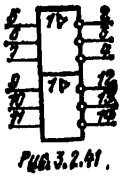


Рис. 3.2.41

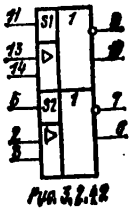


Рис. 3.2.42

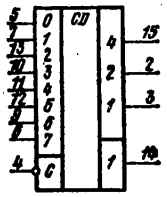


Рис. 3.2.43

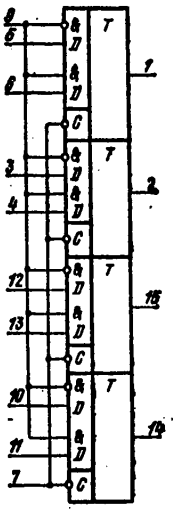


Рис. 3.2.44

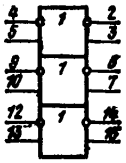


Рис. 3.2.45

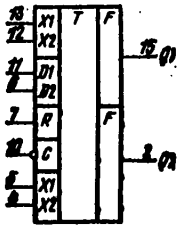


Рис. 3.2.46

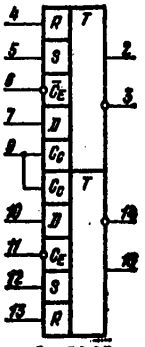


Рис. 3.2.47

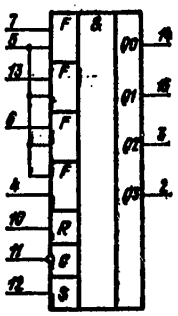


Рис. 3.2.48

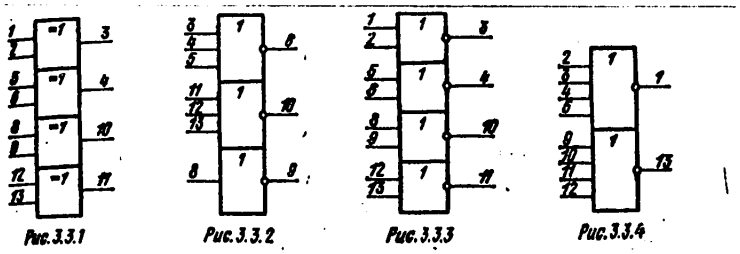


Рис. 3.3.1 Рис. 3.3.2 Рис. 3.3.3 Рис. 3.3.4

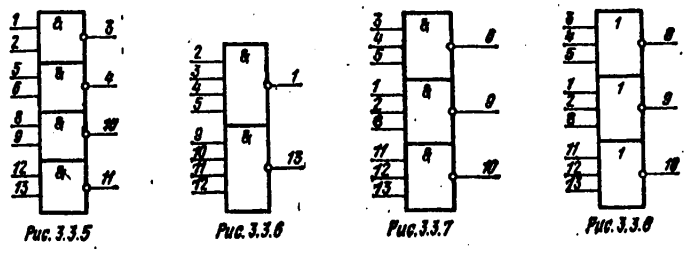


Рис. 3.3.5 Рис. 3.3.6 Рис. 3.3.7 Рис. 3.3.8

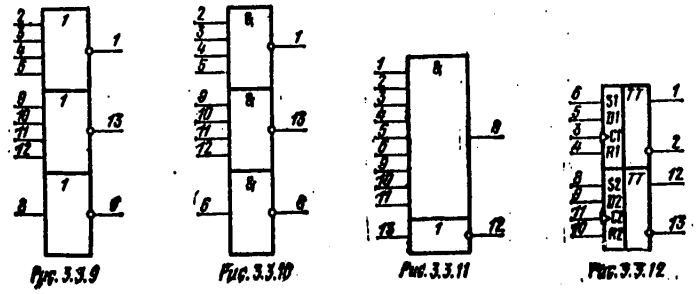


Рис. 3.3.9 Рис. 3.3.10 Рис. 3.3.11 Рис. 3.3.12

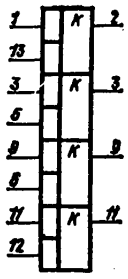


Рис. 3.3.13

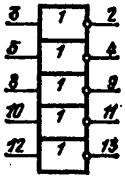


Рис. 3.3.14

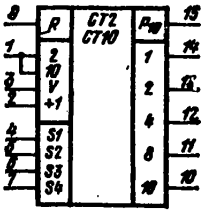


Рис. 3.3.15

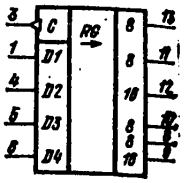


Рис. 3.3.16

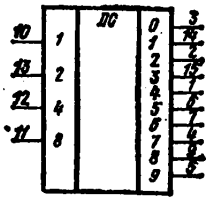


Рис. 3.3.17

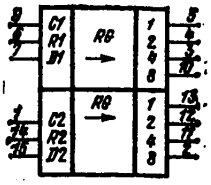


Рис. 3.3.18

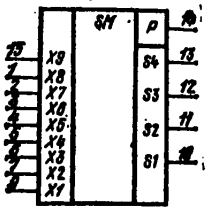


Рис. 3.3.19

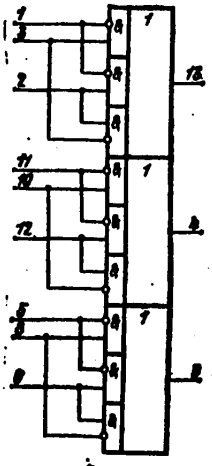


Рис. 3.3.20

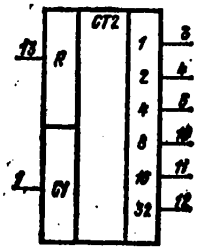


Рис. 3.3.21

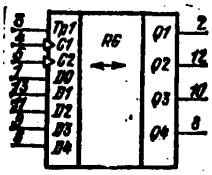


Рис. 3.3.22

198

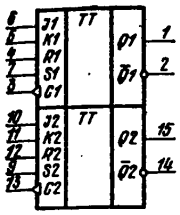


Рис. 3.3.23

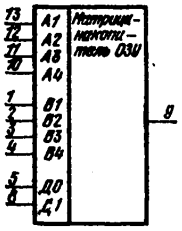


Рис. 3.3.24

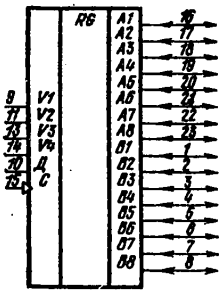


Рис. 3.3.25

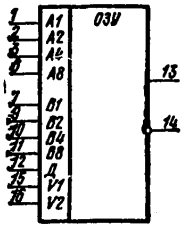


Рис. 3.3.26

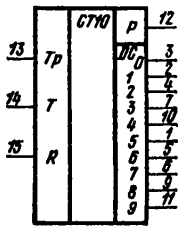


Рис. 3.3.27

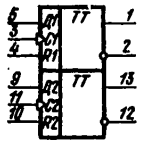


Рис. 3.3.28

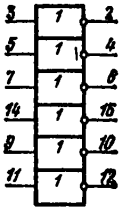


Рис. 3.3.29

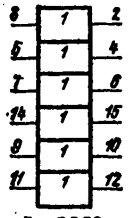


Рис. 3.3.30

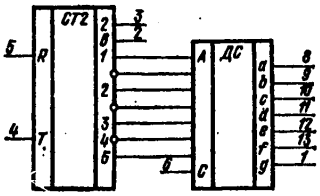


Рис. 3.3.31

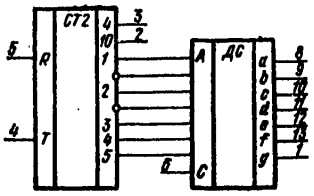


Рис. 3.3.32

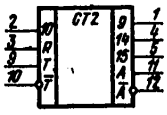


Рис. 3.3.33

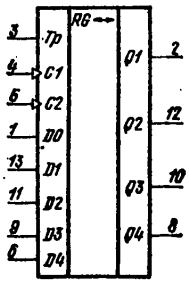


Рис. 3.3.34

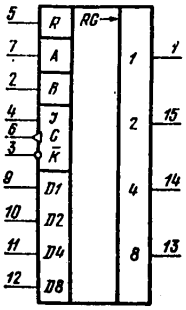


Рис. 3.3.35

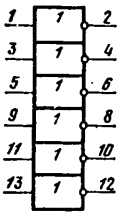


Рис. 3.3.38

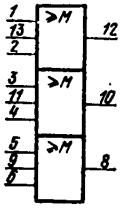


Рис. 3.3.36

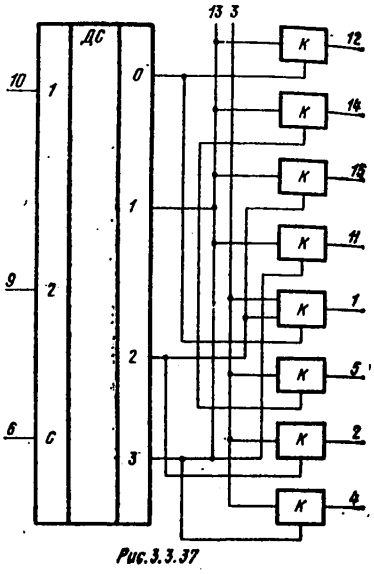


Рис. 3.3.37

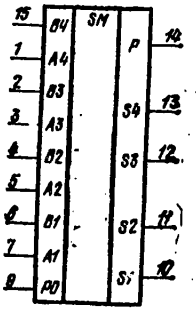


Рис. 3.3.39

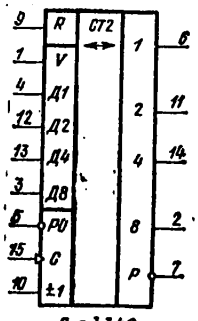


Рис. 3.3.40

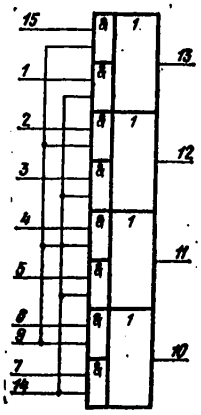


Рис. 3.3.41

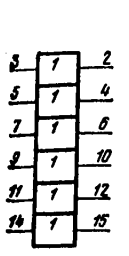


Рис. 3.3.42

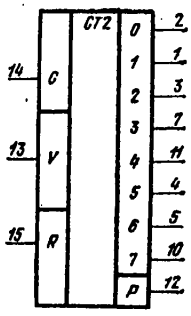


Рис. 3.3.43

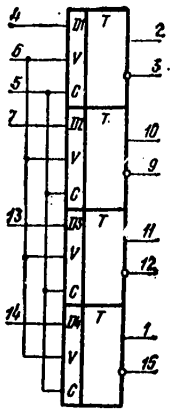


Рис. 3.3.44

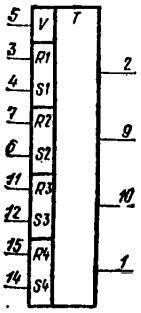


Рис. 3.3.45

BIBLIOGRAPHY

1. Bukreyev I.N., Mansurov B.M., Goryachev V.I., "Mikroelektronnyye skhemy tsifrovykh ustroystv" ["Microelectronic Circuits of Digital Devices"], Moscow, Sovetskoye Radio, 1973, pp 7-50, 99-104.

2. Drozdov Ye.A., Kamarnitskiy V.A., Pyatibratov A.P., "Elektronnyye tsifrovyye vychislitel'nyye mashiny" ["Electronic Digital Computers"], Moscow, Voyenizdat, 1968, pp 73-120.

3. Papernov A.A., "Logicheskiye osnovy tsifrovykh mashin i programmirovaniye" ["The Logic Principles of Digital Computers and Programming"], Moscow, Nauka, 1968.

4. Naumov Yu.Ye., "Integral'nyye logicheskiye skhemy" ["Logic Integrated Circuits"], Moscow, Sovetskoye Radio, 1970.

5. Baliyev K.A., Karmazinskiy A.N., Korolev M.A., "Tsifrovyye integral'nyye skhemy na MDP tranzistorakh" ["Digital Integrated Circuits Using MOS Transistors"], Moscow, Sovetskoye Radio, 1971, pp 15-27, 252-290, 355-362.

6. Crawford R., "Skhemnyye primeneniya MOP transistorov" ["Circuit Applications of MOS Transistors"], Translated from the English, Edited by M.S. Sonin, Moscow, Mir, 1970, pp 9-21, 106-111, 126-134.

7. Shebanin V.V., Tyukhin A.A., Tomov V.I., "Integral'nyye funktsional'nyye uzly dlya zapominayushchikh ustroystv" ["Functional Integrated Circuits for Memories"], Moscow, Sovetskoye Radio, 1976, pp 7-27 (the series "Elementy radioelektronnoy apparatury" ["Radioelectronic Equipment Components"], No. 3).

8. Akuchenko N.A., Sokolova G.N., "Tendentsii razvitiya zapominayushchikh ustroystv" ["Developmental Trends in Memories"], ZARUBEZHNAYA ELEKTRONNAYA TEKHNIKA [FOREIGN ELECTRONICS ENGINEERING], 1974, No. 3.

9. Staros F.G., Krayzmer L.P., "Poluprovodnikovyye integral'nyye zapominayushchiye ustroystva" ["Semiconductor IC Memories"], Leningrad, Energiya, 1973.

10. Mur, "Mikroprotsessory i tekhnologiya integral'nykh skhem" ["Microprocessors and Integrated Circuit Technology"], TIIER [PROCEEDINGS OF THE IEEE], 1976, No. 6, pp 5-11.

Ferkhofshtadt, "Otsenka tekhnologii mikroprotsessornykh BIS" ["An Evaluation of Microprocessor LSI Technology"], TIIER, 1976, No. 6, pp 5-11.

11. Shilin V.A., "Tsifrovyye elementy i ustroystva na priborakh s zaryadovoy svyaz'yu" ["Digital Components and Devices Using Charge Coupled Devices"], ZARUBEZHNAYA ELEKTRONNAYA TEKHNIKA, 1974, No. 5, pp 3-4, 47-84.

12. Grinkevich V.A., "Mikroprotsessornyye komplekty BIS" ["LSI Microprocessor Sets"], ELEKTRONNAYA TEKHNIKA. SER. 6. MIKROELEKTRONIKA [ELECTRONICS ENGINEERING. SERIES 6. MICROELECTRONICS], 1976, Vol. 5, No. 2.

13. Val'kov V.N., Il'yushenko Yu.M., "Tsifrovyye integral'nyye skhemy, mikroprotsessory i mikro-EVM" ["Digital Integrated Circuits, Microprocessors and Microcomputers"], Edited by V.M. Proleyko, Moscow, Sovetskoye Radio, 1977, pp 49-60 ("Electronics" Library").

14. Aleksenko A.G., "Osnovy mikroelektroniki" ["Microelectronics Fundamentals"], Moscow, Sovetskoye Radio Publishers, 1977.

15. Al'tman L., "Perspektivy primeneniya odnokristal'nykh mikroprotsessorov" ["Prospects for the Application of Single Chip Microprocessors"], ELEKTRONIKA, 1974, No. 8, pp 26-34.

CHAPTER FOUR. ANALOG INTEGRATED CIRCUITS

4.1. Function and Application

Analog integrated circuits (AIS) are intended for real time signal processing where the output information of such an IC is similar (analogous) to the input signal. The following analog IC's are treated in this chapter: operational amplifiers; integrated circuit voltage comparators; integrated circuits which multiply analog signals; IC's for radio receivers; switching circuits; analog to digital and digital to analog converter IC's as well as integrated circuit regulators. In contrast to devices using digital IC's, each analog device has a considerably greater number of electrical parameters which make it possible to come up with a complete model of it. Moreover, the application of an analog IC is always specific: a large number of ultimate operating modes with respect to the power supply, signals and load must be specified. In contrast to digital IC's, a certain number of external components must be connected to each analog IC where these components establish the requisite transfer function of the device. The major types of analog circuits will be treated in this chapter and examples will be given for the design of radio equipment assemblies around these circuits.

4.2. Operational Amplifiers

An operational amplifier is an amplifier by means of which one can construct equipment assemblies having parameters which are dependent practically on the properties of the negative feedback circuit in which it is inserted.

The major function of an operational amplifier (OU) is the construction of circuits with a fixed gain and precisely synthesized transfer function. Op amps can be used to construct the most diverse hardware: voltage regulators, signal generators, video amplifiers, active filters, scaling, logarithmic response, differentiating, integrating and other amplifiers. A standard general purpose amplifier can be used in 100 to 150 circuit configurations.

The circuits for the first IC op amps were similar to their discrete prototypes (with certain limitations imposed by the specific features of the integrated circuit structure). However, by the end of the 1960's, IC designers began to actively use new integrated circuit structures and circuit design approaches to improve op amp performance [1, 2].

Regardless of the complexity of the basic circuit configuration, an integrated circuit op amp consists of an input differential amplifier, a voltage amplifier, a DC level shift circuit and an output power amplifier. Depending on the number of stages which make the major contribution to the overal gain, a distinction is drawn at the present time between three state and two stage op amps. The op amps which were developed at first had a three state structure. Beginning in the 1970's, op amps have been designed using only a two stage configuration in which states 2 and 3 have been combined.

The first stage of an op amp is designed in a differential amplifier configuration. A reduction in errors, amplification of the DC component of the signal and an increase in the input stage impedance are achieved by virtue of the input stage operating in a microampere current mode of the emitters. All of the input parameters of op amps are governed by the properties of its differential input stage.

The second stage of the first op amps was designed in a simple differential configuration. When a two-state amplifier circuit is used, the second state has a common emitter (OE) configuration. Besides boosting the gain, the second stage provides for impedance matching of the input and final stages. In order to eliminate the DC voltage component which occurs in an op amp circuit with direct coupling of its stages, a special DC level bias (shift) circuit is additionally introduced. There is no special shift circuitry in two stage op amps, since its function is automatically performed by the second stage.

The final (output) stage of an op amp serves to match the high output impedance of the amplifier stages to a low resistance load, i.e., makes it possible to obtain a low output impedance for the op amp. It is usually designed in a push-pull configuration operating in either the class AB or B mode. A class A output stage is sometimes used in very simple op amp circuits.

Operational amplifiers are usually powered from two symmetrical supplies which provide positive and negative output voltage amplitudes which are equal in value. For the majority of modern op amps, the supply voltages can vary "arbitrarily" in a rather wide range (frequently from ± 3 to ± 15 volts), something which makes it possible to construct both economical circuits and amplifier with a large (or asymmetrical) output signal amplitude. The possibilities for op amp applications depend on its electrical parameters. More than 30 parameters are needed to completely specify op amp performance [1-4], where these parameters make it possible to create a so-called parametric model. This model makes it possible to explain operational amplifier quality without additional testing.

Knowledge of the major parameters of integrated circuit op amps makes it possible for designers to design a circuit without long term breadboarding and to prevent op amp operation in an impermissible mode, so as to reduce the probability of failure. Thus, an exhaustive parametric mode allows for the rapid selection of the requisite type of operational amplifier for a given assembly.

Operational amplifiers are characterized by the gain, which is equal to the product of the gains of all of their stages:

$$K_U(\omega) = \prod_{n=1}^{3} K_n N$$

where $K_U(\omega)$ is the voltage gain of the op amp without feedback; K_n is the gain of an elementary stage; ω is the frequency and N is the number of stages.

The DC gain of several integrated circuit op amps reaches $5 \cdot 10^6$, but it falls off with an increase in frequency. The amplitude-frequency response of an op amp is composed of the frequency characteristics of the individual stages operating with various currents and loads. Each amplifier stage has its own time constant and can be represented in the form of the equivalent RC network. For this reason, the

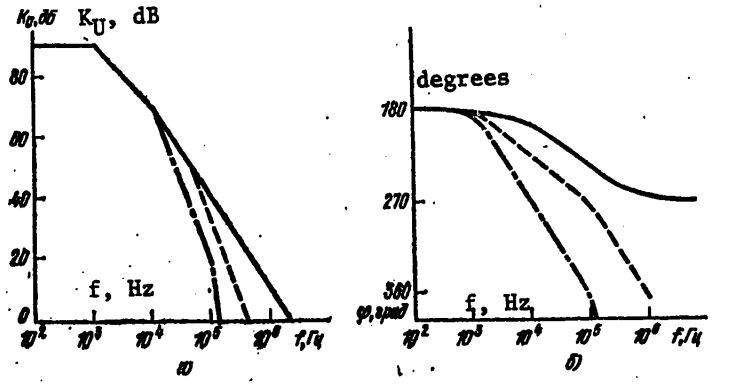


Figure 4.1. The overall amplitude-frequency (a) and phase-frequency (b) response for single stage (solid curves), two-stage (dashed curves) and three stage (dashed and dotted curves) operational amplifiers.

overall amplitude-frequency response (AChKh) of an op amp is approximated in general form by a Bode plot with several salient points (Figure 4.1a). Each stage introduces a phase shift of 90° at the high frequency; for this reason, the phase response of an op amp depends on the number of stages (Figure 4.1b).

Because of the fact that there is a planned phase shift in the signal of 180° at the output of an op amp for the operation of the feedback loop, the overall phase shift in an amplifier looped with negative feedback (OOS) reaches 360° at some particular high frequency. And if the product of the amplifier open loop gain times the negative feedback transmission gain at this frequency exceeds (or is equal to) unity, then this causes the self-excitation of the circuit.

Stable frequency and pulse transfer characteristics are achieved through the use of amplitude-frequency response equalization. For this, capacitive negative feedback loops are introduced which change the slope of the amplitude-frequency response of the closed loop system down to a rolloff rate of 20 dB/octave, which characterizes a stable first order section. A single stage (ultimate phase delay of 90°) would be ideal in terms of op amp stability, but its gain is insufficient (no more than 1,000). One equalizing capacitor in all is needed to stabilize a two state op amp. Three-stage operational amplifiers can be equalized by using two outboard capacitors (or two RC networks). It is difficult to stabilize op amps with more than three stages of amplification without substantially limiting their bandwidth.

An important parameter of op amps is the input impedance. A distinction is drawn between two types of input resistances: the signal input resistance, i.e., that observed between the op amp inputs (the so-called differential input resistance),

and the in-phase signal input resistance [common mode rejection] (resistance between the input and ground). The differential input resistance is defined by the expression:

$$R_{in\ dif} = \Delta U_{in}/\Delta I_{in} = 2\phi_T/I_b \approx 2\phi_T/I_{in},$$

where ΔU_{in} is the voltage change between the op amp inputs; ΔI_{in} is the change in the input current, ϕ_T is the temperature potential (at 300 °K, ϕ_T = 26 mV), I_b is the base current of the input transistor and I_{in} is the input bias current for the operational amplifier (taken from a table of its parameters).

The in-phase input signal resistnce ($R_{in\ ph}$) is defined as the change in the input current with the action of an in-phase input voltage:

$$R_{in\ ph} = \Delta U_{ph\ in}/\Delta I_{in}$$

where $\Delta U_{ph\ in}$ is the increments in the in-phase input voltage between the input and ground.

The input differential resistance falls in a rangeof 10 Kohm to 10 Mohm for bipolar op amps while the in-phase resistance exceeds 100 Mohms. Because of the differn-tial input, an op amp amplifies the difference input voltage and should completely suppress the in-phase voltage. However, an op amp does not completely suppress the in-phase signal and thereby introduces an error into the output signal. The parameter "in-phase signal suppression factor" ($K_{os\ sf}$) [common mode rejection ratio, CMRR] reflects this property of an amplifier. It makes it possible to compare various types of operational amplifiers and to also estimate the error introduced by the op amp, and is defined as the ratio of the op amp voltage gain to the gain for in-phase input voltages.

The difference in the base-emitter voltage drops of the input integrated circuit transistors, and to a lesser extent, the scatter in the nominal values of the remaining components of the operational amplifier lead to the apperance of DC voltage at the output in the absence of ansignal at the input. In order to set the zero level at the op amp output, it is necessary to apply a certain balance (bias) voltage, Ubias, between the op amp inputs.

All of the above mentioned op amp parameters depend on temperature. The tempera-ture drifts in the bias voltage and the input current differences exert the major influence on the error in the function realized by the op amp. The temperature drift takes the form of a change in the voltage or current with a change in the ambient temperature by 1 °C. These changes are superimposed on the input signal, as a result of which, the error voltage is summed, while the error current yields a voltage drop across the internal resistance of the signal source.

All operational amplifiers are designed for an output current (I_{out}), which determines the minimum resistance of the load at the nominal output voltage. Exceeding the given current can cause the op amp to fail.

The output impedance of an operational amplifier is defined by the impedance of its output stage and amounts to 20 to 20,000 ohms (depending on the circuit design and the function of the op amp). The output impedance exerts great influence on the output signal amplitude, especially when the amplifier operates into a low load impedance.

As was stated above, an op amp can perform various functions, which are determined by its feedback. A distinction is drawn between basic circuit configurations for op amps, looped by negative feedback: inverting and noninverting.

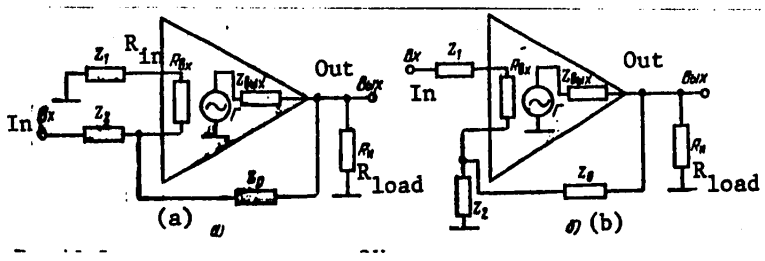


Figure 4.2. Basic circuit configurations for operational amplifiers.

a. Inverting;
b. Noninverting.

In order to simplify circuit design and analysis, the concept of an "ideal" operational amplifier is introduced, which possesses the following properties: the open loop gain of the amplifier K_0 tends to infinity, the rolloff of its frequency response is 20 dB/octave, the input impedance of the op amp tends to infinity, the output impedance approaches zero and the amplifier does not introduce any errors in the DC component gain.

When an op amp is used as an inverting amplifier (Figure 4.2a), the phase of the output signal is shifted through 180° relative to the phase of the input signal. The transfer function of this circuit (when U_{bias} = 0, ΔI_{in} = 0, CMRR = ∞ and R_{load} = ∞) has the form:

$$K_{U\,i} = U_{out}/U_{in} \approx -Z_0/Z_2$$

where Z_0 is the negative feedback impedance and Z_2 is the impedance of the signal source.

A noninverting operational amplifier configuration (Figure 4.2b) is used in those cases where it is necessary to match a source having a high impedance to a signal processing circuit having a low input impedance. In this case, the phase of the output signal duplicates the phase of the input signal. The transfer function of an ideal operational amplifier in a noninverting configuration has the form:

$$K_{U\ n.i.} = U_{out}/U_{in} \approx 1 + Z_0/Z_2$$

Since the value of the gain for integrated operational amplifiers falls in a range of $5 \cdot 10^3$ to $5 \cdot 10^6$, in practice, the error arising in many cases due to the idealization of this parameter ($K_U \to \infty$) may be disregarded. However, one may not disregard the errors from the DC component shift which occur because of the difference in the base-emitter voltages of the input transistors and because of the flow of the input currents of the op amp through the signal source resistance, since they can even exceed the input signal level.

The input currents (I_{in}) of operational amplifiers are due to the base bias currents of the input bipolar transistors (or the leakage currents of the gates for operational amplifiers with field effect transistors at the input). The input currents of bipolar transistors are needed to provide for the operating mode (supply bias) of the input stage and have a value of from 50 nA up to 5 μA. Operational amplifiers with field effect transistors at the input have input currents of less than 1 nA (admittedly, in a limited range of temperatures).

Because of the nonidentical nature of the characteristics of the input stage transistors, the base currents can differ from each other by 20 to 30 percent and introduce a substantial error even when the signal source resistances are equal. The input current difference parameters (ΔI_{in}) shows by how much one input current may differ from another. To reduce this fraction of the error, the internal resistance of the signal source should be chosen as low as possible.

The dynamic characteristics of operational amplifiers are estimated by means of two parameters: the rate of rise of the output voltage $v_{U\ out}$ and its settling time (t_{set}). The rate of rise of the output voltage is understood to be the ratio of the change in the output voltage from 10 to 90% of its nominal value to the time over which this change has taken place, with a stepwise change in the input voltage:

$$v_{U\ out} = (U_{0.9} - U_{0.1})/(t_{0.9} - t_{0.1})$$

The settling time is defined as the time interval during which the op amp output voltage changes from the time of the first intersection of the 10 % level until the final attaining of the 90 % level (of the nominal value) and primarily characterizes the pulse stability of an operational amplifier.

By employing idealized operational amplifier characteristics, one can analyze various op amps configurations in a simple manner. Idealization makes it possible to derive two rules which may be used for the analysis and synthesis of circuits based on operational amplifiers: 1) No current is taken from the signal source at the input terminals of the op amp (a consequence of the fact that $R_{in} \to \infty$); 2) The voltage across the inputs of an operational amplifier looped by negative feedback is practically equal to zero (a consequence of the fact that $K_U \to \infty$).

We shall cite two examples to illustrate the application of these rules. We shall analyze the circuit of an adder (Figure 4.3a). By using rules 1 and 2, we calculate the transfer function of this circuit. First of all, since the current from the signal source is not branched off to the op amp input, the sum of the currents of all sources flows through the negative feedback circuit: $I_1 + I_2 + I_3 = I_0$. Secondly, because of the fact that the voltage across the inputs of an operational amplifier looped by negative feedback is equal to zero, the voltage at point A is also equal to zero and the preceding equation for the current can be rewritten in the form:

$$\frac{U_1}{R_1} + \frac{U_2}{R_2} + \frac{U_3}{R_3} = \frac{U_{out}}{R_0}$$

The fact that the output voltage of the operational amplifier, U_{out}, may be measured both relative to the "true" ground and relative to "signal ground" (point A) has been taken into account here. But in the latter case, this means that the output voltage is applied to the feedback resistor through which the current $I_0 = U_{out}/R_0$ flows. If the nominal value of the resisters are $R_1 = R_2 = R_3 = R_0$, then the circuit operates as an inverting adder:

$$U_{out} = -(R_0/R_R)(U_1 + U_2 + U_3)$$

We shall not consider the circuit of a logarithmic amplifier (Figure 4.3b). The p-n junction of a transistor is usually employed as the element having a logarithmic response. We shall assume that the voltage across the p-n junction is equal to $U_{p-n} = K \ln(I_{p-n})$, where K is a constant and I_{p-n} is the junction current. In accordance with the procedure presented here: 1) No current is branched off to the op amp input, and for this reason, $I_{in} = I_{p-n}$; 2) Using the "unofficial ground" potential, one can calculate that $I_{in} = U_{in}/R$, and consequently, $U_{out} = U_{p-n} = K \ln(U_{in}/R)$, i.e., the amplifier can take the logarithm of the input voltage on a particular scale.

As a result of the idealization of operational amplifier parameters, errors occur when constructing equipment based on them which become less, the closer the parameters of the actual op amp are to the ideal. Operational amplifier designers strive to bring the op amp parameters close to the ideal ones: to increase the gain, the input impedance, the bandwidth and the response speed. In this case,

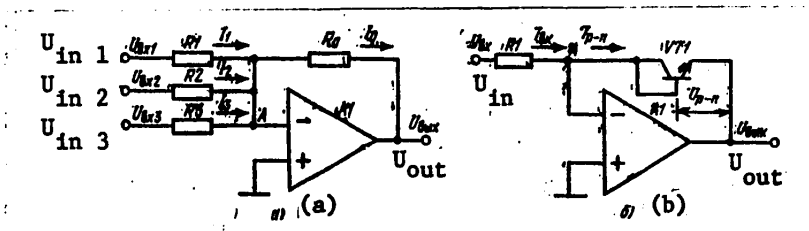


Figure 4.3. Examples of operational amplifier circuit configurations.

a. Adder circuit;
b. Logarithmic amplifier circuit.

efforts are made through the use of new circuit designs and especially, production process techniques to reduce the values of the bias voltage, the input currents and the drift in them as well as the power consumption of the device.

An entire series of semiconductor op amps which can broken down into four groups has been created as a result of the evolution of the circuit design and production process solutions: the bulk of the products are general purpose operational amplifiers which make it possible to construct equipment having an overall error on the order of 1%; precision (instrumentation) operational amplifiers which have a very high gain, as well as guaranteed low levels of drift and noise, which makes it possible to realize assemblies which operate with an error of no worse than tenths of a precent. Moreover, the demand is high for operational amplifiers intended for the construction of wideband amplifiers with a slew rate of more than 50 V/μsec, as well as micropower op amps which consume less than 1 mA from the power supplies and are designed for use in economical equipment (frequently powered by batteries).

4.2.1. Operational Amplifiers with a Two Stage Structural Configuration

The first operational amplifiers of the 140 UD1, 140 UD5 and 153UD1 types had a three stage configuration because of the fact that the technology did not at first make it possible to obtain high resistance loads, or good p-n-p transistors. For three-stage amplifiers, numerous auxiliary components are needed for frequency equalization, balancing, overload protection at the input and output as well as protection against flip-flop operation. Achievements in the field of technology and circuit design have made it possible at the present time to develop operational amplifiers with a two stage structure, since n-p-n and p-n-p transistors can be produced in one production process cycle, where these transistors are used both as an amplifier and as an active load. Two stage op amps operate with lower supply currents and have an increased gain.

Because of the use of integrated circuit input transistors with a high gain in such operational amplifiers, the levels of the input currents are reduced. Moreover, the active loads on the amplifier stages, which are used instead of high resistance resistors do not require large voltage drops to obtain the requisite operating modes, something which makes it possible to provide for stable op amp operation both at low (±3 volts) and high (±15 volts) supply voltages, maintaining the high gain in this case as well as the output signal amplitude which is proportional to the supply voltages. A reduction in the number of amplifier stages down to two also reduces the number of salient points in the amplitude-frequency response curve down to two, and in the final analysis, reduces the number of frequency equalization components to a single capacitor.

Two stage operational amplifier circuits are protected against overloads at the input and output, and some of them also have internal frequency equalization components, which makes it possible to reduce the number of outboard components down to a single balancing resistor. All of the op amps treated in the following are structurally packaged in circular packages with eight leads. The socket configuration of these opartional amplifiers basically conforms to the pin configuration of the 153UD1 op amp. This has been done so that obsolete types of operational amplifiers can be replaced without doing any additional work on equipment. The electrical characteristics of operational amplifiers are given in Table 4.1.

The 153UD2 General Purpose Operational Amplifier. Op amps of this type (Figure 4.4a) have a complex output stage (transistors VT5, VT6, VT9 and VT10), which is powered by the stable current of transistor VT1. The base-emitter voltage of this transistor is controlled by a regulator (transistors VT2...VT4 and resistors R1...R6). Transistors VT6 and VT10 have two collectors; one of the transistor collectors which is shorted to the base, takes the form of a diode which regulates the current of the "operating" collectors in a broad range of supply voltages. The dynamic resistances of the collectors of transistors VT7 and VT11 serve as high resistance active loads for the first stage. Transistor VT8 provides for a constant bias at the emitter-base junction of transistors VT11 and VT7 by means of resistor R7, and it additionally serves as a single inverter in the transition circuit from the differential output of the first stage to the single ended input of the second. Resistor R8 is intended to compensate for the bias voltage, which can be balanced by inserting a variable resistor between pins 1 and 5. Transistors VT13 and VT14, which are connected in a Darlington configuration, form the second stage, the dynamic load on which is the stable current generator (GST), which is formed by the open collector output of transistor VT16. Transistor VT16 has two collectors, one of which is shorted to the base, which makes it possible to effectively stabilize the current of the second collector of resistor of VT16. The bias is set at the base of the transistor by means of the current of the collectors of transistors VT2 and VT3 from the regulator circuit. The second collector current of transistor VT16, in passing through the emitter-base junctions of transistors VT17 (in a diode configuration) and VT15, produces the bias for the operating point of the output stage in the AB mode and powers the second amplifier stage.

The push-pull output stage consists of an emitter follower using an n-p-n transistor (VT20) and an emitter follower using a composite p-n-p transistor

TABLE 4.1. Electrical Parameters of Operational Amplifiers

Parameters	140UD1A	140UD1B	140UD2	153UD1	140UD7	140UD6	140UD	544UD1	153UD2
(1) Zero bias voltage, U_{bi}, millivolts	7	7	5	5	4	5	2	15	05
(2) Bias voltage drift, $\Delta U_{bi}/\Delta T$, $\mu V/°C$	20	20	20	30	6	20	15	20	20
(3) Input currents, I_{in}, nA	$5 \cdot 10^3$	$8 \cdot 10^3$	700	600	200	30	2	0.15	500
(4) Input current difference, ΔI_{in}, nA	$1.5 \cdot 10^3$	$1.5 \cdot 10^3$	200	250	50	10	0.2	0.05	200
(5) Input current difference drift, $\Delta\Delta I_{in}/\Delta T$, nA/°C	30	30	3	17	0.4	0.1	$2.5 \cdot 10^3$	-	2
(6) Voltage gain, K_U, V/mV	0.9	2	35	20	50	70	50	50	20
(7) CMRR, $K_{os\ sf}$, dB	60	60	80	65	70	80	85	70	70
(8) Slew rate, $v_{U\ out}$, V/μsec	0.2	0.5	0.12	0.06	10	2.5	0.25	2	0.5
(9) Unity gain freq., f_T, MHz	5	5	2	1	0.8	1	-	1	1
(10) Settling time, t_{set}, μsec	0.8	1	1.5	-	-	-	-	-	2
(11) Input impedance, R_{in}, Kohm	4	4	300	100	400	2000	30,000	10^4	300
(12) Output impedance, R_{out}, ohms	700	700	100	200	-	-	-	-	-
(13) Maximum output current, I_{out}, mA	3	3	13	5	20*	25*	-	20*	-
(14) Maximum output voltage, $U^{\pm}_{out}$, volts	3	6	10	10	11.5	11	13	10	11
(15) Maximum input voltage, U^{+}_{in}, volts	1.5	1.5	4	5	124	30	-	10	30
(16) Maximum in-phase input voltage, $U^{+}_{in\ ph.}$, volts	3	3	6	8	12	11	13.5	10	12
(17) Power supply voltage, $U_{i.p.}$, volts	-6.3	12.6	12.6	15.0	15.0	15.0	15.0	15.0	15.0
(18) Current consumption, I_{con}, mA	4.2	8	16	6	2.8	2.8	0.6	3.5	3
(19) Internal equalization	No	No	No	No	Yes	Yes	No	Yes	No
(20) Short circuit output protection	"	"	"	"	"	"	"	"	Yes

TABLE 4.1 [continued]:

Parameters	153UD5	153UD4	140UD10
(1)	2.5	5	4
(2)	5	50	-
(3)	125	400	250
(4)	35	15	50
(5)	0.50	3	-
(6)	125	2	50
(7)	94	70	80
(8)	-	0.1	+50; -20**
(9)	-	1	15
(10)	-	-	-
(11)	10^3	200	10^3
(12)	150	-	-
(13)	5	-	-
(14)	10	4	-
(15)	5	2	-
(16)	13.5	5	11.5
(17)	15.0	6.0	15.0
(18)	-	0.8	8
(19)	No	No	No
(20)	Yes	Yes	-

* The value of the short circuit current is given;
** Plus is for a positive output voltage; Minus is for a negative output voltage.

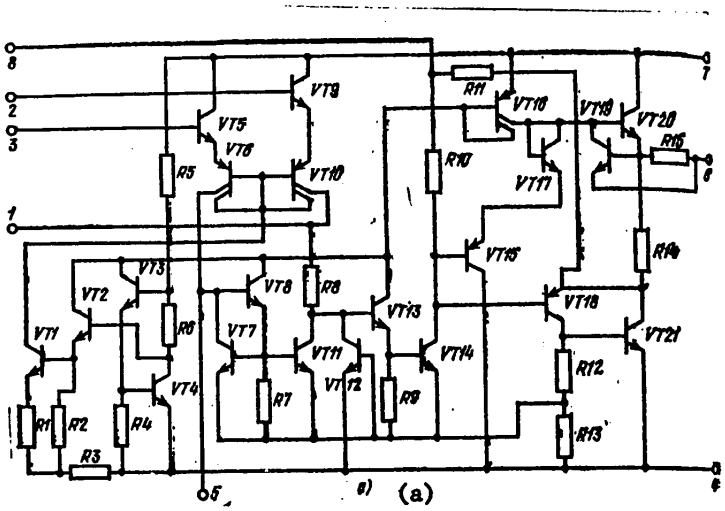
(transistors VT21 and VT18). Transistor VT19 performs the function of a current limiter; it turns on when the current through transistor VT20 exceeds 25 mA. Transistor VT21 is protected against a short circuit current in the load by a 50 ohm resistor. Transistor VT12 serves to protect the output stage against flip-flop mode operation. The plot of the gain as a function of frequency for the 153UD2 operational amplifier (Figure 4.4b) is equalized with a single capacitor.

An original circuit design as well as the use of an active load and an internal regulator have made it possible to cut the current consumption of the 153UD2 operational amplifier in half (Figure 4.5) as compared to the 153UD1 op amp. In this case, the range of in-phase and differential input voltages has increased, while the possible range of supply voltages has been reduced down to ± 3 volts. The 153UD2 op amp is protected against short circuits at the output and has a simple frequency equalization circuit.

The 153UD2 op amp is produced in an encapsulated and unencapsulated variant. The designation of the unencapsulated variant is 740UD5-1. Additionally, domestic industry is producing a number of unencapsulated linear integrated circuits (Table 4.2).

The 140UD7 Operational Amplifier. This type of operational amplifier (Figure 4.6a) is a simplified variant of the 153UD2 op amp circuit. The 140UD7 amplifier has a complex input stage, the arms of which are designed in a complementary common collector--common base circuit configuration using transistors VT1, VT2, VT6 and VT8. A current difference regulator [2] using transistorsVT9 and VT10, the bias to the bases of which is set by means of transistors VT5 and VT12 (used as diodes) is employed to maintain the output stage currents constant.

The voltage picked off of the first stage is amplified by the second stage (transistors VT14 and VT16, which is loaded into the large internal impedance of the stable current generator and the input impedance of dual emitter transistor VT18



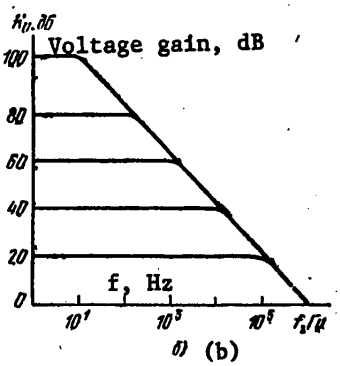


Figure 4.4. The 153UD2 operational amplifier.

a. Basic electrical schematic;
b. The gain plotted as a function of frequency.

which is connected in parallel with it. The stable current generator is designed around the dual collector transistor VT15, which is stabilized by transistor VT11 used as a diode. The output stage, which operates in class AB, is designed around transistors VT23 and VT24. Transistor VT17 (used as a diode) and transistor VT19 bias the operating point of the output stage transistor. Transistors VT21 and VT22 are protected against output stage overloading. They turn on bu virtue of the voltage drop across the resistors inserted in the emitter-base circuit of the given transistors. Transistor VT13 and the second emitter circuit of transistor VT18 are intended to protect the output stage against flip-flop operation. The circuit has an internal equalization capacitor C1 with a nominal value of 30 pF, and for this reason, the amplitude-frequency response of the op amp (Figure 4.6b) is completely equalized. The slope of the amplitude-frequency response (-20 dB/oct) and the constant shift at high frequency which is equal to 90° (Figure 4.6c) allow for the use of the operational amplifier as a follower without additional frequency equalization components (Figure 4.6d). To increase the slew rate of the output voltage

TABLE 4.2 Unencapsulated Linear IC's Produced by Domestic Industry

Designation	Major Function	The Encapsulated IC Series (For Reference)
	Operational Amplifiers. Direct Current Amplifiers	
129NT1A-1... 129NT1I-1	Basic differential amplifier circuit	159NT1
710UD11	Operational amplifier	153UD4
740UD1A-1, 740UD1B-1	The same	153UD1A, 153UD1B
740UD5-1	" "	153UD2
740UD4-1	" "	140UD6
740UD3-1	" "	140UD1
	***	
	Switches	
714KN1A-1... 714KN1V-1	Analog voltage switch with control circuit	-
714KN2A-1, 714KN2B-1	Differential analog voltage switch	-
716KN2B-1	Control circuit for electronic switches in the 273 series of integrated circuits	-
716KT1-1	Dual bipolar chopper for switching analog signals	-
743KT1A-1... 743KT1G-1	Series integrated circuit chopper	101KT1A 101KT1G
K762KT1A-1, K762KT1B-1	Integrated circuit chopper	K162KT1A, K162KT1B

up to 10 volt/μsec, a provision is made for reducing the degree of equalization. For this, capacitor C1 with a capacitance of 150 pFd is connected to pin 8 (as shown in Figure 4.6e). The equalization circuit for the op amp consists of one external variable resistor which is connected to pins 1 and 5.

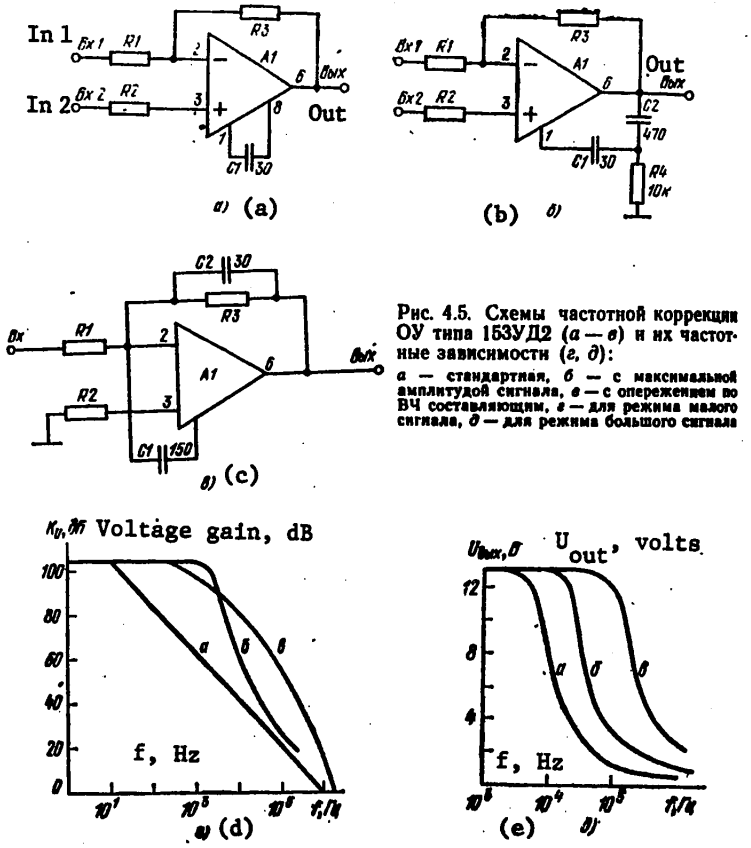


Рис. 4.5. Схемы частотной коррекции ОУ типа 153УД2 (*а — в*) и их частотные зависимости (*г, д*):
а — стандартная, *б* — с максимальной амплитудой сигнала, *в* — с опережением по ВЧ составляющим, *г* — для режима малого сигнала, *д* — для режима большого сигнала

Figure 4.5. Frequency equalization circuit for the 153UD2 op amp (a-c) and their frequency responses (d, e).

a. Standard;
b. With the maximum signal amplitude;
c. With a lead with respect to the high frequency components;
d. For the small signal mode;
e. For the large signal mode.

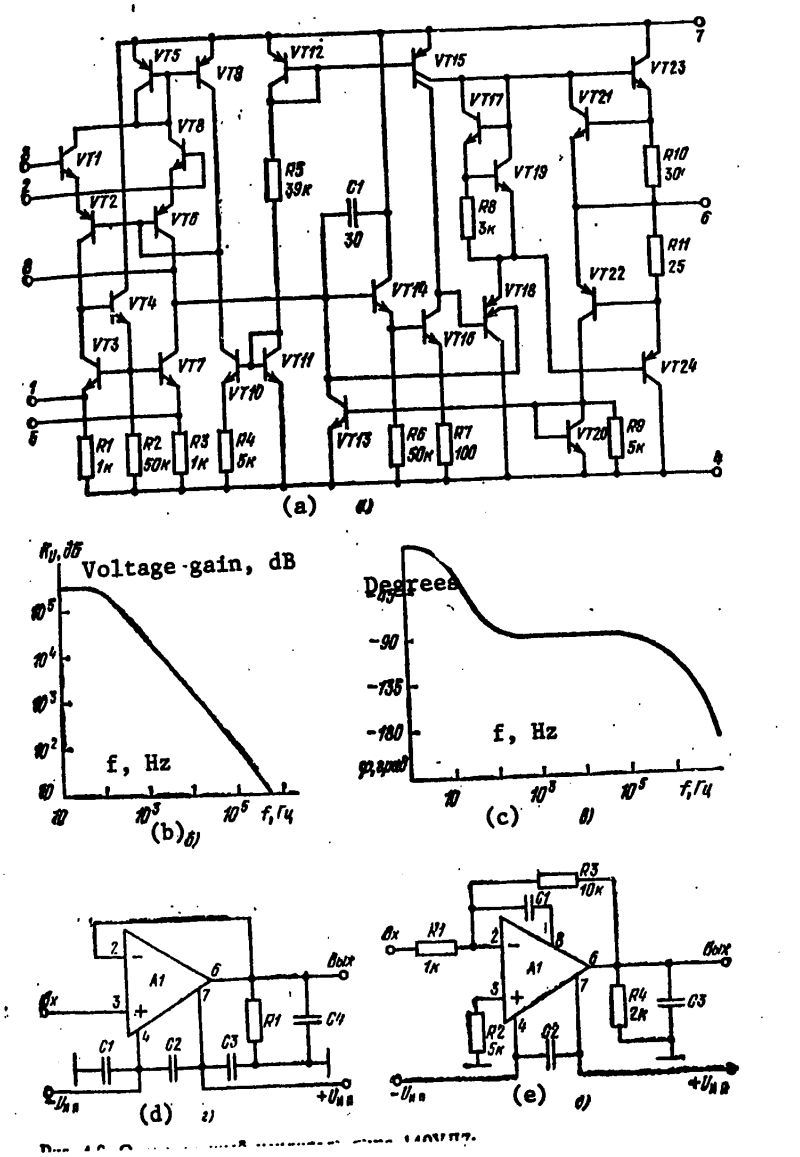


Figure 4.6. The 140UD7 operational amplifier.

a. Basic electrical schematic;
b. The gain as a function of frequency;
c. Phase-frequency response;
d. Circuit configuration for a noninverting follower mode;
e. Circuit configuration for the equalizing capacitance to improve the rise time of the output voltage.

4.2.2. Amplifiers with Field Effect Transistors at the Input

A pair of matched field effect transistors is frequently used to reduce the input currents of an operational amplifier down to the level of the gate leakage currents of the FET's (i.e., down to a value of 10^{-9} A). The improvement in the fabrication technology of IC's has made it possible to obtain bipolar and high quality field-effect transistors in a single production process cycle (on one chip). This, in turn, has made it possible to create semiconductor op amps which have an input impedance at a level of $10^{11}...10^{13}$ ohms, and consequently, an initial bias current approaching 0.1 nA. One of the amplifiers with field effect transistors at the input is the 544UD1 operational amplifier (Figure 4.7). The op amp is designed in a two stage configuration. The input stage takes the form of a differential amplifier with source followers in the form of a matched pair of n-type FET's (VT1 and VT5), working into active loads (transistors VT2 and VT4). The active load provides for a high stage gain and an extended permissible range of of in-phase input voltages. Moreover, the use of field effect transistors makes it possible to feed in large differential input voltages. Internal frequency equalization is employed to improve the frequency response of the amplifier. The second stage and the level shift circuit (transistor VT8), which is designed around low frequency p-n-p transistors, are shunted by an equalization capacitance. The output stage and its bias circuit are designed in a manner similar to that of the 140UD7 op amp. The bias voltage balancing is accomplished relative to pins 1-8.

The favorable input characteristics make it possible to widely utilize the operational amplifier in integrator circuits, operating with large time constants and low values of the capacitances. However, the input currents of the field-effect transistors, which are the leakage currents, are greatly dependent on temperature. With a change in the temperature by 100 °C, the level of the input currents increases by two orders of magnitude and reaches tens of nanoamperes (Figure 4.7c). Moreover, op amps with FET's have large bias voltages (up to 30...50 mV) and a large temperature drift (40 μV/°C).

The factors enumerated above have forced op amp designers to seek out other ways of improving amplifier performance.

One can use transistors for which the current gain exceeds 5,000 to obtain a low value of the input current, i.e., so-called superbeta transistors [21, 25]. Transistors with an ultrahigh current gain are produced on the same chip where the conventional n-p-n transistors are located by means of supplemental emitter diffusion. However, the breakdown voltage of these transistors is reduced in this case. The combination of low voltage superbeta transistors with conventional n-p-n transistors has made it possible to more efficiently produce operational amplifiers with better drift input characteristics (bipolar superbeta transistors have resulting drift parameters better than those of FET's in a wide range of temperatures).

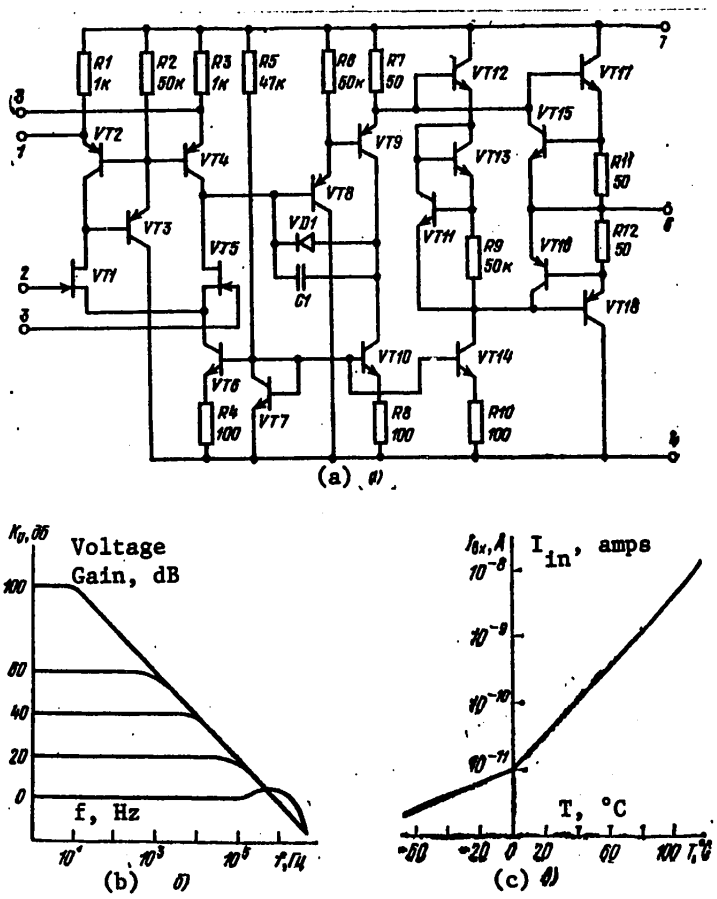


Figure 4.7. The 544UD1 operational amplifier.

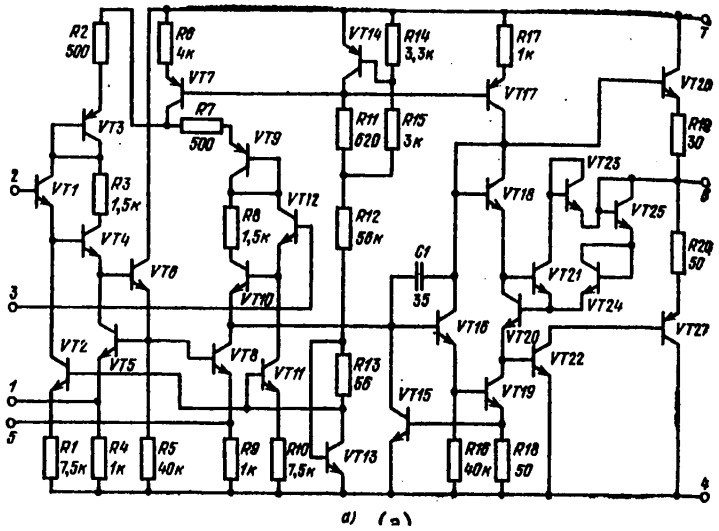
a. Basic electrical schematic;
b. Gain as a function of frequency;
c. The input currents as a function of temperature.

4.2.3. Amplifiers With Super-Beta Transistors

The 140UD Amplifier. This amplifier (Figure 4.8a) is designed as a two-state amplifier. The first complex stage (transistors VT1, VT4, VT10 and VT12) consist of a differential voltage follower (transistors VT1 and VT12), which controls the common emitter amplifier. To reduce the input currents of the operational amplifier, super-beta transistors VT1 and VT12 are used at the input. Transistors

VT4 and VT10 provide for a low collector-emitter voltage of the input transistors, as well as an almost zero voltage between the collector and the base of these transistors. Such a mode is necessary for reliable operation of transistors VT1 and VT12 as well as to reduce the temperature drift of the inverse currents of their collector junctions. The stable current generator (transistor VT7) sets the overall current for the input stage, while transistors VT2 and VT11 control the emitter currents of input transistors VT1 and VT12, and thereby stabilize the value of the input currents.

Transistors used as diodes are employed to increase the maximum differential voltage in both branches of the stage, where these transistors have a high breakdown voltage. The increase in the differential input resistance is accomplished by inserting R2 and R7 in series with the diodes (transistors VT3 and VT9), while resistors R4 and R9 are inserted in the emitter circuits of transistors VT5 and VT8 to balance the bias voltage at the op amp output.

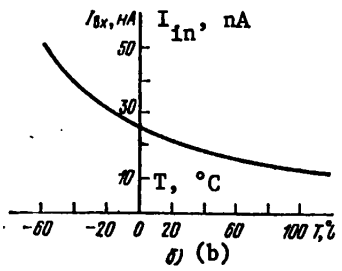


а) (a)

Figure 4.8. The 140UD6 operational amplifier.

a. Basic electrical schematic;

b. The input currents as a function of temperature.



б) (b)

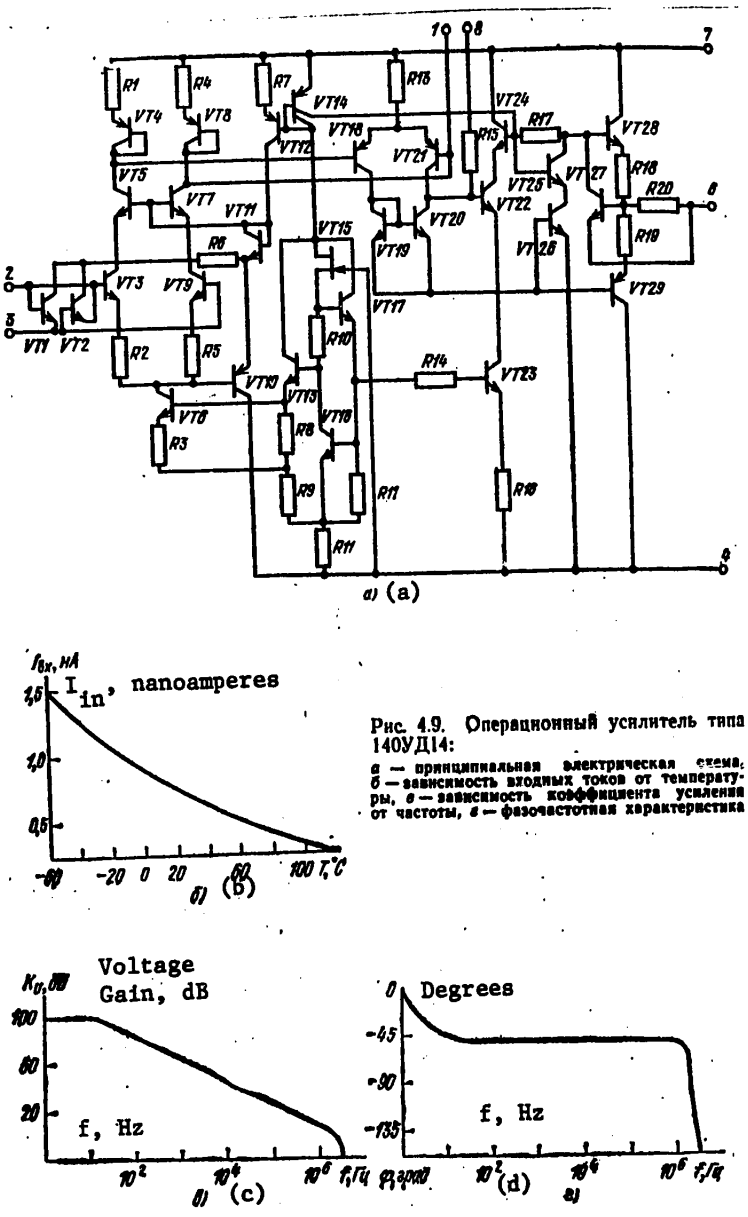


Рис. 4.9. Операционный усилитель типа 140УД14:
а — принципиальная электрическая схема; *б* — зависимость входных токов от температуры, *в* — зависимость коэффициента усиления от частоты, *г* — фазочастотная характеристика

Figure 4.9. The 140UD14 operational amplifier.

a. Basic electrical schematic;
b. The input currents as a function of temperature;
c. The gain as a function of frequency;
d. The phase-frequency response.

The introduction of local negative feedback (resistors R3 and R8) increases the speed and at the same time the stability of the circuit. The direct current mode is governed by the regulator which is designed around transistors VT13 and VT14. The second stage of the operational amplifer is a Darlington configuration (transistors VT16 and VT19). Transistor VT17, which biases the operating point of the output stage transistors in class B (through transistors VT18, VT20 and VT22). The output stage is designed around transistors VT22, VT27 and VT26. The overload protection circuitry uses transistors VT21, VT23, VT24 and VT25. It limits the short circuit output current to no more than 25 mA. Transistor VT15 protects the output stage of the op amp against flip-flop operation. The incorporation of internal frequency equalization in the second stage circuitry (capacitor C1) reduces the phase shift and provides for an amplitude-frequency response roll-off of 20 dB/oct up to the unity gain frequency (1 MHz). The use of super-beta transistors has made it possible to obtain low input currents (down to 30 nA), and what is most important, very good temperature stability of the input current (Figure 4.8b).

The 140UD14 Amplifier. In contrast to the 140UD6 operational amplifier, super-beta transistors are used in all stages in the 140UD14 op amp.(Figure 4.9a). The op amp is designed in a two stage configuration. Transistors VT3, VT5, VT7 and VT9 of the input stage are used in a cascode circuit. The bases of transistors VT5 and VT7 are connected through series connected transistors VT1 and VT2 to the bases of transistors VT3 and VT9. Thanks to this configuration, the super-beta input transistor VT3 and VT9 operate with a collector-base voltage close to 0. To increase the bandwidth, resistors R2 and R5 are inserted in the emitters of transistors of VT3 and VT9.

Transistors VT5 and VT7 have a large breakdown voltage and protect the low voltage super-beta input transistors against breakdown. Moreover, the emitter junctions of transistors VT1 and VT2, which are inserted between the bases of the input transistors in opposition to each other, protect the input stage against breakdown by large differential input voltages. The stable current generator using transistor VT6 provides for a regulated supply current to the input stage and thereby also clamps the level of the input currents. The bias voltage at the base of the stable current generator of the input stage is supplied from a voltage regulator (transistors VT13 and VT15-VT17, as well as resistors R8-R12). In a manner similar to the regulator in the 153UD2 operational amplifier, this circuit provides for constant bias throughout the entire range of supply voltages. The currents of transistors VT5 and VT7 are regulated by the input current difference regulator, where transistor VT11 (used as a diode) and transistor VT10 are employed.

The circuit of the second stage (transistors VT18 and VT21), the current of which is regulated by the DC level of the first stage collector voltage provides not only for the transition from the differential output of the second stage to the single input, but also for a high gain by virtue of the active load (transistors VT19 used as a diode and VT20), as well as for a shift in the DC level. Transistor V VT22 series to supply bias to the output stages.

The output stage of the amplifier is designed around n-p-n transistor VT28 and p-n-p transistor VT29. The stage is protected against an output short circuit to ground or to the power supply. The use of super-beta transistors in the 140UD14 amplifier has made it possible to obtain an input current level I_{in} of less than

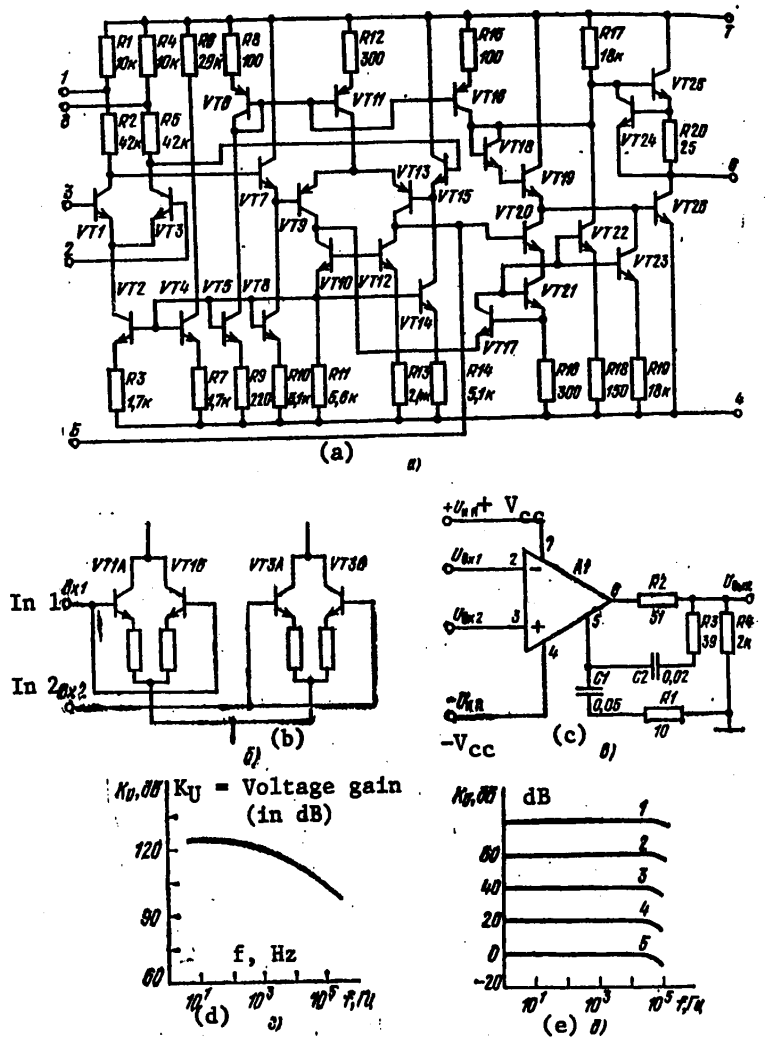


Рис. 4.10. Операционный усилитель типа 153УД5:

а — принципиальная электрическая схема, *б* — схема входного каскада, *в* — основная схема частотной коррекции, *г* — зависимость коэффициента усиления разомкнутого усилителя от частоты, *д* — зависимость коэффициента усиления от частоты, элементов обратной связи и частотной коррекции в режиме масштабного усилителя

220

Curve Кривая	ohms R_1, Ом	ohm R_2, Ом	pFd C_1, пФ	pFd C_2, пФ
1	10*	—	50	—
2	470	—	1000	—
3	47	—	10000	—
4	27	270	50000	1500
5	10	390	50000	20000

Figure 4.10. The 153UD5 operational amplifier.

a. Basic electrical schematic; b. Schematic of the input stage; c. Basic frequency equalization circuit; d. Open loop amplifier gain as a function of frequency; e. The gain as a function of frequency, feedback components and frequency equalization in a scaling amplifier mode.

1.5 nA throughout the entire temperature range (see Figure 4.9b). The amplitude-frequency response of the op amp is equalized by external equalization circuits (Figure 4.9c).

4.2.4. The 153UD5 High Precision Operational Amplifier

The 153UD5 operational amplifier (Figure 4.10a) belongs to the class of high precision op amps used for the construction of instruments. Its specific features are a low zero bias voltage (0.5 mV), low levels of drift and noise and a high gain (more than 10^6). But the major property of this operational amplifier is the fact that it makes it possible to maintain a high value of the closed loop gain of the operational amplifier with a high degree of precision (for example, one can obtain K_U = 1,000 ± 0.3%). The specific features of this parameter determine the basic circuit of the operational amplifier and the technology for its fabrication.

The input stage of the op amp is designed in the usual differential configuration. However, input transistors VT1 and VT3 take the form of a parallel connection of two transistors (Figure 4.10b) to reduce the drift. The first stage is supplied with current by the stable current generator (transistor VT2) and is loaded into identical resistors R1 + R2 and R4 + R5. The reduction of the thermal effect from the high power output transistor elements is achieved by the special arrangement of the input stage. Transistors VT1 and VT3 occupy a large area on the chip (approximately one-third of it) and are positioned crosswise to each other.

Op amp circuit designers have dispensed with the use of an active load on the input stage so as to reduce the zero bias voltage and the temperature dependence of the input characteristics. The increase in the input impedance of the second stage and the corresponding reduction of its impact on the input characteristics are achieved by designing the stage in a complex common collector--common emitter circuit configuration using transistors VT7, VT9 and VT13, VT15 which are well-matched with respect to their parameters. The stable current generators of the second stage (transistors VT10-VT12) provide for stability of the input currents and a high resistance load for the second stage. By converting the differential output to a single input, the active load impedance of the second stage provides for a high gain.

The third stage has an amplifying transistor VT20 (a common emitter stage) with a load in the form of a stable current generator (transistor VT16). Transistors VT18 and VT19 shift the operating point of the output power transistors VT25 and VT26 to class AB, which eliminates distortions in the output. Moreover, transistor VT19, which is used as an emitter follower, makes it possible to reduce the output impedance of the operational amplifier. The output current limiting in the case of a short circuit is provided by transistors VT23 and VT24, which prevent the overloading of transistors VT25 and VT26. Transistor VT23 limits the current consumption by the base of transistor VT26. The amplitude-frequency response of the op amp is corrected by two frequency equalization networks (Figure 4.10c). The plot of K_U as a function of frequency is shown in Figure 4.10d for the open loop amplifier, while the amplitude-frequency responses of the op amp used as a scaling amplifier are shown in Figure 4.10e.

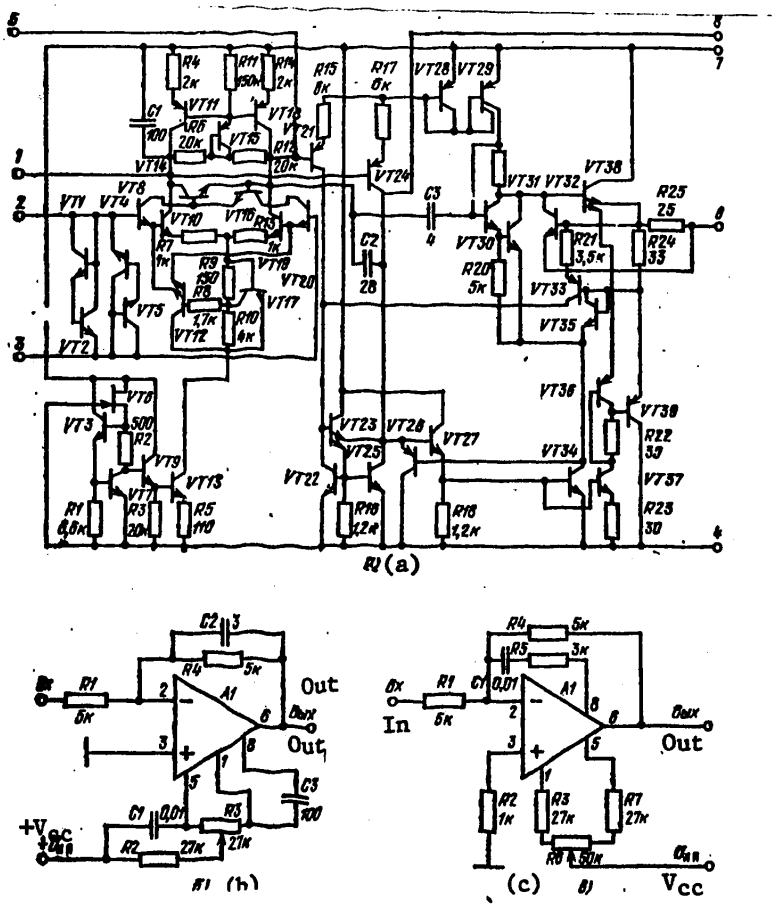


Figure 4.11. The 140UD10 operational amplifier.

a. Basic electrical schematic;
b,c. Frequency equalization circuits used to reduce the settling time and to increase the output voltage slew rate respectively.

4.2.5. High Speed Operational Amplifiers

The limited operational speed is one of the substantial drawbacks to standard op amps. General purpose amplifiers with equalization down to the unity gain level have a small signal bandwidth of about 1 MHz and an output voltage slew rate of up to approximately 0.6 V/μsec. But this drawback can be overcome if a high

frequency channel is incorporated in the op amp circuitry. There exist many methods of designing the high frequency channel, which are basically distinguished by the circuit configurations of the equalizing networks and the types of amplifier stages employed [5]. Although semiconductor op amps also possess low parasitic capacitances, they nonetheless cannot have a fast response without taking special steps, since one of the amplifier stages should be designed around an integrated circuit p-n-p transistor. The 140UD10 high speed operational amplifier (Figure 4.11a) has an output voltage slew rate of 50 V/μsec and a unity gain frequency of 15 MHz.

The good frequency parameters of the op amp were achieved as a result of using a high frequency channel in the circuit, through which the high frequency components "bypass" the slow p-n-p transistor. Moreover, by virtue of a unique circuit design, the op amp is distinguished by high stability of the parameters throughout the entire range of supply voltages of ± 5 ... ± 16 volts. This op amp is designed in a three stage configuration. To increase the input impedance, the first differential stage uses a Darlington configuration (transistors VT8, VT10, VT20 and VT19). To extend the gain bandwidth, resistors R7 and R13 are inserted in the emitters of its amplifying transistors. The input stage is powered from the stable current generator (transistor VT13). The current from transistor VT13 is fed to a special distribution circuit, which is designed around transistor VT17, dual emitter transistor VT12 and resistorsR8-R10. Transistor VT12 is inverted and provides "make-up" current for the emitters of the input transistors.

This distribution circuitry provides for little change in the input stage currents throughout the entire temperature range. The circuit for protecting the input stage against a high in-phase voltage is designed around transistors VT14 and VT16, while transistors VT1, VT2, VT4 and VT5 protect the input stage against differential signal overloading. Transistors VT11 and VT18 play the part of an active load on the input stage. Transistor VT15 (used as a diode) limits the level of the collector-base voltage of these transistors.

The second stage of the amplifier is also designed in a differential circuit configuration (p-n-p transistors VT21 and VT24). Transistors VT22 and VT25 serve as active loads for the second stage. The direct current mode of the stage is set by biasing transistors VT21 and VT22 with the regulated collector voltage of the input stage. The third amplification stage uses transistors VT27, VT34 and VT30, VT31, the load for which is the stable cu-rent generator using transistor VT29, the current in which is stabilized by the voltage drop across the diode formed by the connection of the second collector of the transistor to its base. The output stage is designed around the dual emitter n-p-n transistor VT38 and the p-n-p transistor VT39. The second emitter of transistor VT38 serves to control the output p-n-p transistor.

Such a circuit increases the speed of the p-n-p output transistor, Transistors VT32, VT33 and VT38 protect the output stage of the op amp against overload when the output is short-circuited. Transistor VT33 protects the circuitry of the operational amplifier against flip-flop operations, and at the instant of overloading, shunts transistor VT39.

There are three capacitors in the op amp circiutry to improve the transmission of high frequencies. Capacitor C1, which shunts one half of the differential input stage for high frequencies thereby converts its differential output to a single ended output. Furthermore, the high frequency signal bypasses the second differential stage which is designed around low speed p-n-p transistors through capacitor C2.

The high frequency signal component is fed from the output of the first stage directly to the base of the third stage transistor. Capacitor C3 (6 pFd) serves to transmit a certain percentage of the high frequency components of the signal from the output of the first stage to the input of the final (output) stage.

High speed amplifiers are less stable than low frequency op amps, and for this reason, to prevent oscillation in the circuitry, it is necessary to have parasitic capacitance between the op amp output and its inverting input. To reduce the indicated parasitic capacitance, special external equalization circuits are employed (Figures 4.11b and c), the composition of which depends on the task which the operational amplifier performs. The balancing of the amplifier is accomplished by inserting a variable resistor between leads 1 and 5.

4.2.6. Micropower Operational Amplifiers

Operational amplifiers are needed for applications in economical equipment, which operates especially in a standby mode (frequently with battery power), which consume little power from the power supplies. The 153UD4 op amp (Figure 4.12a) has a current consumption of 0.8 ma for power supply voltages of $U_{i.p.}$ [V_{cc}] = ± 6 volts.

The gain of the op amp in this mode is higher than 5,000. This op amp is desinged in a two stage circuit configuration. The first simple differential stage (transistors VT1 and VT5) drives an active load (transistors VT2 and VT4) and is powered from a stable current generator, which is transistor VT3. The second stage is designed as a common emitter-common collector circuit (transistors VT18 and VT15). The collector circuits of transistors VT12 and VT14 serve as the loads on the second stage. The output stage is designed around n-p-n transistor VT19 and the composite [2, 5] p-n-p transistor VT17 and VT20. The operating point of the output transistors is biased by transistors VT13 and VT16.

Resistors R10 and R11 serve to protect the op against output short circuits. The direct current operating mode of the first and second stages of the op amp is assured in the case of wide variations in the supply voltages by a regulator circuit designed around transistors VT6-VT10. Two frequency equalization networks are needed for complete correction of the amplitude-frequency response of this operational amplifier (Figure 4.12b).

The 140UD12 operational amplifier is available at the present time (Figure 4.13). This type of op amp can be used as the micropower amplifier and as a general purpose operational amplifier. The amplifier is designed for operation in a wide range of supply voltages of ± 1.2 volts to ± 18 volts and is designed in a two stage circuit configuration. The amplitude-frequency response is equalized with a single

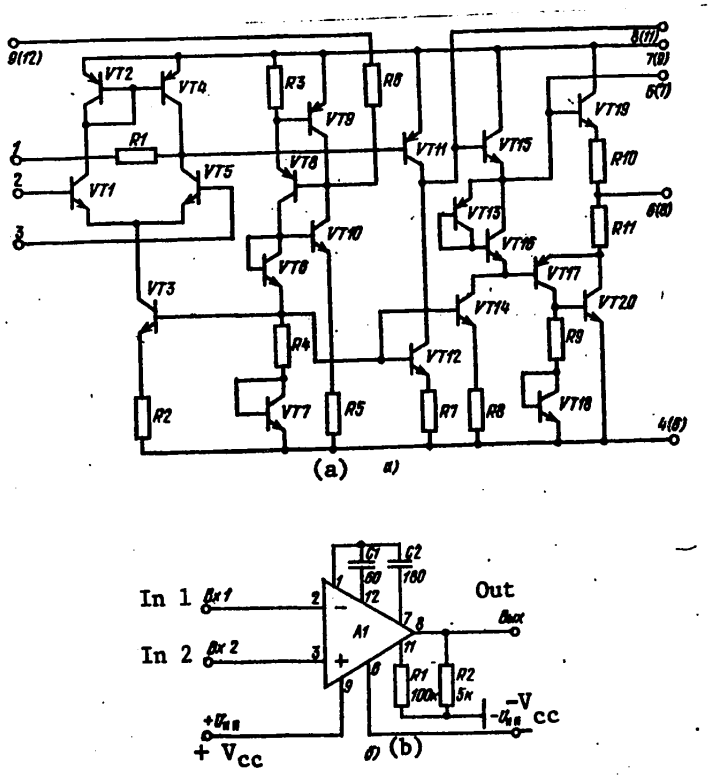


Figure 4.12. The 153UD4 operational amplifier.

a. Basic electrical schematic (the numbering of the pins of the 153UD4 op amp is given in parentheses and the numbers outside the parentheses apply to the 710UD1 unencapsulated; ;

b. The frequency equalization circuit.

internal capacitor. Protection of the output stage against overloads is provided as well as protection against flip-flop operation. The major difference between this amplifier and other types of op amps is the fact that the operating mode of the internal stabilizer-regulator, which determines the entire DC operation of the op amp, is specified from the outside.

By setting the bias current of the stabilizer-regulator, one can vary the op amp parameters from micropower levels up to parameters characteristic of general purpose operational amplifiers.

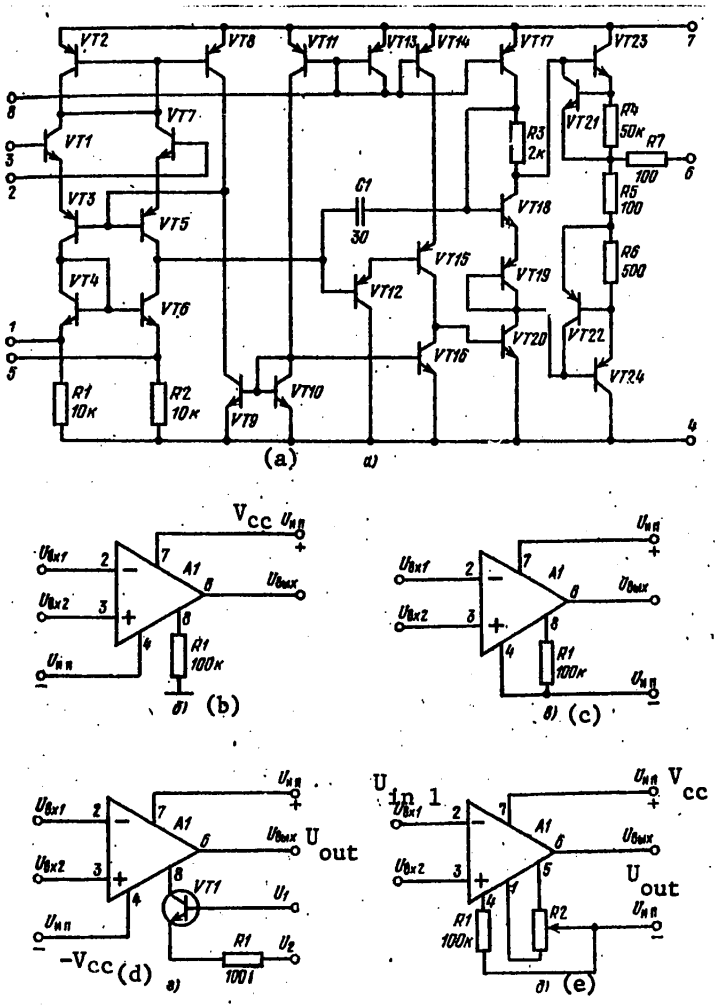


Figure 4.13. Basic electrical schematic (a) and the circuits for supplying bias current to the 140UD12 operational amplifier (b-e).

Circuits which illustrate the methods of setting the current of the stabilizer-regulator are shown in Figure 4.13c-e. The parameters of the op amp for various bias currents are given in Table 4.3.

TABLE 4.3 Electrical Parameters of the 140UD12 Operational Amplifier

Parameter	$V^{\pm}_{pwr}$ = ±3 V I_{bias} = 1.5 μA	$V^{\pm}_{pwr}$ = ±3 V I_{bias} = 1.5 μA	$V^{\pm}_{pwr}$ = 15 V I_{bias} = 1.5 μA	$V^{\pm}_{pwr}$ = 15 V I_{bias} = 15 μA
Zero bias voltage, U_{sm} [$V_{0\ bias}$], mV	5.0	5.0	5.0	5.0
Bias voltage drift, $\Delta U_{sm}/\Delta T$, μV/°C	3	-	-	-
Input currents, I_{in}, nA	7.5	750	7.5	50
Input current difference, ΔI_{in}, nA	3	15	3	15
Drift in the input current difference, $\Delta\Delta I_{in}/\Delta T$, nA/°C	-	-	-	-
Voltage gain, K_U	50	50	200	100
Common mode rejection ratio, $K_{os\ sf}$, dB	70	70	70	70
Output voltage slew rate, $v_{U\ out}$, V/μsec	0.03	0.035	0.1	0.8
Settling time, t_{set}, μsec	3	0.6	1.6	0.35
Input resistance, R_{in}, MOhms	50	5	50	5
Output resistance, R_{out}, ohms	$5 \cdot 10^3$	$1 \cdot 10^3$	$5 \cdot 10^3$	$1 \cdot 10^3$
Maximum output curent, I_{out}, mA	2.9	5	2	10
Maximum output voltage, $U^{\pm}_{out}$, volts	2	2.1	10	10
Maximum input voltage, $U^{\pm}_{in}$ volts	1	1	10	10
Maximum in-phase input voltage, $U^{\pm}_{in\ ph}$, volts	1.2	1.2	12	12
Current consumption, I_{con}μA	25	125	30	170

The presence of internal frequency equalization, the absence of flip-flop operation, the flipping of the inputs as well as protection against output short-circuits permits the wide utilization of this operational amplifier in various circuit configurations.

4.3. Integrated Circuit Comparators

The necessity arises in a number of cases of converting analog signals to digital form. For this, among others, special devices called comparators are used, which are specialized operational amplifiers with a differential input and a single or paraphase digital output [7, 8]. The input stage of a comparator is designed on analogy with op amp circuits and operates in a linear mode. A "1" signal is generated at the comparator output if the difference between the input signals is less than the comparator actuation voltage, or a "0" signal is generated if the difference between the input signals exceeds the comparator actuation voltage. The signal being studied is fed to one input of the comparator while a reference voltage is applied to the other.

A comparator may be used as a threshold gate in automation circuits to quantize a signal in high speed analog to digital converters. It can be used in self-excited oscillators, in pulse amplitude discriminators and peak detectors, as well as a read amplifier for magnetic and semiconductor memory signals. The major parameters of a comparator are: the sensitivity (the precision with which the comparator can differentiate the input and reference signals), speed (reponse, determined by the actuation delay and signal rise time), fan-out load capacity (load (capability of the comparator of controlling a certain number of digital IC inputs).

We shall consider the circuits of the most widespread integrated circuit comparators, the parameters of which are given in Table 4.4 [9, 10].

A comparator based on the 521SA2 integrated circuit (Figure 4.14) has two differential amplifier circuits, an output emitter follower, zener diode level shift circuits and a circuit for limiting the output signal amplitude. The differential input stage (transistors VT1 and VT4) have the usual low zero bias voltage for integrated circuit op amps. The emitters of transistors VT1 and VT4 are powered from a stable current generator (transistor VT5), because of which the collector currents of the first stage transistors are almost independent of an in-phase input signal.

The second differential stage (transistors VT3 and VT6) have as their basis a balanced bias supply circuit. In the balanced state, the voltage of the single output of this stage does not change with fluctuations in the positive supply voltage. The base potential of transistor VT2 is thereby clamped (with an increase in the positive supply voltage, the collector currents of transistors VT6 and VT3 also increase, with the collector voltage of transistor VT3 remaining constant).

To increase the current fan-out load capability, transistor VT6 is equipped with an emitter follower (transistor VT8). The integrated circuit zener diode VD1, which is inserted in the emitter circuits of the second stage transistors, has a reference voltage of +6.2 volts, which clamps the potentials without transistors VT3 and VT6 at a level of about +6.9 volts. Consequently, the permissible signal for the comparator inputs can approach 7 volts.

Zener diode VD2, which is inserted in the output emitter follower circuit, shifts the output signal level "downward" by 6.2 volts, so as to make it compatible with

the input signals for digital TTL integrated circuits. Transistor VT9 isolates the output circuit from the bias circuit of the output stage current generator (transistor VT5) with a compensating diode (transistor VT10 is used as a diode). Transistor VT7 (used as a diode) limits the peak-to-peak value of the output signal on the positive side: for signal levels at the output greater than +4 volts, transistor VT7 turns on and shorts the differential output of the second stage. Because of the limiting of the amplitude, the speed of the comparator is increased significantly.

TABLE 4.4 Parameters of Integrated Circuit Comparators

Parameter	Type of Comparator and Parameter Normal Value		
	525SA1	521SA2	521SA3*
Current consumption, I_{con}, mA:			
From a positive power supply	13.5	10	6.0
From a negative power supply	6.5	8.9	5.0
Zero bias voltage, U_{sm}, mV	3.5	5.0	3.0
Common mode rejection ratio, CMRR, dB	70	70	-
Average input current, I_{in}, μA	75	75	0.1
Input current difference, ΔI_{in}, μA	10	10	0.01
Voltage gain K_U	$75 \cdot 10^3$	$75 \cdot 10^3$	$200 \cdot 10^3$
The "1" voltage, volts	2.5 to 6.0	2.4 to 4.0	-
The "0" voltage volts	-1.0 to 0	-1.0 to 0	-
The "0" output current, mA	0.5	1.6	-
The turn-on delay time, t_{del}, nsec	135	160	200
Input voltage, gating, $U_{in, gate}$, volts	-1.0 to 0	-	-
Gating current, I_{gate} mA	2.5	-	-

*Operating with a single +5 volt power supply

The 521SA2 comparator is simple to use, but does not have any gating inputs. In a dual differential comparator circuit with the 521SA1 (Figure 4.15a), the outputs of two individual comparators are combined using emitter followers with OR logic. One common level shift diode and bias divider is used for both comparators. The application of the dual channel design makes it possible to realize a higher level of integration, as well as improve the electrical parameters of equipment,

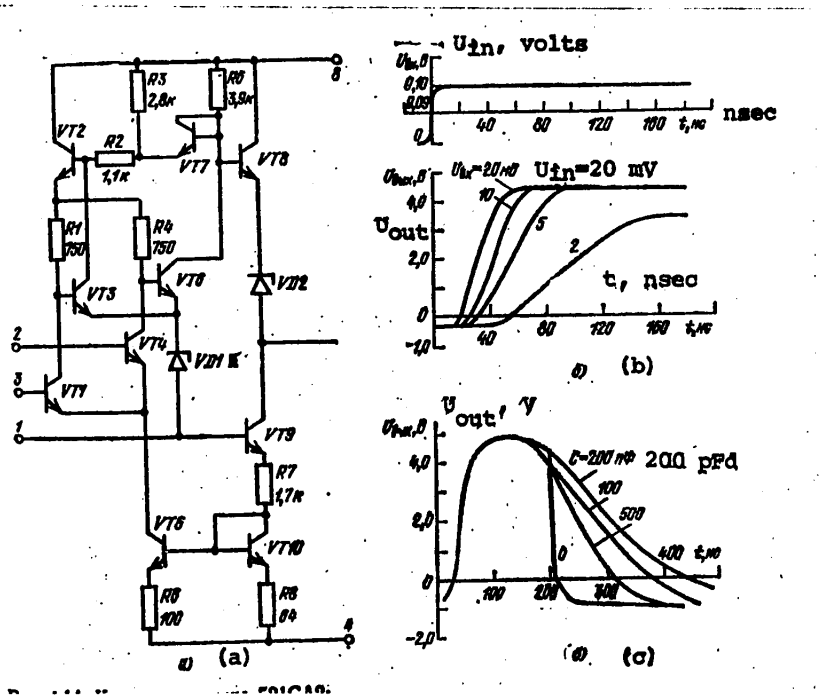


Figure 4.14. The 521SA2 comparator.

a. Basic electrical schematic;
b,c. The rise time U_{out} as a function of the input voltage over-regulation and the load capacitance respectively.

especially devices for reading magnetic memory signals. Because of the identical nature of the parameters of both comparators, it is possible to design dual threshold circuits, having a symmetrical response to postive and negative values exceeding the absolute signal level over the threshold level.

Comparators using the 521SA1 integrated circuit, in contrast to the 521SA2 device, have two gating inputs, as well as a parallel circuit configuration for the limiting networks for the output stage saturation level (transistor VT2 is added in the second stage to reduce the peak to peak value of the signal at the base of transistor VT7 when it is saturated).

A dual comparator performs almost the same electrical function as two of the above mentioned single comparators, however, the power consumption of this IC is only 50% greater. The basic circuit configuration for a type 521SA1 comparator is shown in Figure 4.15b. The reference voltage is fed to one of the inputs, while the input signal is fed to the other. In the case where the input signal exceeds the

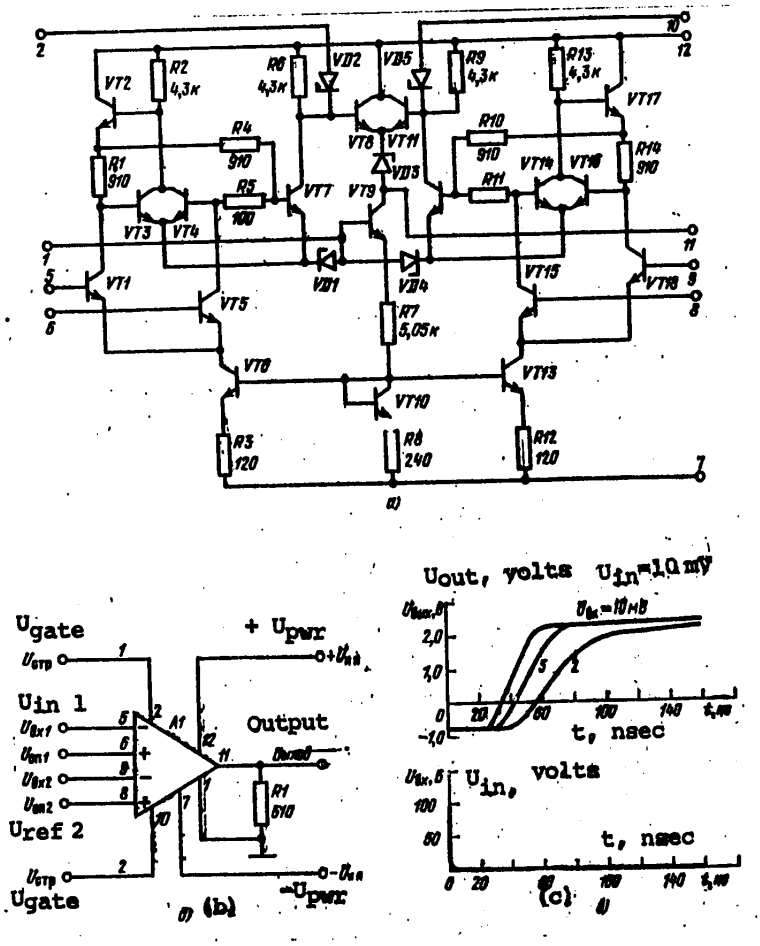


Figure 4.15. The 521SA1 dual comparator.

a. Basic electrical schematic;
b. External circuit configuration;
c. Output voltage rise times as a function of the input signal overregulation voltage levels.

reference voltage, the output voltage switches to the positive or negative state (Figure 4.15c).

The comparator configuration considered here can be used as a voltage comparator in analog-code converters, where one input is controlled by the analog signal and the other is controlled by a reference signal fed from a step resistive matrix. The circuit can also be used for a film or disk magnetic memory as read amplifier.

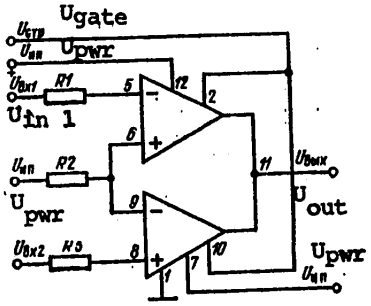


Figure 4.16. A threshold gate designed around the 521SA1 dual comparator.

Threshold gates which are indicators of an output voltage relative to present precise limits form a special group of circuits for comparator applications (Figure 4.16).

4.4. Integrated Circuit Analog Multipliers

Analog integrated circuit multipliers (IAP) are designed to perform the operation of multiplying two analog quantities. They can be used in frequency doubler, phase detector, and balanced modulator circuits, as well as in automatic control systems as multipliers and squaring circuits. In conjunction with operational amplifiers, analog IC multipliers can perform division, extract roots and perform trigonometric functions.

The existing types of analog multipliers can be broken down into two groups: balanced modulators intended for operation in a wide frequency bandwidth (40 MHz and more) with small input signal levels (up to 0.5 volts) and analog multipliers themselves, which are intended for operation in a narrow band of frequencies with high level input signals (up to ±10 volts). The electrical parameters of the 526PS1 balanced modulator circuit (Figure 4.17) are given in Table 4.5.

The main assembly of the 526PS1 integrated circuit is a cross coupled quad differential amplifier (transistors VT1, VT4, VT5 and VT8). In terms of its action, it is similar to a common emitter amplifier, but its emitter currents do not depend on the input voltages. It is not difficult to note that the difference between the output currents of the amplifier (being the output quantity) is proportional not only to the input voltage of the amplifier (it is fed to input X, pin 10), but also to the difference between the emitter currents:

$$\Delta I_{out} = f(U_{in}, \Delta I_0).$$

The emitter currents can be regulated by feeding a voltage to the bases of transistors VT2 and VT7 (this voltage is fed to the Y input, pin 11) with pins 2 and 12 shorted together. The transfer function of a balanced modulator is a function of the voltages fed to the X and Y inputs, and has the form [11]:

$$\Delta I_{out} = \Delta I_{вых} = (I_0/2)\,[\mathrm{th}\,(U_Y/2\varphi_T) \times \mathrm{th}\,(U_X/2\varphi_T)].$$

If identical load resistors R_H are connected to pins 8 and 9, then the output signal can be obtained in the form of the voltage difference:

$$U_{out} = U_{вых} \approx \Delta I R_н = I_0 R_н/2 [\text{th}(U_Y/2\varphi_T) \text{th}(U_X/2\varphi_T)]. \quad (4.1)$$

An internal regulator (diodes VD1 ... VD5 and resistor R9) provide for stable DC operation of the circuit and set the bais for transistors VT3 and VT6, maintaining the emitter current constant for the quad amplifier. One can conclude from formula (4.1) that the output voltage is a nonlinear function of the input potentials, however, at small values of the input voltages, the circuit operates as a linear signal multiplier, having the following transfer function:

$$U_{вых} \approx (I_0 R_н/8\varphi_T^2) U_X U_Y.$$

The linearity condition for each of the inputs can be written in the form:

$$|U_{вх} - \text{th}(U_{вх}/2\varphi_T)|/U_{вх} < \delta$$

where δ is the permissible nonlinearity of the amplitude response of the multiplier.

The value of the hyperbolic tangent can be represented in the form of a series [12]:

$$\text{th}\frac{U_{вх}}{2\varphi_T} = \frac{U_{вх}}{2\varphi_T} - \frac{1}{3}\left(\frac{U_{вх}}{2\varphi_T}\right)^3 + \frac{2}{15}\left(\frac{U_{вх}}{2\varphi_T}\right)^5 \ldots.$$

The values of the input voltages are given in Table 4.6 as a function of the coefficient δ and the temperature.

The linear range for the Y input can be expanded if a resistor R_Y is inserted between pins 2 and 12. Then the input current difference will be determined by the equation:

$$\Delta I = U_Y/(2r_э + R_Y). \quad (4.2)$$

where r_e is the resistance of the emitter-base junction.

If $R_Y >> (r_e = \phi_T/I_e)$, then the value of r_e may be disregarded; then formula (4.2) is simplified:

$$\Delta I = 2U_Y/R_Y, \quad (4.3)$$

and expression (4.1) will have the form:

$$U_{out} = U_{вых} = (U_Y R_н / R_Y)[\text{th}(U_X/2\varphi_T)].$$

But in this case, the linear input voltage will be limited by the direct current mode (which is set by the internal regulator) to a level of approximately 0.5 volts.

A schematic for the use of the 526PS1 integrated circuit as a dual balanced mixer is shown in Figure 4.18. Since a dual balanced mixer usually operates with a low input signal level (input Y) and a high reference signal level (input X), its transfer function can be written in the form:

$$U_{out} = U_{вых} = (I_0 R_н U_Y / 4\varphi_T)[\text{th}(U_X/2\varphi_T)],$$

where $U_Y \leq \phi_T$.

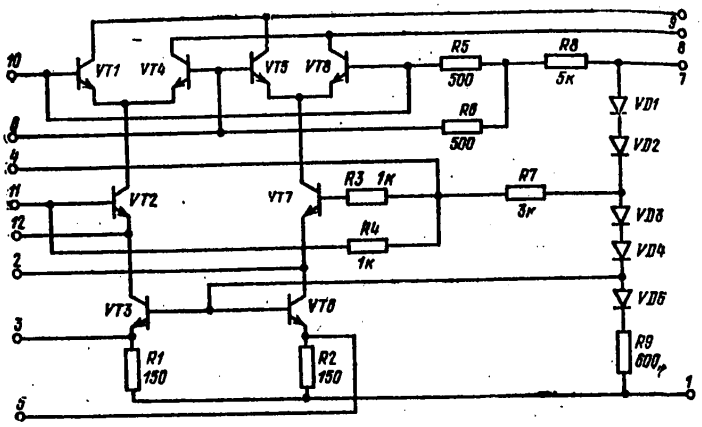


Figure 4.17. Basic electrical schematic of the 526PS1 balanced modulator.

In the case of harmonic input (input Y) and heterodyne (input X) signals, the harmonics $n\omega_0 \pm m\omega_1$ are present in the spectrum of the output signal of an ideal twin balanced mixer. Limiting ourselves to the difference frequency output voltage $(\omega_0 - \omega_1)$, we can write the transfer function of a dual balanced mixer as:

$$U_{вых\ р} = (I_0 R_н U_Y) B / 8\varphi_T. \qquad (4.4)$$

TABLE 4.5 Parameters of Integrated Circuit Multipliers

Parameter	140MA1	526PS1	525PS1
Input control signal suppression factor, $K_{in\ con}$, dB	46	8	46
Reference signal suppression factor, $K_{in\ ref}$, dB	46	65	46
The dynamic control signal voltage range, D, dB	16	-	-
Control signal gain, K_U	2.9	-	-
Upper cutoff frequency, f_{up}, MHz	2	40	1
Input impedance, R_{in}, MOhms	-	0.050	20
Output impedance, R_{out}, ohms	-	-	30
Converter transconductance, S, A/V	-	5	-
Multiplication linearity, percent	-	-	1
Supply voltage, U_{pwr}, V	±12	+6	±15
Permissible input voltage, U_{in}, volts	±5	-	±10
Power dissipation, P_{dis}, mW	250	36	170

TABLE 4.6 Range of Permissible Input Voltages

δ, %	(1) $\frac{U_{вх}}{\varphi_T}$	(2) Значения $U_{вх}$ при различной температуре, °С			
		−60	+25	+60	+125
1	0,34	6,1	8,7	9,8	11,7
5	0,8	14,1	20,6	23	27,5
10	1,16	21	30	33,3	40
15	1,48	26,7	38	42,5	51
20	1,78	32	45,6	51	60

Key: 1. $U_{in}/\phi T$;
2. Values of U_{in} for various temperatures, °C.

where B is the dependence on the reference signal level (the calibration ratio). One may assume for a low level reference signal that $B \approx (U_0/2\phi_T)U_0 = U_X$, and therefore formula (4.4) has the form:

$$U_{вых\ р} = (I_0 R_н/16\varphi_T^2) U_X U_Y.$$

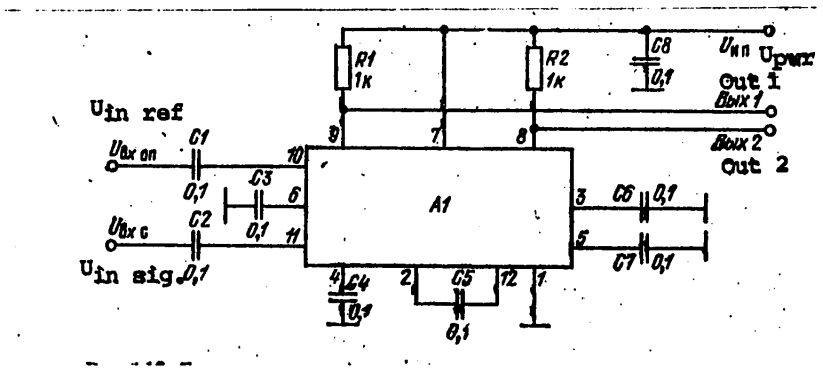


Figure 4.18. Circuit configuration of the 526PS1 integrated circuit used as a dual balanced mixer.

With an increase in the voltage at the reference input, the function becomes nonlinear (Figure 4.19a). The conversion gain, which is defined as the ratio of the intermediate frequency input [sic] voltage to the signal input voltage (Figure 4.19b) is measured in decibels:

$$K_{IF} = 20 \log(U_{out\ r}/U_{in\ s}). = \overline{K_{пр} = 20 \lg (U_{вых\ р}/U_{вх\ с})}.$$

In the 140MA1 balanced modulator (Figure 420a), the main multiplication circuitry is designed around transistors VT6, VT9, VT11 and VT14. The differential amplifier (transistors VT5, VT8 and VT12, VT15) controls the multiplier emitter currents.

The multiplier emitter current difference is made to be a linear function of the input voltage at the Y input by inserting resistor Ry between the emitters of the differential amplifier (pins 4 and 10). The current levels in the emitters of the quad of amplifier transistors (VT6, VT9, VT11 and VT14 is regulated by the voltage at the Y input, and since the level of the currents flowing through the stable current generators (transistors VT7 and VT13) is stable, the difference in these currents is determined using formula (4.3). The linear input voltage range of up to +5 volts is achieved by virtue of the high supply voltage of ±12 volts. A Darlington circuit (transistors VT5, VT8, VT12 and VT15) is used to increase the Y input impedance. To increase the X input impedance, a differential stage is inserted in the modulator circuit, where this stage is designed as a common emitter configuration. This stage controls the bases of the multiplier. Working from the fact that the Y input is linear, while the input differential amplifier has the gain of [1], the transfer function of the modulator can be written in the form:

$$\overline{U_{вых} = (2R_н/R_Y)\, U_Y \operatorname{th} (U_X/2\varphi_T)},$$

(4.5)

where $U_Y \leq \pm 5$ volts. The level of the emitter currents is clamped by the stable current generators (transistors VT2, VT4, VT7 and VT13). Bias is fed to the bases of the transistors of these stable current generators from transistor VT10 (used as a diode).

If pins 2 and 12 are joined together and they are grounded through normalizing resistor R, then the current level through the bias diode can be determined from the formula:

$$I_d = (U_{pwr} - U_{eb})/(600 + R),$$

where I_d is the diode current (transistor VT10), U_{pwr} is the negative supply voltage, U_{eb} is the voltage drop across the base-emitter junction and R is the value of the resistor which determines the current level while 600 ohms is the approximate value of the internal resistance of the diode.

In order that a high input voltage can be applied to the Y input and conversion linearity assured in this case, the voltage at the collectors of the differential amplifier transistors should be no less than the input signal voltage. The normal operating mode of the modulator is achieved by feeding the requisite bias to the bases of transistors VT1 and VT3 (the X input) through a voltage divider from the positive power supply. The modulator can operate both from balanced and unbalanced power supplies; in this case, it is necessary to observe the matching of the modulator at the inputs and output.

In the circuit configuration where the 140MA1 integrated circuit is used as a balanced modulator operating from power supplies at ± 12 volts (Figure 4.20b), the direct current mode is set by a divider (the nominal values of the resistors are 3.6 to 2.4 KOhms). The current level I_0 is set by means of a resistor with a nominal value of 11 KOhms, insered betweens 2 and 12 to ground. The X and Y inputs are decoupled by means of capacitors. To prevent self-excitation, series resistors with nominal values of 51 ohms are inserted in the circuits of leads 5 and 9. The voltage traces at the inputs and outputs in the balanced modulator circuit are shown in Figure 4.20c.

An example of a phase detector constructed with the 140MA1 integrated circuit is shown in Figure 4.21. The operation of the linear phase detector (Figure 4.21) is based on the following trigonometric equation:

$$[\cos\omega\tau \cos(\omega\tau + \varphi)] = (K_1/2)\cos(2\omega\tau + \varphi) + (K_2/2)\cos\varphi$$

By using a low pass filter, one can segregate the desired component, which is proportional to $\cos\phi$. The modulator in this circuit serves as a harmonic function multiplier.

The 525PS1 analog multiplier (AP) (Figure 4.22) operates at lower frequencies than the 140MA1 modulator. It is designed for the multiplication of input voltages with a linearity of no worse than 3% (the level at both inputs is up to ± 10 volts).

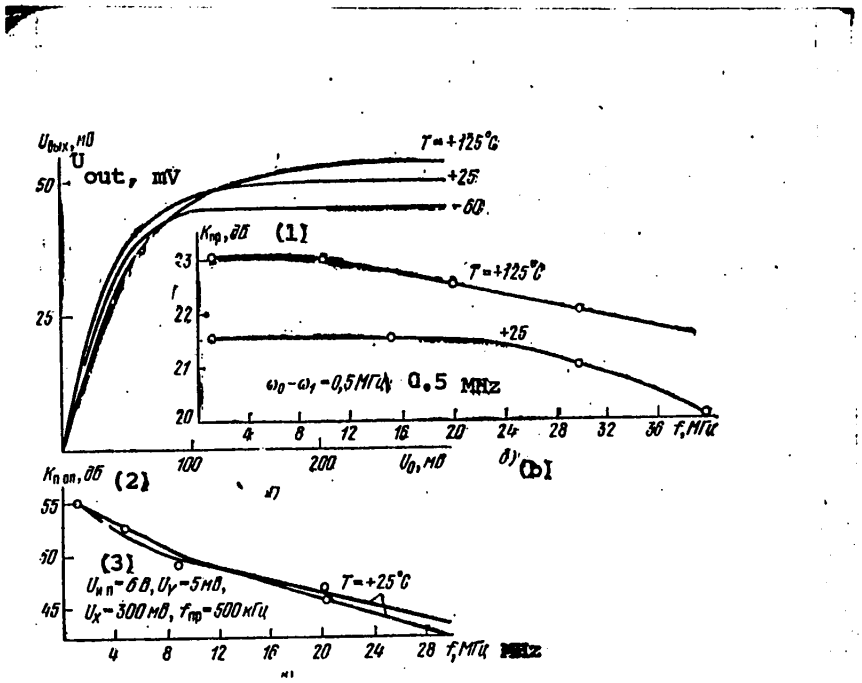


Figure 4.19. The intermediate frequency output voltage ($\omega_0 - \omega_1$) as a function of the reference signal voltage (a) and as a function of the conversion gain frequency (b) and reference signal voltage suppression (c).

Key: 1. K_{pr} [conversion voltage gain], dB;
2. $K_{p\ op}$ [$K_{in\ ref}$ = reference signal suppression factor], dB;
3. Supply voltage of 6 volts, U_Y = 5 mV, U_X = 300 mV and f_{IF} = 500 KHz.

The analog multiplier consists of two differential amplifiers, which control the operation of the main multiplication circuit (transistors VT8, VT11, VT13 and VT15).

The differential amplifier (transistors VT7, VT9 and VT16, VT14) sets the difference in the emitter currents of the two pairs of transistors of the multiplier circuit proportional to the differential input signal. As follows from (4.5), an exponential component is present in the output voltage of the modulators which is due to the nonlinear dependence of the emitter currents of the multiplier on the voltage at the X input. This component does not permit obtaining good linearity at the circuit output. In order to obtain a linear dependence of the output voltage with a high X input voltage level, it is necessary to take the logarithm of the X input signal beforehand. For this, a differential logarithmic stage is inserted in the multiplier circuitry. The differential stage (transistors VT1, VT2 and VT6, VT5) converts the input voltage to the currents $I_0 + I_X$ and $I_0 - I_X$

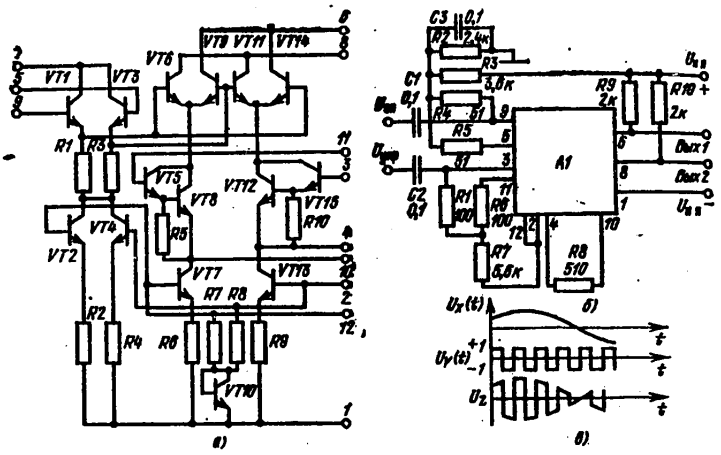


Figure 4.20. The 140MA1 balance modulator.

a. Basic electrical schematic;
b. Circuit configuration;
c. Voltage traces at the modulator inputs and outputs.

by means of resistor R_X, which is inserted between pins 5 and 6. Since the current I_0 is determined by the stable current generators (transistors VT3 and VT4), the level of the current I_X can be calculated from the following equation [13, 14]:

$$I_X = U_X/(2r_e + R_X) = \overline{I_X = U_X/(2r_э + R_X)}.$$

The currents $(I_0 + I_X)$ and $(I_0 - I_X)$, in flowing through diodes VD1 and VD2, produce a voltage drop across them, the difference in which is the output voltage of the differential stage, and has the form:

$$U_{out} = U_{d1} - U_{d2} = \phi_T \ln[(I_0 + I_Y)/(I_0 - I_X)].$$
$$\overline{U_{вых} = U_{д1} - U_{д2} = \varphi_T \ln[(I_0 + I_Y)/(I_0 - I_X)]}.$$

The overall transfer function of the multiplier is described by the formulas:

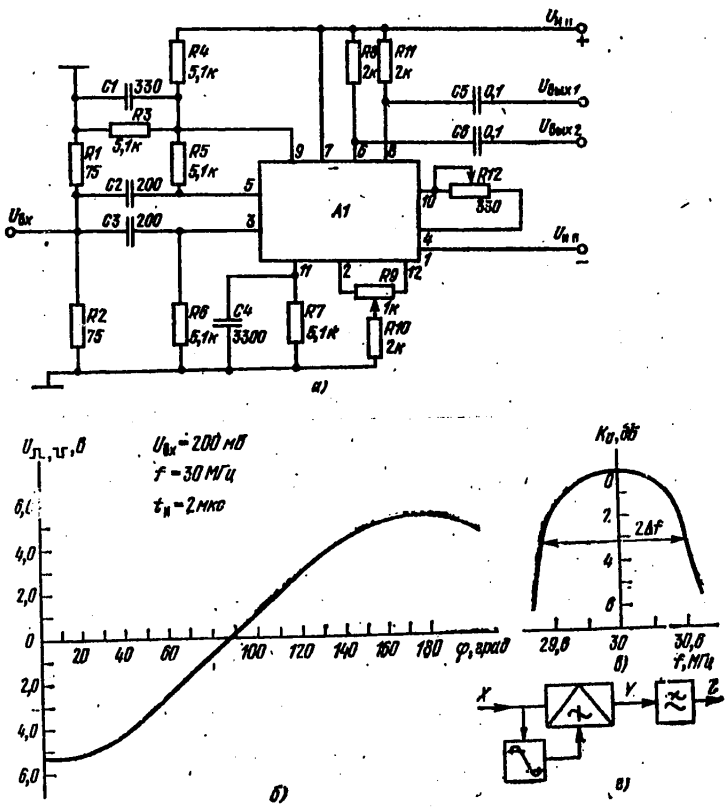


Figure 4.21. A phase detectr based on the 140MA1 integrated circuit.

a. Design example; b, c. Amplitude-phase and frequency response characteristics respectively; d. Block diagram.

$$U_{out} = U_{вых} \approx |2R_н/(I_0 R_X R_Y)| U_Y U_X$$

or $U_{out} = KU_X U_Y$,

where $K = 2R_{load}/(I_0 R_X R_Y)$. $K = 2R_н/(I_0 R_X R_Y)$.

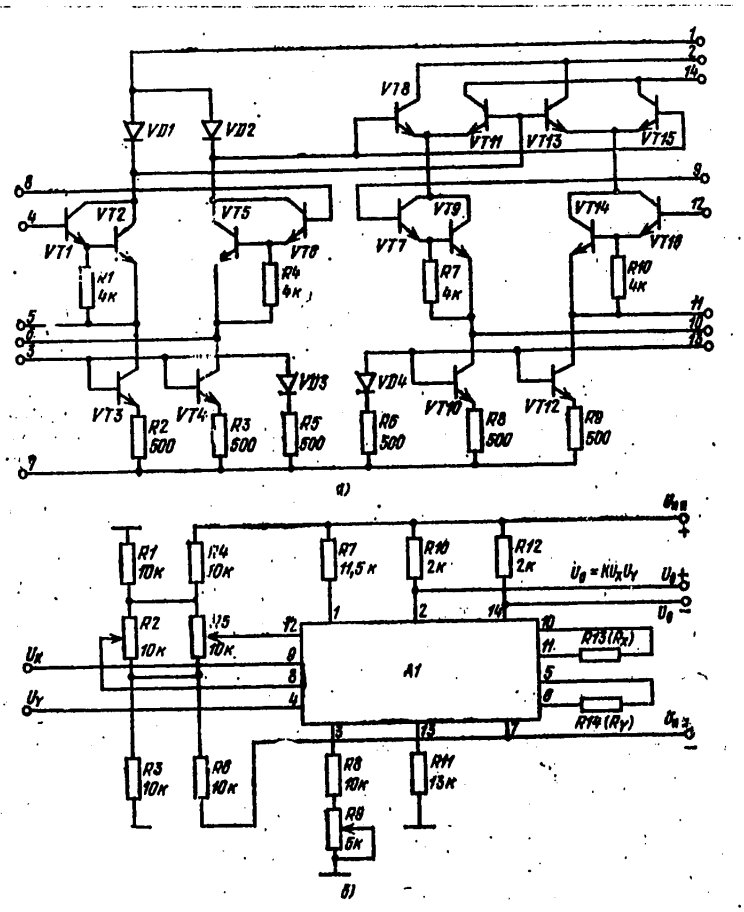


Figure 4.22. Basic schematic of the 525PS1 analog multiplier (a) and the basic circuit configuration of the 525PS1 IC (b).

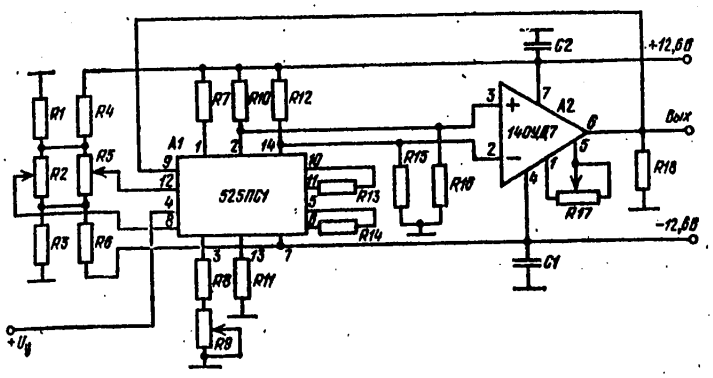


Figure 4.23. Schematic of a level shifting analog multiplier using a 140UD7 op amp powered by a ±15 volt power supply.

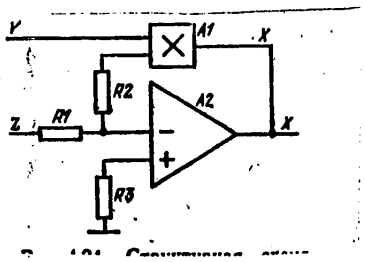


Figure 4.24. Block diagram of a X = Z/y. voltage divider.

The current level I_0, on the level of which the entire DC operation of the circuit depends, is normalized by means of resistors inserted between pins 3 and 13 to ground. In this case, the current flowing through diodes VD1 and VD2 can be determined from the expression:

$$I_d = I_0 = (U_{pwr}^{-} - U_d)/500 + R \qquad (4.6)$$

where R is the nominal value of the resistors in ohms.

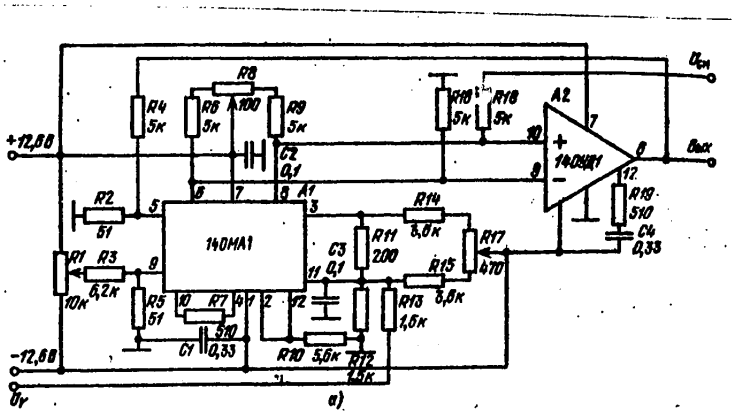
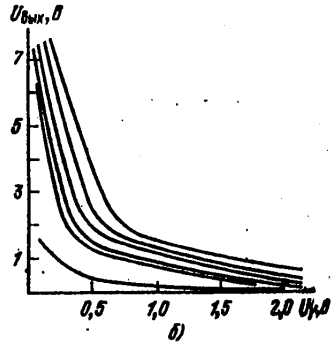


Figure 4.25. Schematic of a voltage divider based on the 140MA1 integrated circuit (a) and its transfer functions (b).



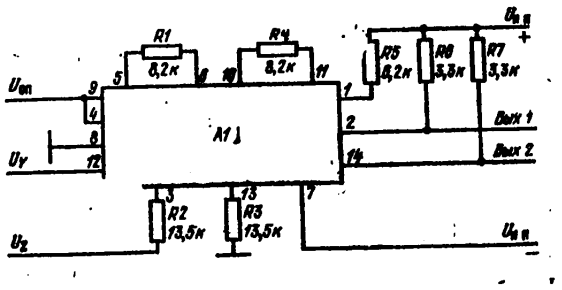


Figure 4.26. Simultaneous multiplication and division circuit based on the 525PS1 integrated circuit.

The configuration of the 525PS1 integrated circuit as an analog multiplier (Figure 4.22b) makes four quadrant multiplication possible for input analog signals having a level of up to ±10 volts with an amplitude of the output signal of ±10 volts. Thus, the scaling factor of the circuit is 0.1. In order to obtain a greater output voltage amplitude, the circuit should operate from a positive supply of +32 volts. In this case, the output voltage of the multiplier circuit in the no-signal mode is 21 volts. In order to bring this voltage to the zero level, it is necessary to add a bias circuit.

In the analog multiplier which is equipped with a level bias circuit, designed around the 140UD7 op amp (Figure 4.23), in order to match the DC level at the multiplier output to the permissible input voltages of the op amp, a divider with a division ratio of 1:10 is inserted between them. A level shifting four quadrant multiplier with an output voltage of ±10 volts can also be obtained without using an additional +32 volt power supply. In the circuit shown in Figure 4.23, the multiplier operates from a power supply with voltages of ±15 volts. In this circuit, the scaling factor of the multiplier, K, is reduced by 10 times by virtue of the reduction in the load resistance, while the op amp, in turn, is used as a scaling amplifier with a gain of K = 10.

As was stated above, various functions can be modeled using analog multipliers. We shall a consider a few examples from this area.

A squaring operation can be realized, if a voltage U is fed to the X and Y inputs, which are connected together in the basic circuit configuration. Then the output voltage can be determined from the formula $U_{out} = KU^2$, where $U = U_X = U_Y$ and the scaling factor is:

$$K = 2R_{load}/I_0 R_X R_Y.$$

The division of two signals is accomplished by the circuit depicted in Figure 4.24 in which the multiplier is used as a negative feedback element for an operational amplifier. In this circuit, the op amp will strive to maintain ground potential at its inverting input. Assuming that the input current of the op amp, I_{in}, is close to zero, we find the transfer function of the circuit:

$$K U_X U_Y / R_1 = -U_Z / R_2.$$

From which $U_X = -R_1/(KR_2)(U_Z/U_Y)$. If we choose $R_1 = KR_2$, then $U_X = -(U_Z/U_Y)$.

In the voltage divider designed around the 140MA1 integrated circuit (Figure 4.25), the two analog multiplier inputs are tied together; then the output voltage of the op amp will be equal to:

$$(U_Z/R_2) = (KU_X^2/R_1), \text{ откуда } U_X = -\sqrt{(R_1 U_Z)/(R_2 K)}.$$

Consequently, this circuit generates the square root function of the input signal. In all of the circuits treated above, the analog multiplier is used with a level shift circuit.

It is possible to construct a frequency doubler based on an analog multiplier. For this, it is necessary to connect a high pass filter to the output of the analog multiplier. The operational principle of such a circuit is based on the trigonometric identity:

$$(\cos \omega t)^2 = 1/2 (1 + \cos 2\omega t).$$

The high pass filter does not pass parasitic low frequency signals at the output.

We will note that based on an analog converter, it is not difficult to design a device, the output voltage of which is proportional to the ratio of the product of two analog quantities to a third component:

$$U_{out} = K(U_X U_Y)/U_Z,$$

where U_Z is the voltage which regulates the level of the current I_0 [see formula (4.6)]. A circuit for the simultaneous multiplication and division of signals designed around the 252PS1 analog converter is shown in Figure 4.26. The value of I_0 is determined from the expression:

$$I_0 = (U_Z - U^-_{pwr} - U_{eb})/(R_3 + 500).$$

Some applications of analog converters can be based on the fact that there is the capability of varying the resistances R_X and R_Y in a linear fashion.

4.5. Analog Integrated Circuits for Radio Receiving Equipment

The integrated circuit component base is being widely introduce into modern communications equipment. The technological state of the art makes it possible to create a products list of analog IC's, which provide for the construction of practically all of the assemblies of radio receiving equipment. For example, the K242 series of integrated circuits, fabricated using thick film technology, can be used at frequencies of up 110 MHz. They are used to construct the channels of color television sets [15, 16] as well as other radio receiving equipment. The 235 series integrated circuits are designed for operation at frequencies of up to 200 MHz and have good noise parameters, referenced to the bandwidth ($\overline{U}_n$ = 0.01 ... 0.8 μV). Semiconductor integrated circuits are being widely introduced at the present time.

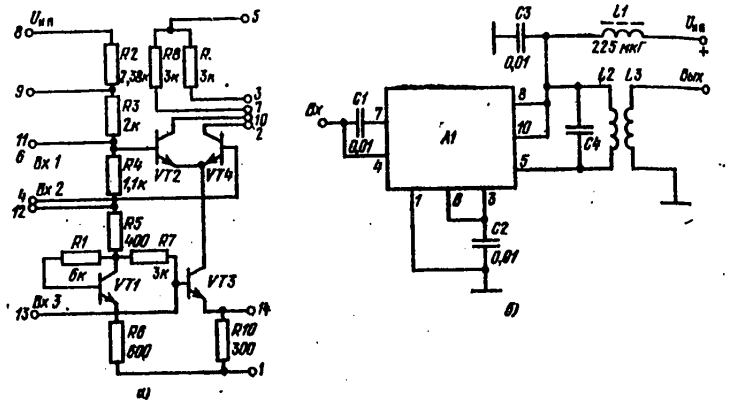


Figure 4.27. The 175UV4 high frequency amplifier.

a. Basic electrical schematic; b. Circuit configuration; C4, L2 and L3 are chosen from the calculation of the requisite frequency.

4.5.1. The Differential Amplifier

Differential amplifiers were developed in the initial stages of semiconductor integrated circuit design. These amplifiers are universal and can be used in all assemblies of receiving and amplifying equipment. Only a qualitative improvement in them is underway at the present time: the expansion of the frequency range, the reduction of the noise and power consumption and the increasing of the output power.

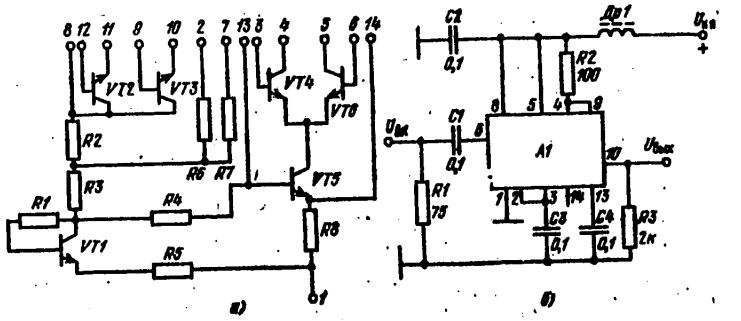


Figure 4.28. The 175UV2 high frequency amplifier.

a. Basic electrical schematic; b. Circuit configuration when used as a video amplifier.

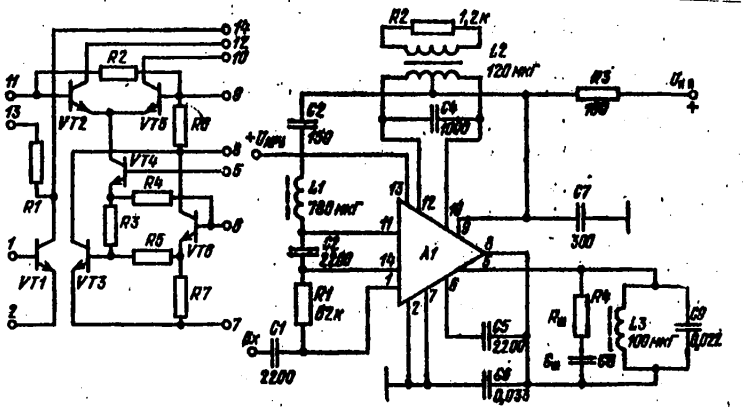


Figure 4.29. The K175US2 high frequency amplifier.

a. Basic electrical schematic; b. Circuit configuration.

The simplest differential circuit with a stable current generator and a bias circuit is widely used in all stages of a receiving and amplifying channel: the RF amplifier, mixers, local oscillators, limiters, variable and fixed gain IF amplifier stages as well as AM and FM detectors. The 175UV4 integrated circuit (Figure 4.27) with a passband of 150 MHz can serve as an example of a differential amplifier.

The direct current mode of the amplifier is set by the bias of transistor VT1 (by means of negative feedback resistors R1). By switching the tap on the divider

(9, 11, 12), one can adjust the level of the collector current for transistor VT3. Transistors VT2 and VT4 form a differential amplifier, which is powered by a stable current from transistor VT3. The considerable noise level (a noise factor of 6 to 8 dB) makes it difficult to use this IC in the input stages of receiving equipment.

The 175UV2 amplifier circuit (Figure 4.28) incorporates two additional transistors for the construction of a local oscillator. The frequency range of the given circuit is limited to 60 MHz and the noise figure to 6 dB.

Yet another example of a differential amplifier is the K157US2 integrated circuit (Figure 4.29). In this variant, the control circuit for the current generator is designed around transistors VT3 and VT6. Resistors R2 and R6 as well as transistor VT3 are intended for specifying the operational mode of transistor VT4. Transistor VT1 serves as a preamplification stage. It can be seen from the

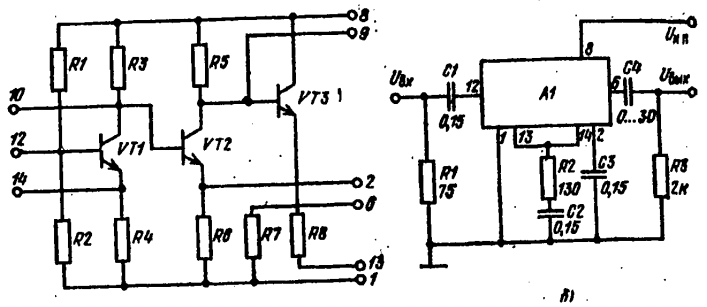


Figure 4.30. The 175UV3 broadband amplifier.

Key: a. Basic electrical schematic;
b. Circuit configuration.

circuit configuration that realized here using one integrated circuit are an RF amplifier, mixer, local oscillator and IF amplifier with AGC. The amplitude modulated signal is fed to the base of transistor VT1, the collector load on which is a tuned circuit: capacitor C3 and inductance coil L1. The gain of this stage can be regulated through the choice of the nominal value of resistor R1. The signal is fed from the collector of transistor VT1 to the base of transistor VT2 of the differential pair (transistors VT2 and VT5), the current in which is regulated by transistor VT4. The generator circuit operates with this transistor, the frequency of which depends on the parameters of the parallel resonant circuit L3, C9.

The 175UV3 amplifier can serve as an example of wide band amplifiers (Figure 4.30).

4.5.2 Low Frequency Amplifiers (UNCh)

The design of high power semiconductor integrated circuit low frequency amplifiers involves the solution of a number of circuit design, structural and production

process problems. First of all, economical output stages must be developed having high power integrated circuit structures, where the stage should introduce little nonlinear distortion into the signal. Secondly, a technology must be developed for producing n-p-n structures with a high permissible current density and an elevated gain on a single chip, as well as injection p-n-p structures with high gains. Further, it is necessary to optimize the fabrication technology for integrated circuits with power output structures, so as to obtain large permissible currents (1 to 2 amps) and low bulk resistance of the collector with a small structure area. And finally, it is necessary to develop an IC structure which assures reliable operation and eliminates self-heating.

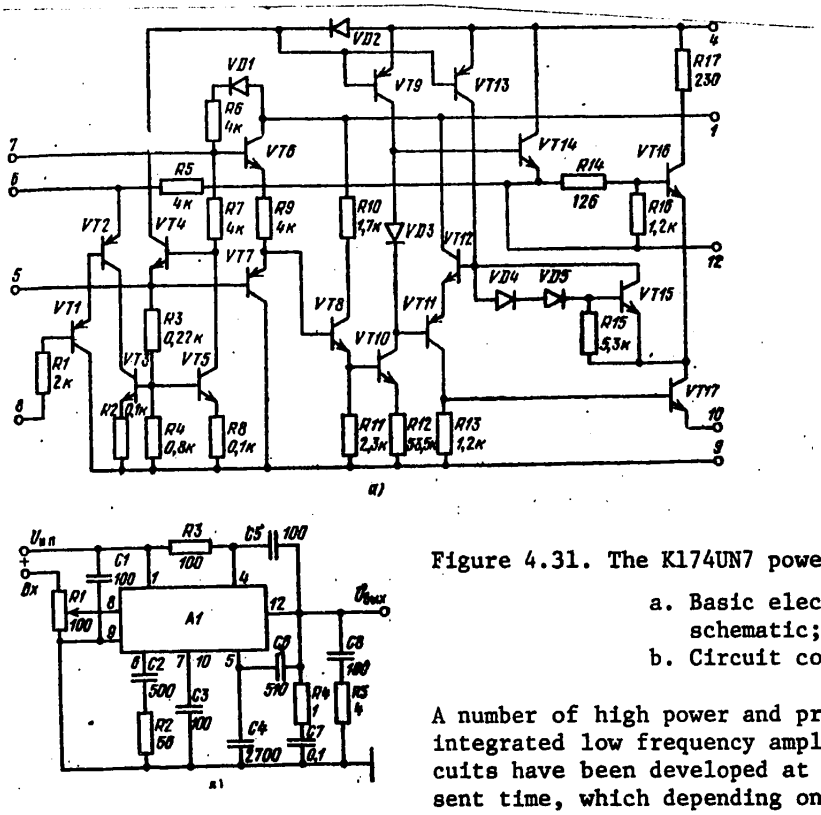


Figure 4.31. The K174UN7 power amplifier.

a. Basic electrical schematic;
b. Circuit configuration.

A number of high power and preamplifier integrated low frequency amplifier circuits have been developed at the present time, which depending on the type of radio receiving equipment, can be used in the following variants: an integrated circuit audio preamplifier plus an output stage using discrete components; an audio preamplifier plus and integrated circuit high power audio amplifier (or a single high power audio amplifier IC) with a sufficient voltage gain.

The K174UN7 low frequency amplifier circuit (Figure 4.31) has an output power of 4.5 watts. The input stage of the amplifier is designed around a composite p-n-p transistor (transistors VT1 and VT2), the load for which is transistor VT3. The preamplifier stage is designed around transistors VT7, VT8 and VT10.

For the purpose of reducing the load on the input stage, transistors VT7 and VT8 are connected in a common collector configuration. The load on transistor VT10 is the current generator made with transistor VT9. The power output stage is designed around transistor VT14, VT16, VT11 and VT17, and delivers an output current of 1 amp. The bias current of the output transistor VT10 is governed by the current flowing through transistor VT9, and the voltage drop which appears across diode VD3. The bias current of the output transistor VT17 is governed by the current of transistor VT13 and the voltage drop produced across the "stack" of p-n junctions (VD4, VD5, and VT15). The circuit for stabilizing the DC operating point of the amplifier uses transistors VT4 and VT5. An external network which equalizes the frequency response at high frequencies is connected to pin 5, while a feedback circuit which serves to adjust the gain is connected to pin 6.

The amplifier delivers an output power of up to 4.5 watts into a load of 4 ohms with a power supply voltage of 15 volts. The IC package has a heat sink radiator. The description of yet another integrated circuit audio amplifier with an output power of 1 watt, the K1US744, is given in [18].

Audio preamplifiers are used as microphone and headphone amplifiers in radio equipment and to amplify weak signals from various transducers. The considerable gain ($K_U \geq 1{,}000$), the low noise and the good linearity are the major characteristics of a preamplifier.

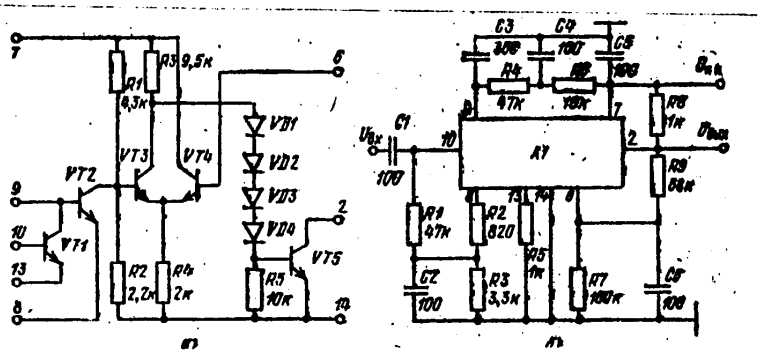


Figure 4.32. The K174UN3 audio preamplifier.

a. Basic electrical schematic;
b. Circuit configuration.

The circuit of the K174UN3 audio preamplifier (Figure 4.32) contains a two stage input amplifier using transistors VT1 and VT2, with external loads and bias circuits, as well as a two stage output amplifier using transistors VT3 and VT5. The circuit makes a provision for incorporating external feedback through transistor VT4. Diodes VD1 ... VD4 serve for matching the DC level of the collector voltage of transistor VT3 and the base potential of the output transistor.

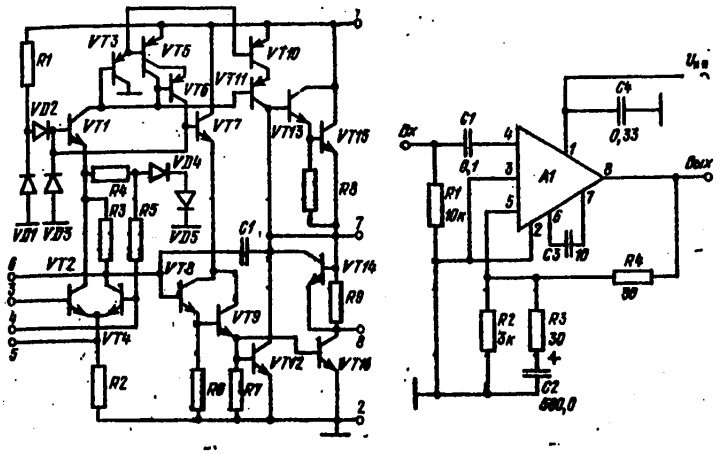


Figure 4.33. The 538UN1 preamplifier.

a. Basic electrical schematic;
b. Circuit configuration.

The amplifier is used with a large number of outboard components, which govern its temperature stability, frequency response and gain. With a resistance in the base circuit of transistor VT1 of R = 1 KOhm, the amplifier noise voltage referenced to the input is U_n = 1.5 μV in passband of 20 KHz.

Improving the noise characteristics of the amplifiers by means of refining the technology and optimizing the choice of the operating modes of the transistors is the basic problem of this direction in general purpose circuits. The 538UN1 amplifier (Figure 4.33) can serve as an example of a preamplifier with improved characteristics.

The two stage amplifier circuit makes it possible to obtain a gain of $K_U \geq 10^5$. The input stage is designed in a differential circuit configuration (transistors VT2 and VT4). The input stage is powered from an emitter follower (transistor VT1). A composite emitter follower (transistors VT8 and VT9) serves to match the input and output stages. The current of this emitter follower is governed by the output potential of transistor VT7. Transistor VT12, the active load on which is transistors VT10 and VT11, inverts the signals fed from the output of the composite emitter follower. The output stage, which is designed around transistors VT13, VT15 and VT16, has good linearity and makes it possible to obtain a harmonic distortion factor of $K_h \leq 0.1\%$. Transistor VT14 serves to protect the output stage against current overloads.

An improvement is achieved in the temperature stability and power supply voltage stability by incorporating a voltage regulator in the circuit which uses reverse biased diodes VD2 and VD3, which also reduce the collector-emitter voltage of the input stage transistors.

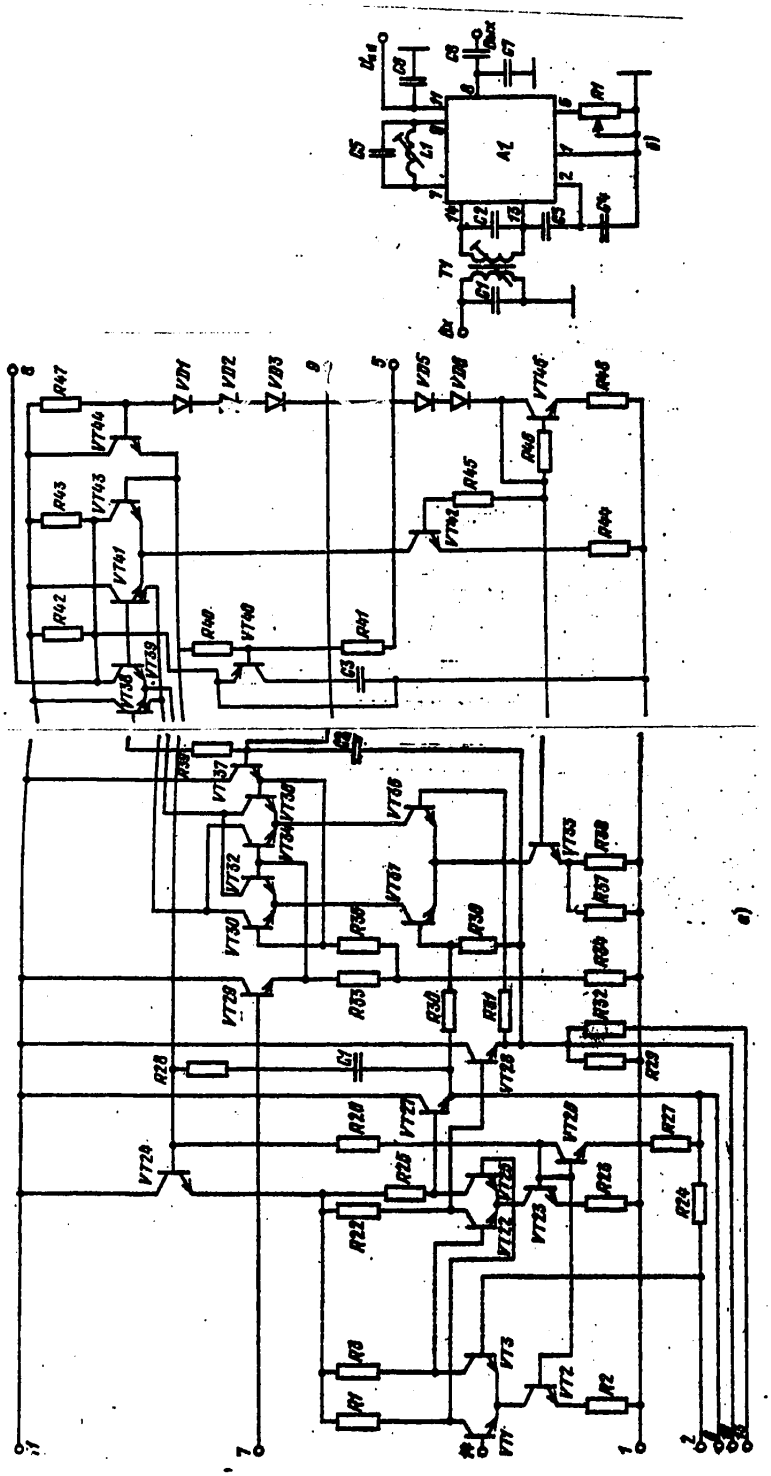


Figure 4.34. The K174UR1 intermediate frequency amplifier.

a. Basic electrical schematic;
b. Circuit configuration used as an audio channel amplifier for a television receiver.

The regulator governs the entire DC operation of the integrated circuit. To improve the frequency response, an equalizing capacitance C1 is introduced into the circuit. The unit gain frequency of this IC reaches 15 MHz, while the noise voltage referenced to the input in a frequency range of from 0.1 to 10 KHz is $\overline{U}_n$ = 1.2 μV with a gain of 500.

External feedback from the IC output to the emitters of the input stage (pin 5) is provided for normal operation of the amplifier. To achieve stable operation of the amplifier, the capacitance of the internal feedback capacitor C1 can be increased by connecting an external capacitor C3 (pins 6 and 7) in parallel with the internal capacitance.

4.5.3. Specialized Integrated Circuits

Integrated circuits are being developed at the present time for amplifying, limiting and detecting FM signals, as well as IC's for amplifying, converting and detecting AM signals, and frequency modulated IF amplifier systems.

The K174UR1 integrated circuit (Figure 4.34) is intended for applications as an audio channel IF amplifier in a television receiver. This IC can be used in the FM channels of radio receiving equipment. We shall consider its design.

The audio carrier is fed from the output of an external bandpass filter, which segregates the difference frequency of 6.5 MHz, to the input of a limiter-amplifier, which consists of eight series coupled differential amplifiers (transistors VT1--VT26) and two output emitter followers (transistors VT28 and VT27). The limiter-amplifier is looped by deep negative feedback through resistor R24, which suppresses the parasitic amplitude modulation (55 dB) in a wide dynamic range of input signal levels.

The limited signal is fed from the outputs of the amplifier string to the input of an FM quadrature detector, which takes the form of a balanced modulator, designed around transistors VT30--VT37. To obtain a signal which is shifted in phase relative to the input signal and to control the bases of the transistors of the detector multiplication circuitry (transistors VT29 and VT37), an external parallel resonant circuit tuned to a frequency of 6.5 MHz (Figure 4.34b) should be connected to pins 7 and 9.

The signal is fed from the output of the detector to the input of an electronic attenuator, the function of which is to preamplify the accompanying audio signal and provide for gain control. The electronic attenuator consists of two cross coupled differential amplifiers (transistors VT38--VT44), the arm of each of which is designed around a dual emitter transistor. The volume control is accomplished by means of a variable resistor connected between pin 5 and the common lead of the IC.

Because of the fact that the intercarrier sound does not pass through the volume control circuit, it is not subject to the influence of background hum and noise induction. This simplifies the remote control of the loudness. There is a regulator in the IC which is designed around diodes VD1--VD6, transistor

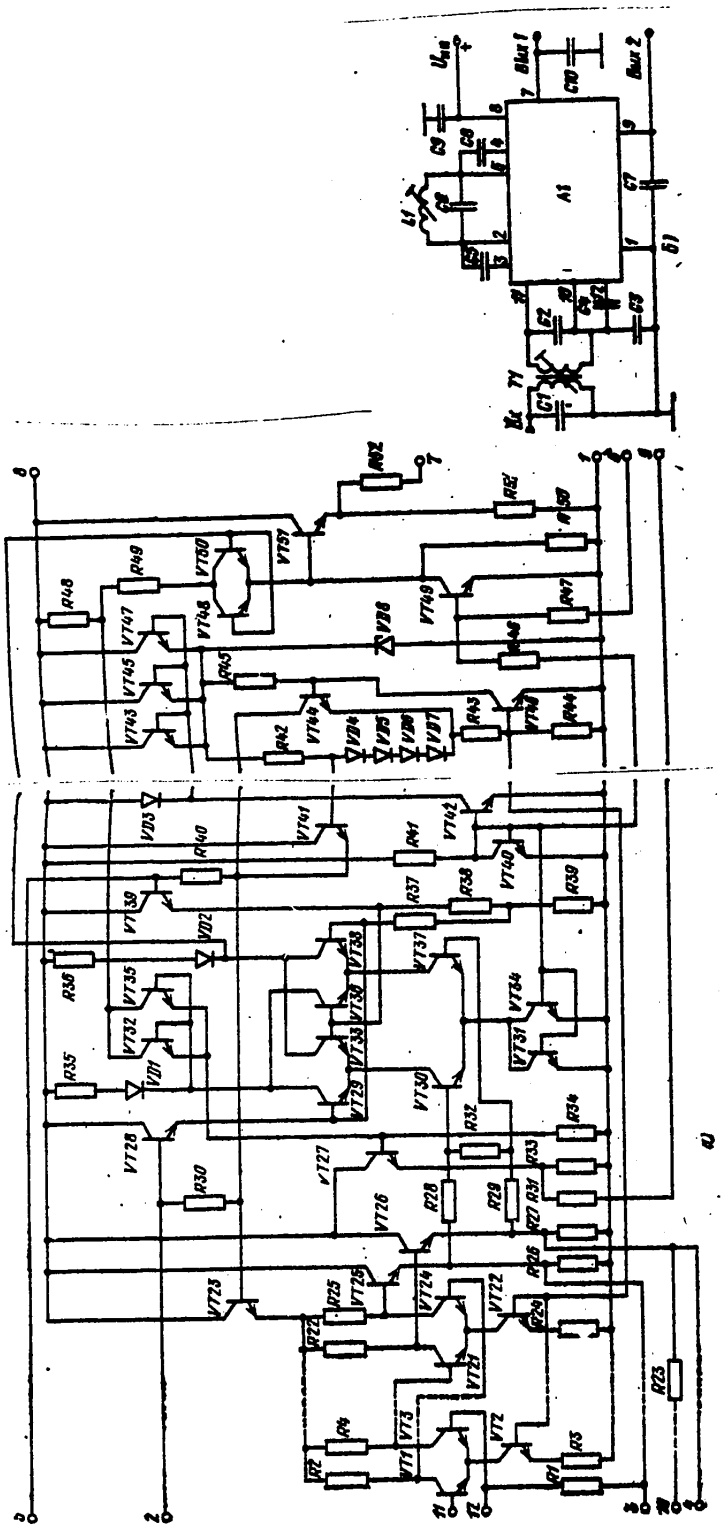


Figure 4.35. The 526UR1 intermediate frequency amplifier.
a. Basic electrical schematic;
b. Circuit configuration when used as an audio channel amplifier in a television receiver.

VT45 and resistors R46 and R48. It reduces the influence of a change in the supply voltage on the amplifier parameters.

The 526UR1 integrated circuit (Figure 4.35a) is also intended for use as an audio channel IF amplifier in a television receiver. This IC can also be used in other FM channels. As can be seen from the basic schematic, the 526UR1 IC is also constructed based on a combination of the differential amplifier and multiplier circuits treated above.

The broadband amplifier (transistors VT1--VT22) serves as a limiter-amplifier with a high value of amplitude modulation suppression (no less than 40 dB). The limited signal is fed to the reference input of the balanced modulator (the bases of transistors VT30 and VT37), as well as to the frequency dependent quadrature network, which includes external capacitor C, as well as the LC network which is connected to the second input of the multiplier between pins 4 and 3. The quadrature circuit converts the frequency modulated signal to a phase modulated one, which is then detected by the balanced multiplier.

The demodulated signal is fed through a level reduction circuit (attenuator, transistors VT48 and VT50) to an audio preamplifier with electronic gain control (the control signal is fed to pin 10). The 526UR1 integrated circuit has a low frequency output voltage of U_{out} audio = 150 mV when U_{pwr} = 12 volts.

The K174UR2 integrated circuit (Figure 4.36), besides its main function (video channel IF amplifier in a television receiver), may also be used to construct a high fidelity AM receiver. The intermediate frequency is fed from the output of an external lumped constant selective filter to the IF amplifier, which has three stages (transistors VT1, VT3, VT5, VT7, VT10, VT11, VT12, VT17, VT18, VT19, VT22 and VT23).

Electronic gain control is provided in the first two stages, which are designed in a complex differential circuit with a common collector-common emitter configuration. Identical diode structures, VD4, VD5, VD9 and VD10, the bias current of which is controlled by changing the automatic control voltage, are used for this. The paraphase AM signal is fed from the output of the IF amplifier to the inputs of a detector designed in a balanced multiplier circuit configuration (transistors VT33, VT34, VT35, VT46, VT47 and VT49) as well as a limiter (transistors VT28 and VT29). An external parallel tuned circuit, which is tuned to the intermediate frequency (38 MHz) is connected to the output of the limiter (pins 8 and 9 in Figure 4.36b). The internal resistors R61 and R64 of 5.1 KOhms each are used in this mode. The signal is fed from the output of the amplitude limiter to the reference input of the detector (transistors VT39 and VT44). When two signals are present in the detector, a video signal is produced at its output.

Besides the video signal, there are the doubled intermediate frequency of the audio subcarrier and the doubled intermediate frequencies of the chrominance subcarriers which appear at the output of the detector. This is due to the presence of square-law components in the amplitude response of the detector.

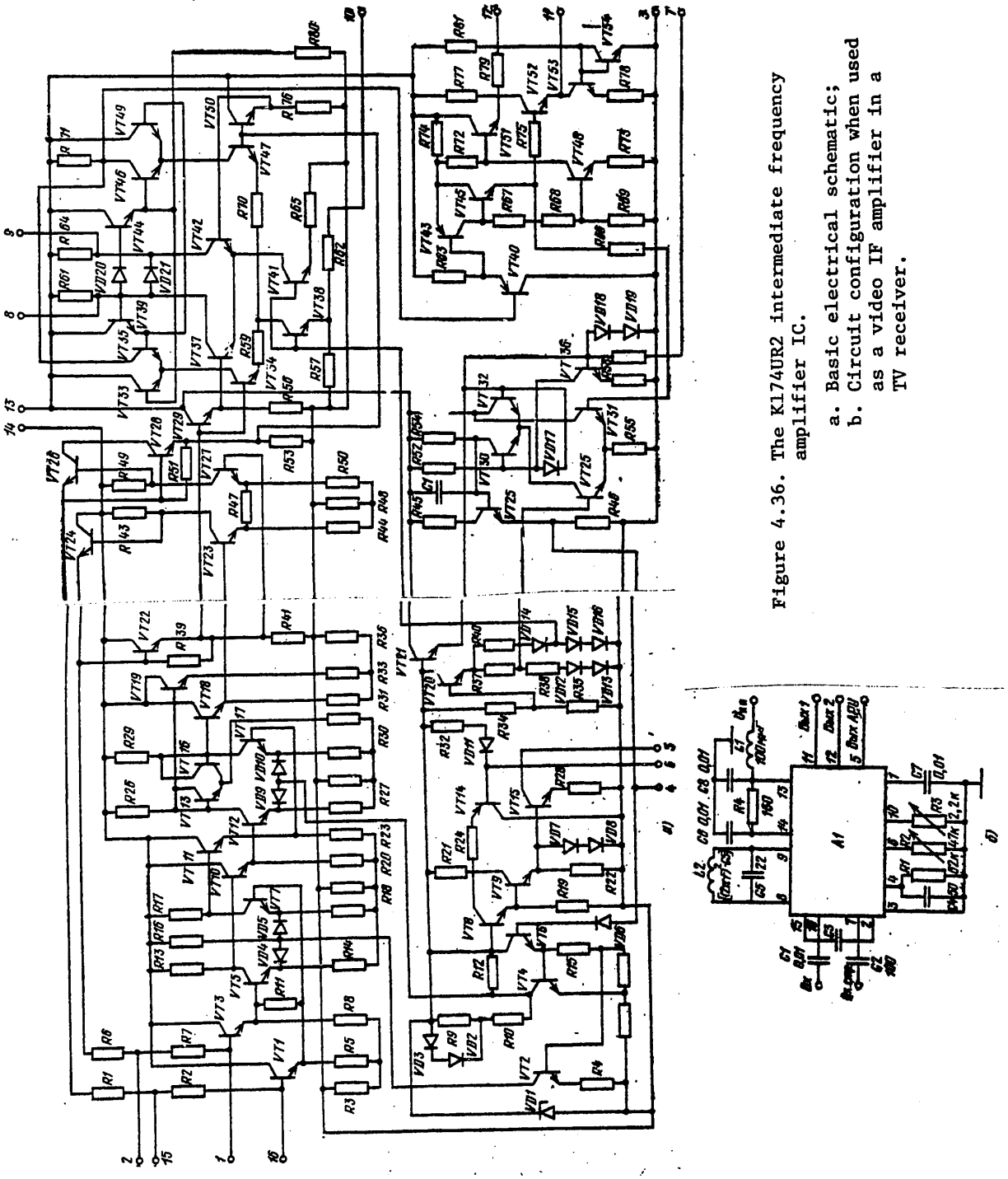


Figure 4.36. The K174UR2 intermediate frequency amplifier IC.

a. Basic electrical schematic;
b. Circuit configuration when used as a video IF amplifier in a TV receiver.

The audio signal and the chrominance difference signals can be segregated from the video signal by means of frequency detectors after further amplification in the other units of a television receiver. The positive polarity video signal is fed to pin 11 while the negative video signal is fed to pin 12 from the output of the detector through the video preamplifier (transistors VT40, VT43, VT45 and VT51) and the phase inverter (transistor VT52).

Because of the fact that the AGC system should respond to the average value of the received signal voltage, an AGC keying system is used in the IC in which data on this signal is used which is contained in the horizontal blanking pulse. At the moment when the horizontal blanking pulse arrives at the input to the keying amplifier (pin 7) from the preamplifier, it charges capacitor C1, which is incorporated in the keying amplifier circuitry, until reaching the corresponding voltage which is also used as the control voltage for the operation of the AGC system.

The AGC voltage is fed from the output of the keying amplifier to the input of the regulating amplifier (transistors VT2, VT4). By connecting a capacitor and resistor in parallel to pin 4, one can change the AGC time constant. This pin can be used as the input for manual gain control. The AGC voltage is fed from the input of the regulating amplifier to the electronic gain control outputs of the IF amplifier stages and to the input of the threshold amplifier.

The AGC voltage is fed from the output of the keying amplifier to the input of the regulating amplifier (transistors VT1, VT4). By connecting a capacitor and resistor in parallel to pin 4, one can change the AGC time constant. This pin may also be used as an input for manual gain control. The AGC voltage is fed from the output of the regulating amplifier to the electronic gain control inputs of the IF amplifier stages and to the input of the threshold amplifier. [Translator note: Near duplication of these two paragraphs appears in original; apparently editorial error].

The AGC voltage is fed from the output of the threshold amplifier to pin 5 and is used as the AGC in other units of the television receiver (in the IF preamplifier or in the television channel switcher). The actuation threshold for this amplifier is set by means of an external resistor, which is inserted between pin 6 and the common lead of the IC. The AGC level is adjusted by means of an external resistor, which is inserted between pin 10 and the common lead of the IC. A provision is made in the integrated circuit for temperature compensation for the change in the electrical characteristics of the detector and the keying amplifier.

4.5.4. IC's for the Construction of Selective Circuits

Work on the design of semiconductor IC's for selective circuits is going in several directions (for example, IC's are being developed for active filters, as well as IC's which use the phase-locked loop principle [19]). The use of semiconductor integrated circuit technology makes it possible to find circuit design solutions which improve the quality of these devices and substantially reduce the dimensions of selective circuits as compared to similar devices using discrete components.

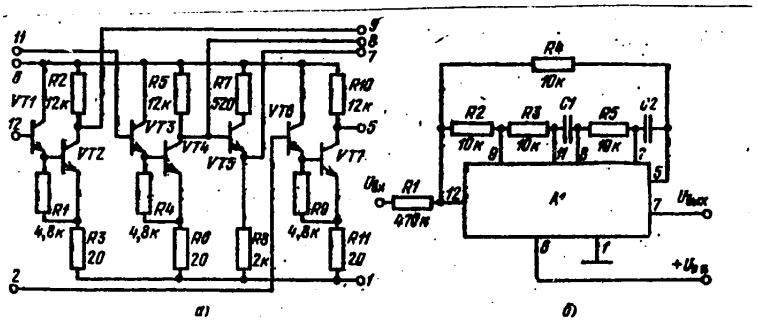


Figure 4.37. The 529UP1 amplifier.

a. Basic electrical schematic;
b. Design example of a low pass filter.

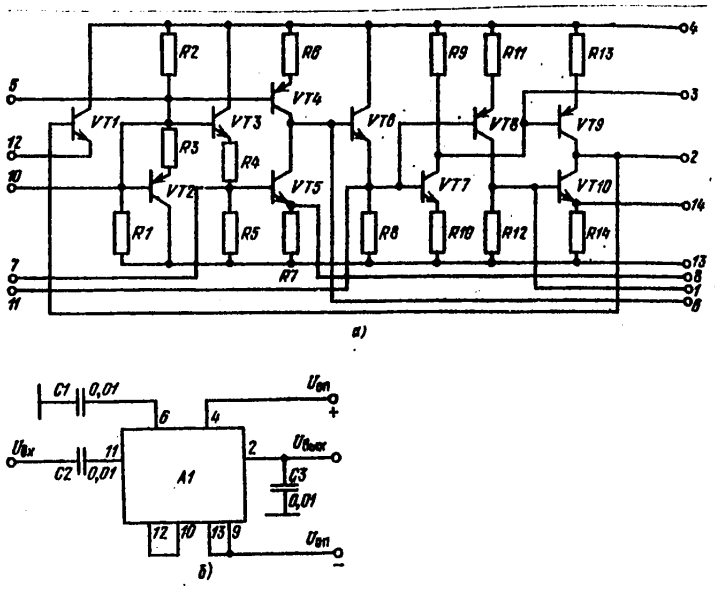


Figure 4.38. The K283SS1 gyrator.

a. Basic electrical schematic;
b. "Grounded" inductance circuit configuration.

When designing semiconductor IC's for active filters, the primary attention is devoted to the development of the basic operational amplifiers. The op amp configuration as a second order filter section is the most widespread in active RC filter circuits. This filter section is based on integrators, and for it, three high quality amplifiers are required. In a number of cases, when elevated requirements are not placed on the sensitivity and Q of filters, one can use comparatively simple IC's with a low gain. For example, the 529UP1 integrated

circuit (Figure 4.37) contains three identical amplifiers on a single chip (overall current consumption of 3 mA and a single power supply voltage of 6 volts), each of which has an input impedance of 30 KOhms and a gain of 40 dB. A typical active filter section with a Q of 50 in a frequency range of up to 200 KHz is realized on the basis of this IC.

The research which has been done in the field of IC design for another class of active filters, gyrators, shows that the existing circuit design techniques for the construction of semiconductor IC's make it possible to effectively solve one of the major problems of the practical realization of gyrator circuits: assuring the stability of the DC mode when the parameters of the components change and when adjusting the value of the gyrator conductance.

Hybrid IC's - the K283SS1--K283SS9 [20] (Figure 4.38) - make it possible to realize an "inductance" with a range of nominal values of from 1 mHy up to 100 Hy at frequencies of from 1 to 300 KHz with a Q of from 10 to 500 and a permissible deviation in the gyration impedance of $\pm$ 3%. These IC's are powered from two supplies with a voltage of $\pm$ 6 volts.

The active filter IC's treated here can be used in low frequency audio channels of receivers. When developing IC's for high frequency selective circuits, it has proved to be convenient to use the principle of phase automatic frequency control (FAPCh) [PLL - phase locked loops]. A PLL system contains an oscillator, which is voltage controlled, a phase detector and a low pass filter.

The development of IC's employing the PLL principle is one of the promising trends at the present time in work on high quality radio receivers, which will make it possible to reduce the number of inductances, and consequently, the dimensions of the device. A further improvement in semiconductor IC's by means of increasing the level of integration and expanding the functional capabilities opens up the prospects of fabricating entire functional assemblies of communications equipment in a single production process cycle.

4.6. Integrated Circuits for Analog to Digital and Digital to Analog Data Conversion

Mutual digital and analog data converters are broken down into two groups: analog to digital converters (ATsP) [A/D converters], which serve to convert an initial analog quantity to a digital equivalent (or code) corresponding to it, as well as digital to analog converters (TsAP) [D/A converters], intended for generating an analog output quantity corresponding to the digital code fed to the converter input [21, 22].

D/A and A/D converters consist of digital and analog circuits. The digital circuits (counters, registers, decoders, adders, programming memories) control the conversion process in accordance with the conversion algorithm. Analog circuits generate highly stable reference voltages, which switch the analog levels, amplify and convert them on a specified scale, and realize instantaneous storage and integration. Sets of IC's are being produced at the present time for the construction of the analog circuits of D/A or A/D converters. The breakdown of

a converter into several IC's, which takes place because of technological reasons, also has its positive aspects, since it makes it possible to construct various types of converters in terms of their resolution using a single set of IC's.

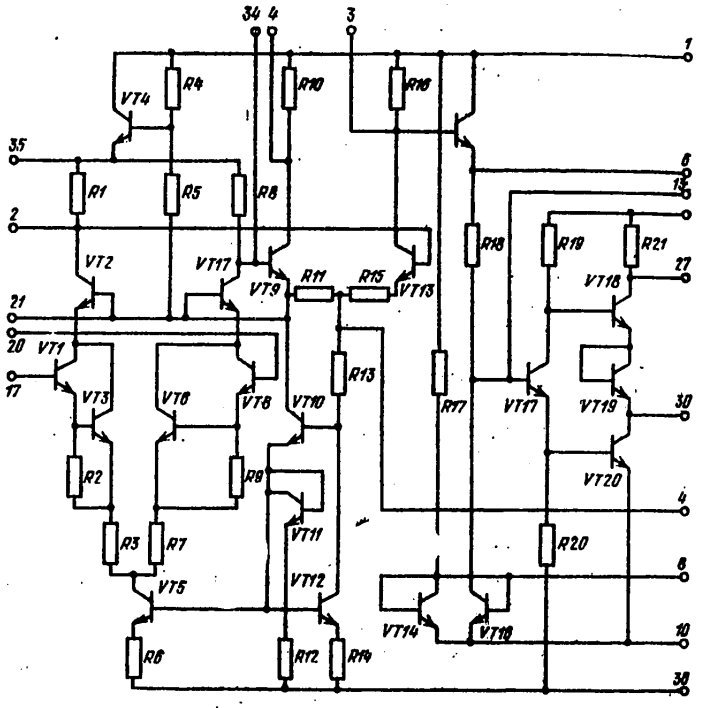


Figure 4.39. Basic electrical schematic of the voltage comparator incorporated in the 240SA1 IC's.

The type and number of IC's needed for the construction of the digital circuits of A/D and D/A converters is governed by the procedure chosen for signal conversion, the requisite speed and the number of bits. CMOS circuits are used here for economical devices, TTL integrated circuits are used for standard devices and ECTL for high speed converters.

One can use the hybrid IC's of the 228, 240, 265 and 252 series for the design of the analog circuits. The 240 series is a functionally complete set of IC's, which is intended for the construction of multichannel (up to 30 channels) [23] 10 digit A/D converters with an input voltage range of $\pm$ 5 volts and a conversion time for the maximum input voltage to a binary code of $\overline{100}$ microseconds. Six [sic] types of analog IC's are incorporated in the 240 series: the 240 SA1, 240 UD1, 240 KN1, 240 KN2 and 240 KN3.

The 240 SA1 integrated circuit (Figure 4.39) is a voltage comparator, which is intended for performing the operation of comparing two analog quantities, with a resolving power of no less than 2 mV, and has an input impedance of 1 MOhm. The comparator is designed in a two stage configuration. The input differential

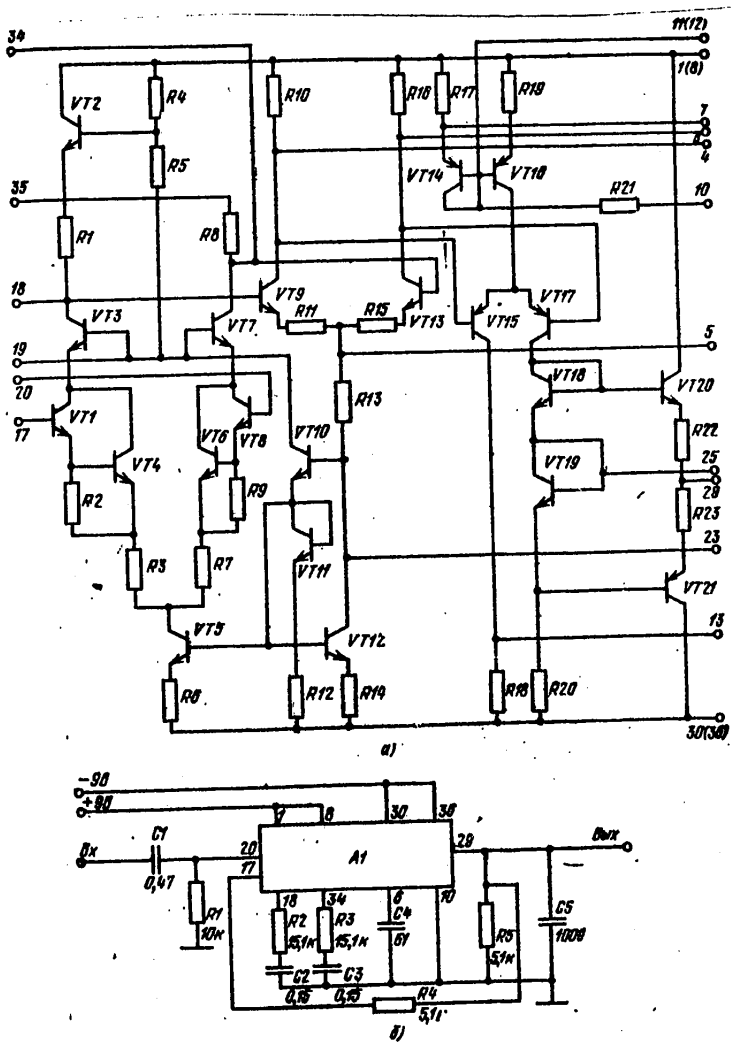


Figure 4.40. The 240UD1 operational amplifier.

a. Basic electrical schematic;
b. Circuit configuration.

stage has transistors connected in a Darlington configuration to increase the input impedance. The use of the 129NT1 integrated circuit pair in the input stage has made it possible to obtain a good bias voltage (2 mV). In order to limit the maximum positive output voltage to the level permissible for logic elements, the output stage is powered at a reduced voltage of +5 volts. The comparator can generate a current of up to 12 mA in a load, where the slew rate of the output voltage exceeds 10 volts/μsec.

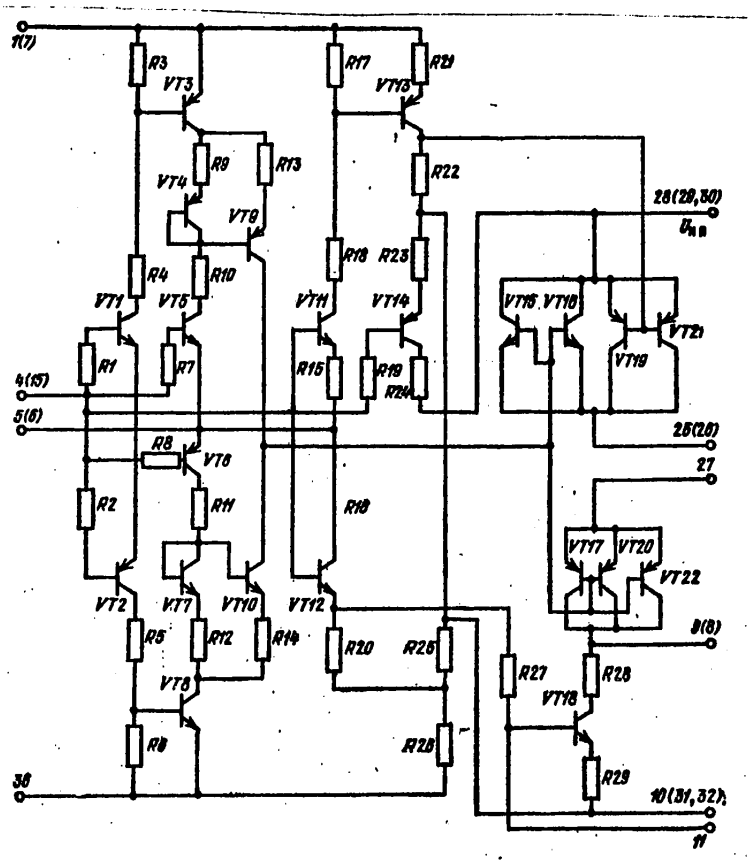


Figure 4.41. The 240KN1 analog switch.

The 240UD1 operational amplifier (Figure 4.41) operates as the input signal amplifier of an A/D converter, as well as an amplifier which sums the input currents in a D/A converter. Two differential amplifier stages and a differential follower make it possible to obtain an internal gain in excess of 8,000 in a wide band of frequencies (more than 100 KHz). An emitter follower (transistor VT10) provides for a high common mode rejection ratio. The input differential stage, designed as a Darlington configuration, has an input impedance of about 1 Mohm, an average input current of I_{in} = 1.5 microamps, and an input current difference of ΔI_{in} = 0.2 microamps. The amplifier bias voltage is U_{bias} = 2 mV, while its temperature drift is U_{bias} = 10 μV/°C. The output power amplifier stage generates a current of 5 mA in the load. Two frequency equalization circuits are introduced into the circuitry to improve the frequency response; in this case, the output voltage slew rate is 2.1 V/μsec.

The 240KN1A,B analog switch (Figure 4.41) is designed for connection of either a positive or a negative reference voltage at the output (depending on the input signals).

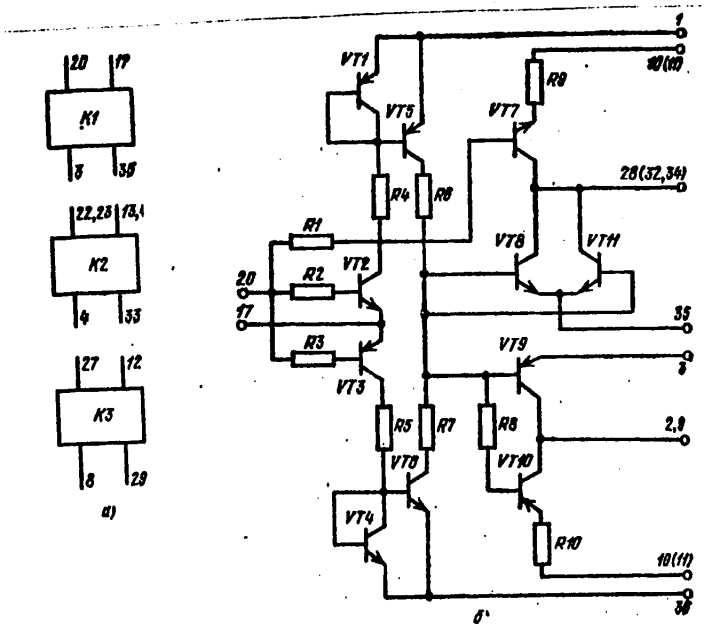


Figure 4.42. The 240KN2 analog switch.

a. Block diagram;
b. Basic electrical schematic.

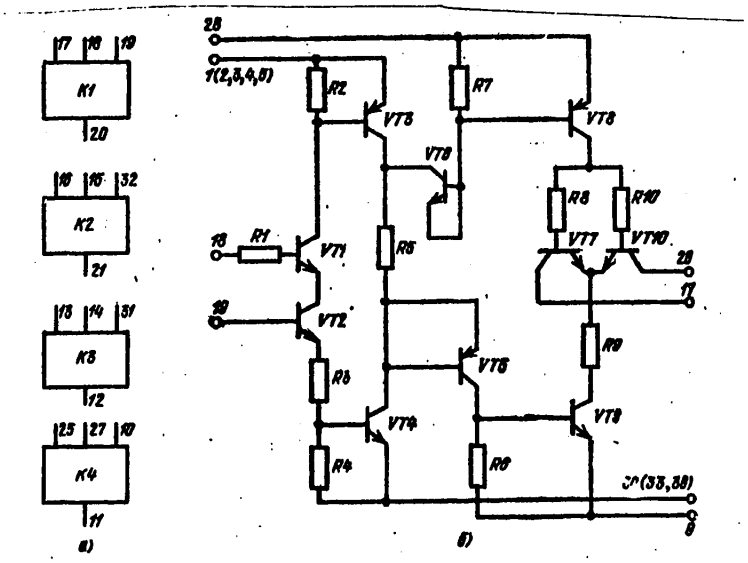


Figure 4.43. The four bit 240KN3 switcher.
a. Block diagram; b. Basic electrical schematic.

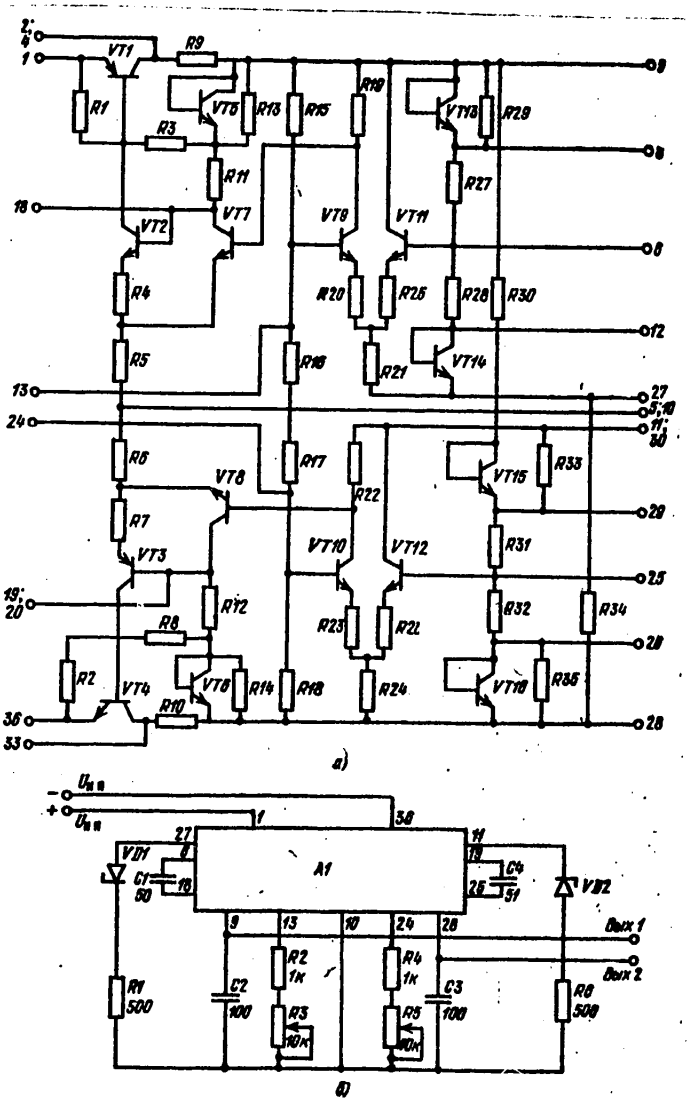


Figure 4.44. The 240YeN1 voltage regulator.

a. Basic electrical schematic;
b. Circuit configuration.

If a "1" is fed to pin 4, while an "0" is fed to pin 5, a positive reference voltage appears at pins 26 and 25. If the potentials at the input change places, then a potential close to zero will appear at pins 26 and 25, while a negative reference voltage will appear at pin 27. The error in the transmission of the reference voltages is $\pm$ 2.5 mV for the 240KN1A switch and $\pm$ 5 mV for the 240KN1B.

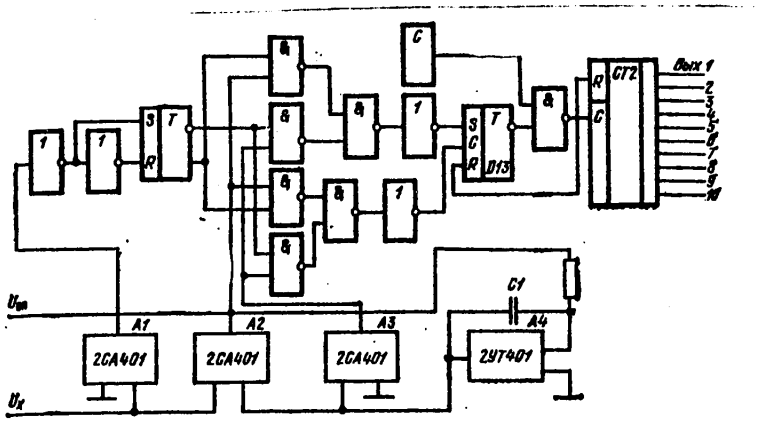


Figure 4.45. Block diagram of a double integration analog to digital converter.

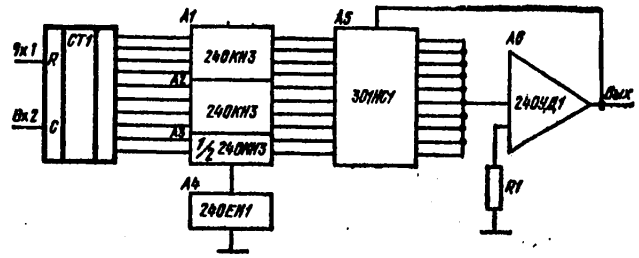


Figure 4.46. Block diagram of a 10 digit digital-analog converter.

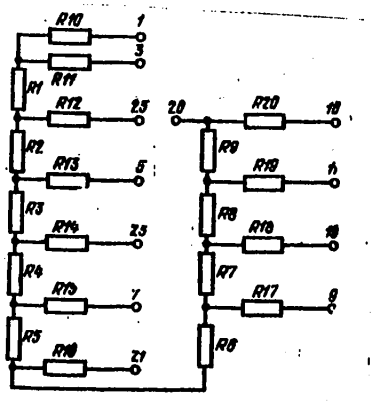


Figure 4.47. Basic electrical schematic of the 301NS1 resistive matrix.

The block diagram of the 240KN2 integrated circuit (Figure 4.42) contains three bit reference voltage switches having a transmission error of ± 10 mV. By feeding a "1" potential to pin 20 and an "0" to pin 17, we obtain the positive reference voltage at pin 35 and a voltage close to zero at pin 3. If the potentials at the inputs are changed to the opposite values, then a negative reference voltage will appear at pin 3, while a voltage close to zero will appear at pin 35.

The four bit 240KN3 switcher (Figure 4.43) is designed for switching negative and positive polarity

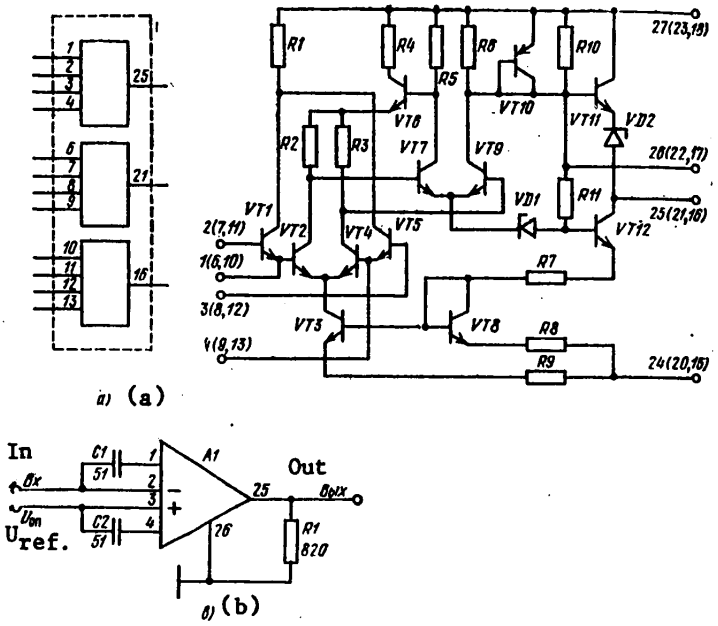


Figure 4.48. The 252SA1 comparator.

a. Block diagram;
b. Basic electrical schematic of a single comparator;
c. Circuit configuration for a single comparator.

voltages of ± 5 volts, depending on the control signal levels. The switch in the 240KN3 integrated circuit has a residual voltage of 1 mV, a leakage current of the turned-off switch of 100 nA, a resistance of the turned-on switch of 100 ohms and a switching time of 1.0 μsec. The switch operation can be analyzed using the first channel as an example. When the "1" level is fed to pin 18 and the "0" level is fed to pin 19, the switch turns on, and the signal passes from pin 17 to pin 20. When the potential at pins 18 and 19 changes, the switch cuts off and the signal does not get from pin 17 through to pin 20.

The 240YeN1 voltage regulator (Figure 4.44) makes it possible to obtain a stabilized voltage of ± 5 volts with an instability in the output voltage with respect to current and voltage of no more than 0.06%; the average temperature coefficient of the output voltage is no more than 0.005%/°C and the load current for each output runs up to 25 mA. The regulator does not have an internal reference voltage source, because of which, the reference voltage supplies are designed around external zener diodes VD1 and VD2; the output voltages are adjusted by variable resistors R3 and R5.

The 240 series integrated circuits are made using hybrid film technology and use active outboard elements of the 129NT1B, V, 2T202, 2T332, 2T364, 2T360, etc. types, assembled in a 155-36-1 package and operate from a ± 9 volt ± 10% power

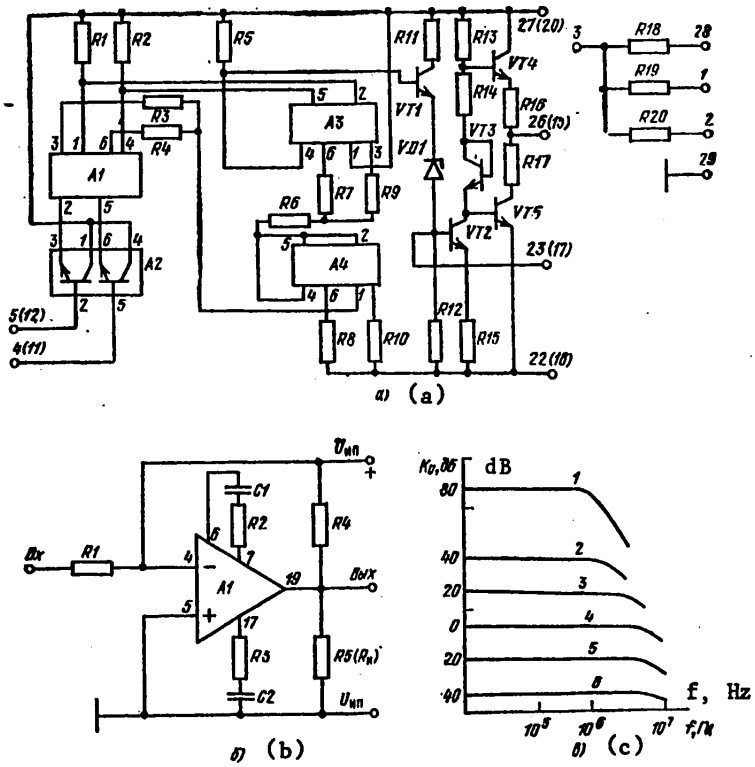


Рис. 4.49. Операционный усилитель типа 252УД1:
а — принципиальная электрическая схема, б — схема включения, в — зависимость коэффициента усиления от частоты

Curve. Кривая	R_1, Ом Ohms	R_{oc}, кОм Kohms	$C_{1,6}$, пФ pFd	C_2, пФ pFd
1 (без ОС) (1)	—	—	0	0
2	51	6,2	390	10^4
3	26	1,2	1300	240
4	10	7,5	4700	2400
5	2	2,7	9400	10^4
6	2	8,2	10	10^4

Figure 4.49. The 252UD1 operational amplifier.

a. Basic electrical schematic;
b. Circuit configuration;
c. The gain as a function of frequency:

Key: 1. (Without feedback).

supply. The curves for the electrical parameters of the 240 series analog IC's as a function of temperature are given in [23]. The 240 series was developed for the construction of double integrating A/D converters (Figure 4.45). The digital portion of this circuit can be constructed using any TTL integrated circuit.

The addition of a resistive matrix expands the functional capabilities of the 240 series. When using such matrices, the series can be employed to construct D/A converters and other kinds of A/D converters. The possible circuit of a 10 bit D/A converter using a 301NS1 integrated circuit is shown in Figure 4.46.

The matrices of R - 2R resistors are intended for converting a parallel digital code to the corresponding voltage level at the output. The major characteristics of the 301NS1 R - 2R resistive matrix (Figure 4.47) are: a division factor K of from 1/1024 to 1023/1024, a division step of h (1/1024), a relative division error δ% ($\pm$ 0.0135), the scatter in the nominal values of the resistors, ΔR, is 0 to 100 ohms, as well as a maximum input voltage U_{in} of 12.6 volts.

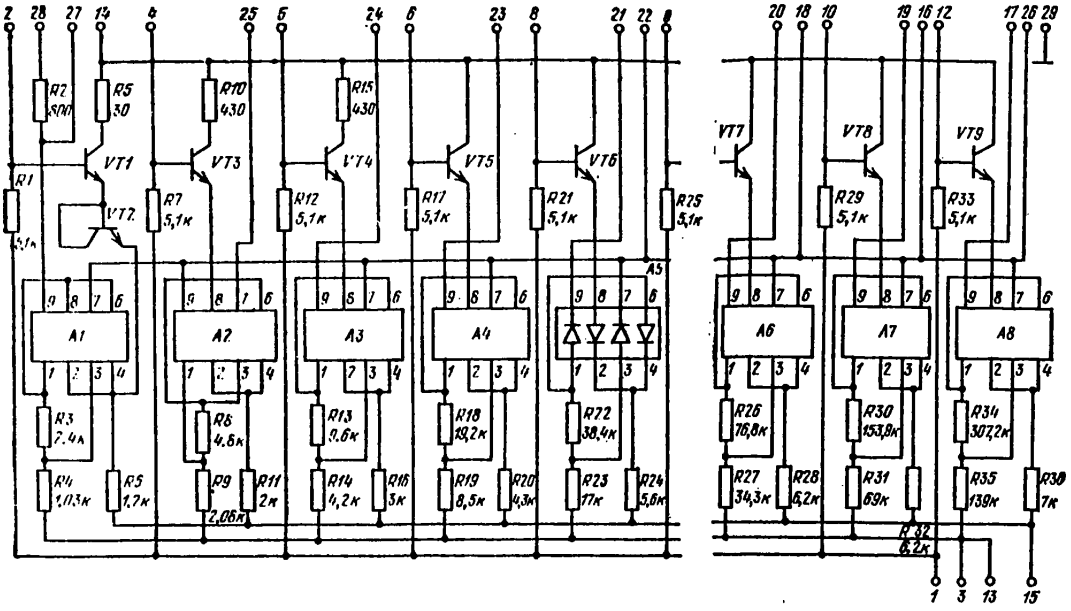


Figure 4.50. The basic electrical schematic of an 8 bit digital/analog converter which converts to a positive polarity current.

Another set of IC's intended for construction of A/D and D/A converters is the 252 series, which consists of seven types of IC's, based on which one can construct 8 to 10 bit converters for analog signals represented in the form of positive or negative voltages.

Included in the complement of the 252SA1 integrated circuit (Figure 4.48) are three comparators with a current sensitivity of better than 2 microamps. The two stage comparator circuit provides for a voltage gain of no less than 1,000. The input stage of the comparator is designed in a complex differential circuit configuration and makes it possible to configure the comparator both with a high

input impedance (the utilization of an input emitter follower: transistors VT1 and VT5), and with a reduced input impedance (the signal is fed to the bases of transistors VT2 and VT4). The 252SA1 comparator has an output voltage slew rate of no less than 30 V/μsec for an input signal voltage of 10 mV (the emitter follower inputs are used in this mode).

Incorporated in the 252UD1 integrated circuit (Figure 4.49) are two operational amplifiers with feedback resistors. Each op amp is designed in a two stage configuration. Two differential stages and a power gain stage provide for a gain of no less than 7,000. The input differential stage, the arms of which use Darlington circuits, is characterized by the following input parameters: $R_{in} \leq$ 900 KOhms, $U_{bias} \leq 12$ mV; $I_{in} \leq 0.1$ μA and $\Delta I_{in} = 0.02$ μA. To increase the input impedance of the op amp and expand its gain bandwidth, inserted in the emitter circuits of the input stage are resistors having a nominal value of 50 ohms. An improvement is made in the frequency response of the operational amplifier through the choice of the external frequency equalization networks; in this case, the small signal passband of the op amp (when $U_{in} = 0.1$ volts) is about 6 MHz and the output voltage slew rate is 5 V/μsec. The nominal values of the frequency equalization components should be chosen as a function of the gain by means of Table 4.7.

TABLE 4.7. The Choice of Equalization Elements for the 252UD1 Operational Amplifier

K_U (1)	C_1, пФ pFd	R, Ом Ohms	C_2 пФ pFd	R_8, кОм Kohms
∞	0	0	0	0
100	3,90	51	10	8,2
10	1300	26	240	1,2
1	4700	10	240	0,75

Key: 1. Voltage gain, K_U.

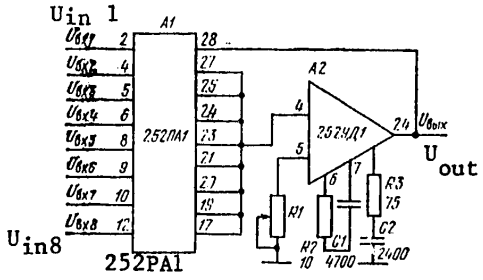


Figure 4.51. Block diagram of an 8 bit digital to analog converter converting to negative polarity current.

The 252PA1 integrated circuit is an 8 bit binary code to positive polarity current converter (Figure 4.50) and consists of 8 switches and a resistive matrix. The switches, depending on the digital combination at the IC inputs, control the output current of the matrix. When a signal which turns on the switch appears at the circuit input, a current flows in the load, which is normalized by the resistances of the matrix and the reference supply voltage. The relative conversion precision in this circuit is no worse than $\pm$ 0.4%; the current levels in each bit of the converter are given in Table 4.8. In order to construct a binary code to voltage A/D converter, it is necessary to connect an operational amplifier at the output of the 252PA1 integrated circuit, where this amplifier sums the bit currents (Figure 4.51). In this case, we obtain a D/A converter for a negative polarity.

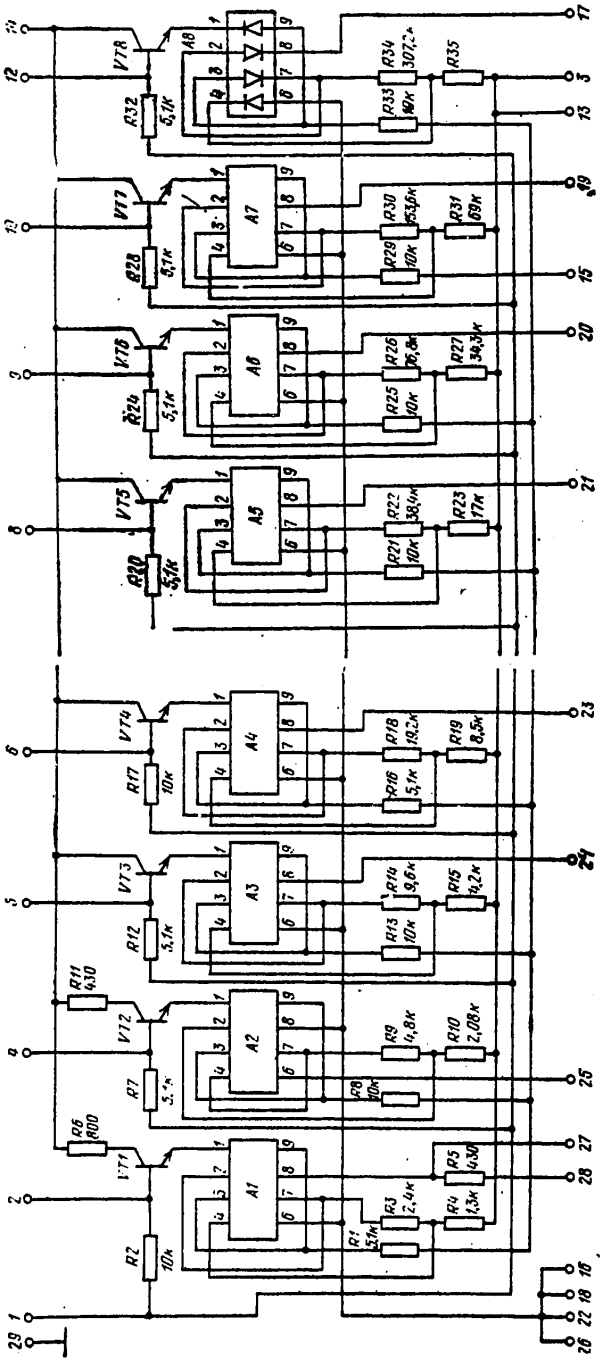


Figure 4.52. Basic electrical schematic of an 8 bit digital to analog converter converting to negative polarity current.

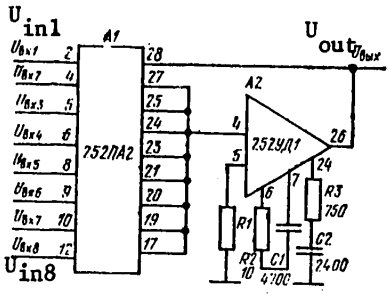


Figure 4.53. Block diagram of an 8 bit digital to analog converter, which converts to positive polarity current.

The 252PA2 (Figure 4.52) 8 bit binary code to negative current converter is distinguished from the preceding by the polarity of the diodes and the reference power supplies. The relative conversion precision is also no worse than 0.4%; the levels of the bit currents correspond in absolute value to the analogous currents in the 252PA1 integrated circuit. When a summing amplifier is connected to the 252PA2 integrated circuit, we obtain a positive polarity digital to analog converter (Figure 4.53).

A 10 bit binary code to negative current converter can also be designed using two 252PN1 and 252PA3 IC's, where the resistive matrix and diode switches are incorporated in the 252PN1 integrated circuit (Figure 4.54), while the 252PA3 IC contains the control circuitry (Figure 4.55). The relative operational precision of this converter is no worse than $\pm$ 0.1%.

The block diagram of a 10 bit D/A converter (Figure 4.56) is based on the 252PA3, 252PA1 and 252UD1 integrated circuits. The four-channel 252KN1 current switcher (Figure 4.57), which is intended for the distribution of bipolar current signals at a frequency of from 0 to 60 MHz with a transmission gain of 0.8 and a switch on to off transmission ratio of 40 dB is included in the 252 series for the construction of multichannel D/A converters. The 252KN1 integrated circuit is powered by two power supplies at $U_{sup} = \pm$ 6 volts ($\pm$ 1%) and switches a current of up to 2 mA. An analog memory circuit can be designed around the 252KN1 and 252UD1 integrated circuits (Figure 4.58).

There are no regulators in the 252 series, and for this reason, one can use integrated circuit stabilizers from the 275 or 142 series as the reference voltage sources.

A prerequisite for the transition to the production of D/A and A/D converters as functionally complete assemblies (even on one substrate) was the creation of a broad component base of operational amplifiers, comparators, analog switches and keyers, digital IC's as well as reference voltage sources. Success in thin film technology is also of great importance, which made it possible to create sets of precision resistors.

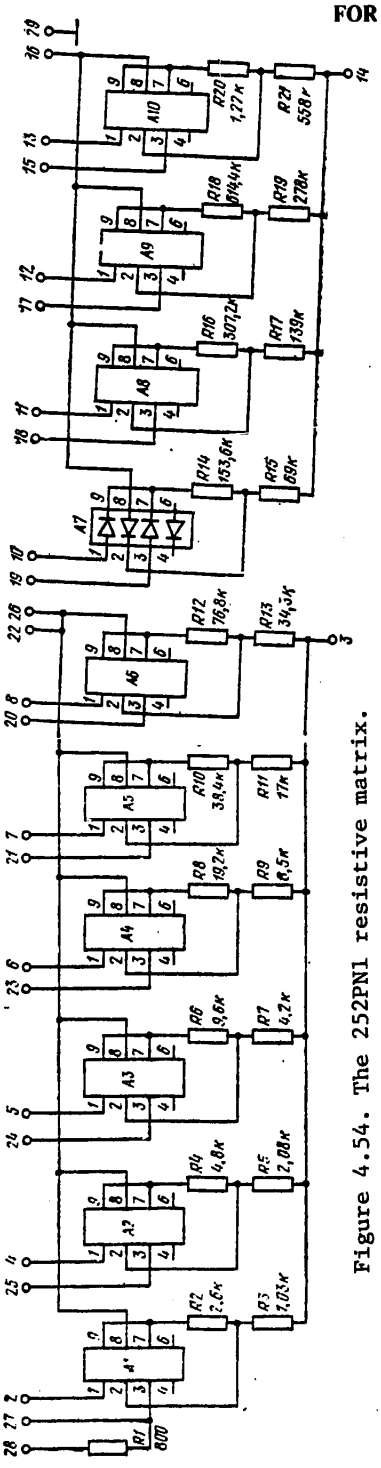


Figure 4.54. The 252PN1 resistive matrix.

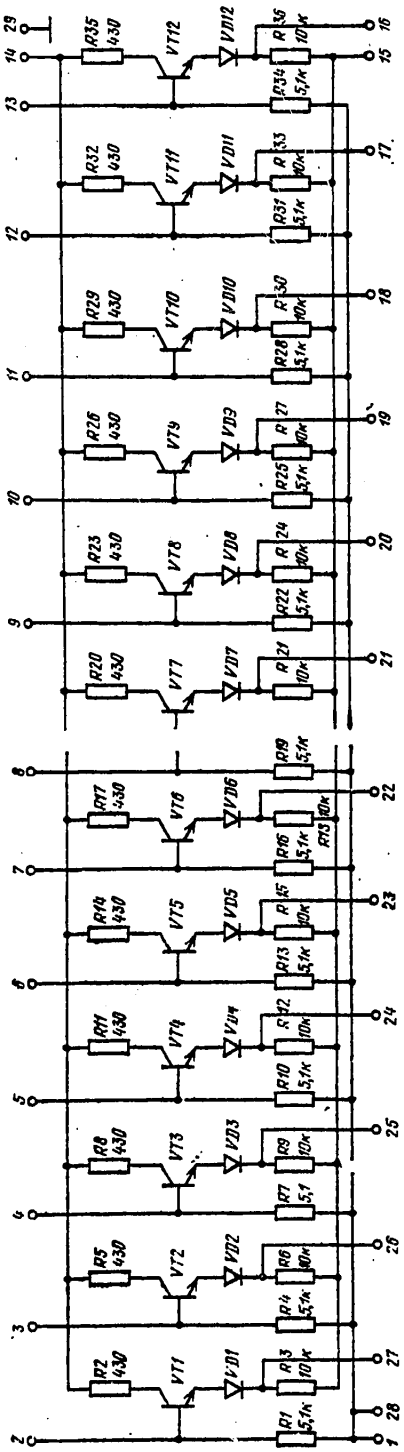


Figure 4.55. Basic electrical schematic of the 252PA3 controller.

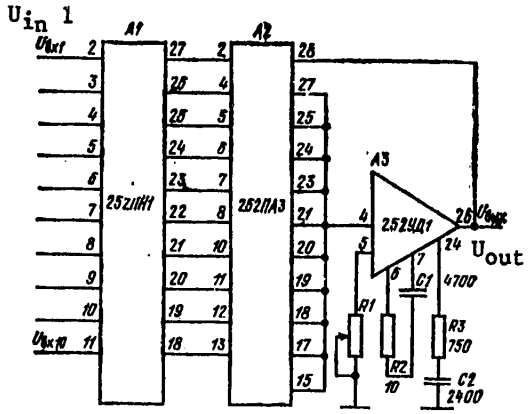


Figure 4.56. Block diagram of a 10 bit digital to analog converter, which converts to negative polarity.

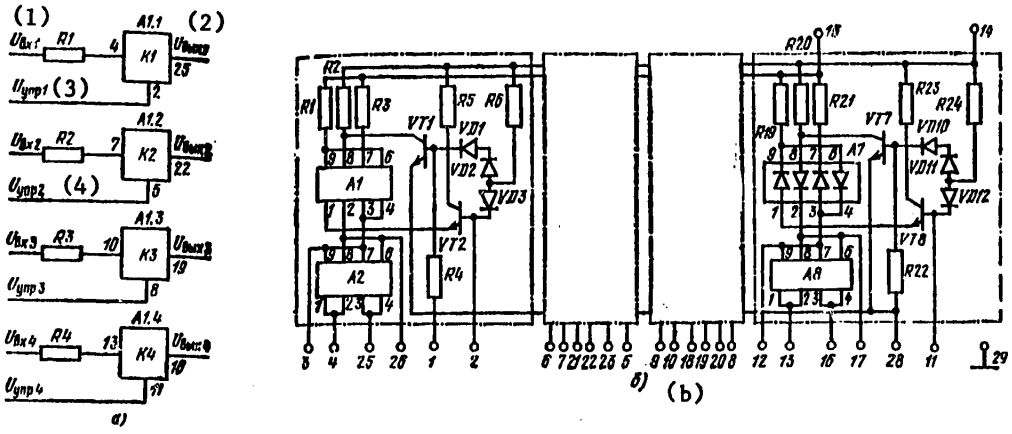


Figure 4.57. The 252KN1 four-channel switcher.

a. Block diagram;
b. Basic electrical schematic.

Key: 1. Input voltage 1;
2. Output voltage 1;
3. Control voltage 1;
4. Control voltage 2.

TABLE 4.8. Parameters of the 252PA1, PA2 and PA3 Integrated Circuit Converters

Parameters / Параметры	252PA1, 252PA2 / 252ПА1, 252ПА2	252PA3 / 252ПА3
Bit Currents / Токи разрядов, мА I_1	2,5±0,125	2,5±0,125
I_2	(1/2)I_1±0,2%	(1/2)±0,1%
I_3	(1/4)I_1±0,4%	(1/4)I_1±0,2%
I_4	(1/8)I_1±0,8%	(1/8)I_1±0,2%
I_5	(1/16)I_1±1,6	(1/16)I_1±0,4%
I_6	(1/32)I_1±3,2	(1/32)I_1±0,4%
I_7	(1/64)I_1±6,4%	(1/64)I_1±0,8%
I_8	(1/128)I_1±12,8%	(1/128)I_1±1,6%
I_9	—	(1/256)I_1±3,2%
I_{10}	—	(1/512)I_1±6,4%
(1) Суммарный входной ток разрядов, мА	5±0,25	5±0,25
(2) Максимальный уровень входного напряжения управления, В	4	4
(3) Ток потребления по цепи управления одним разрядом, мА	1	—

Key: 1. Total input bit current, mA;
2. Maximum level of the input control voltage, volts;
3. Current consumption for the control circuit of a single bit, mA.

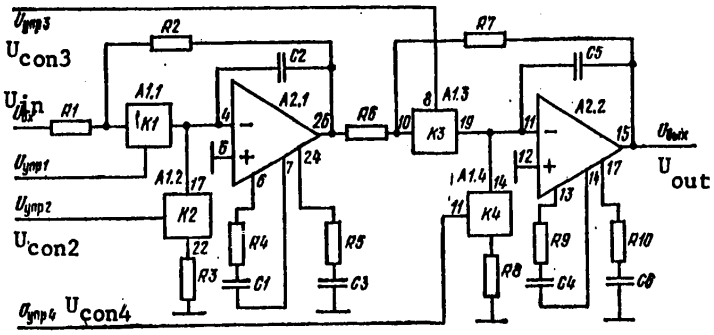


Figure 4.58. Block diagram of an analog memory.

4.7. Analog Switches

Analog switches (AK) are used for switching analog signals in analog to digital and digital to analog data conversion circuits. Moreover, analog switchers are used as switching components in telemetry, blanking, data multiplexing circuits, as well as choppers in operational amplifier circuits with signal spectrum conversion [25].

The following parameters are the classification criteria for analog switches: the turned-on switch resistance R_0, the residual voltage U_{res} across the closed switch, the leakage current of the channel I_{leak}, the resistance of the turned-off switch R_{off}, the input impedance of the control circuit R_{in}, the switchable current I_{switch} (or voltage U_{switch}), the level of the control signal current I_{con} (or voltage level U_{con}), as well as the turn on and off speed. Both bipolar and unipolar structures are used for the design of analog switches. An analog switch can be designed in the form of an individual IC, or it can be composed of several IC's and other components.

Bipolar integrated choppers of the 101KT1 and 124KT1 types (Figure 4.59), based on the series compensation effect, can be used as the switching element for the construction of precision analog switches. There are two identical n-p-n (in the 101KT1 IC) or p-n-p (in the 124KT1 IC) integrated circuit transistors in these choppers, which are made on a single chip (so that the transistors of these IC's have a common collector and contain four p-n junctions: two emitter-base junctions and two collector-base junctions). The integrated circuit transistors of the choppers have a high degree of identity of their characteristics, which assures a small mutual scatter in the remaining parameters (and in the absolute values of the parameters in the compensated switch circuit) as compared to discrete transistors. Both transistors of such an analog switch are in the same state, and for this reason, a small scatter in the parameters is assured by the opposing configuration of the two transistor circuits with respect to the residual voltage and current.

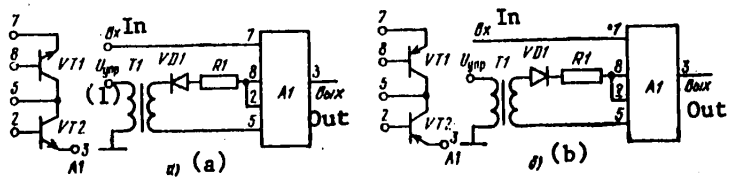


Figure 4.59. The 101KT1 (a) and 124KT1 (b) bipolar integrated circuit chopper.

The 101KT1 and 124KT1 integrated circuit choppers are made in a circular eight pin package, while the 162KT1 integrated circuit chopper, which is similar to the 124KT1 chopper in terms of its parameters, is produced in a flat pack. The main parameters of the 101KT1 and 124KT1 integrated circuits are given in Table 4.9. The electrical schematics of the application of bipolar integrated circuit choppers are shown in Figure 4.59. Here IC's inserted in parallel, series and parallel-series switch configurations are used as single switches.

The given IC's can also operate in structurally compensated switching circuits, where an improvement in the characteristics is achieved by virtue of the special configuration of the signal source and load.

The major difficulty in the application of the switch components treated above using parametric compensation consists in the fact that the control circuitry is

TABLE 4.9. Maximum Values of the Main Electrical Parameters of Various Types of Analog Switches

Parameters	101KT1A	124KT1A	273KT1	143KT1	190KT1	190KT2	168KT2
Resistance of the switch when "turned on", ohms	-	-	100	100	500	50	100
Switch leakage current when "switched off", nA	-	-	100	20	100	50	20
Turn-on delay time, μsec	0.03	-	1	2.0	-	-	0.3
Turn-off delay time, μsec	0.4	-	5	1.6	-	-	-
Resistance between emitters, ohms	100	100	-	-	-	-	-
Leakage current between emitters, nA	10	45	-	-	-	-	-
Residual voltage between emitters, microvolts	50	100	-	-	-	-	-
Number of channels	1	1	1	2	5	4	4

complicated, where this circuit should be isolated from the signal source and the load.

The hybrid 273KT1 integrated circuit can serve as an example of a medium speed switch with an isolated control circuit. The switch control circuitry uses a transformer here. The parameters of the 273KT1 integrated circuit are given in Table 4.9, while its electrical schematic and recommended circuit configuration are shown in Figure 4.60. A signal supplied from standard TTL integrated circuits is suitable for the control of the circuit.

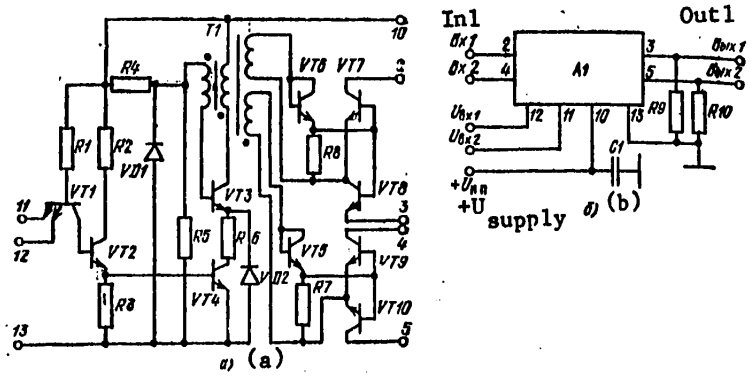


Figure 4.60. The 2731KT analog switch.

a. Basic schematic; b. Circuit configuration.

Analog switches using field-effect transistors have become quite widespread at the present time. Field-effect transistors with a controlling p-n junction are voltage switched and do not consume any control current. These devices are suitable for switching both currents and voltages, since they are galvanically decoupled from the control and signal circuits.

Field-effect transistor switches are controlled by voltages having an amplitude of 10 volts. The output signal levels from standard TTL circuits have a range of 0.3 to 3 volts. For this reason, to realize a switch circuit, it is necessary in the majority of cases to use level interface circuitry. In the switch using field-effect transistors, equipped with a control circuit and incorporated in the 284KN1 integrated circuit (Figure 4.61), the analog switching circuit is designed as a T-section switch, which takes the form of a combination of series-parallel and series switches; in this case, the series switches and the parallel switch operate out-of-phase.

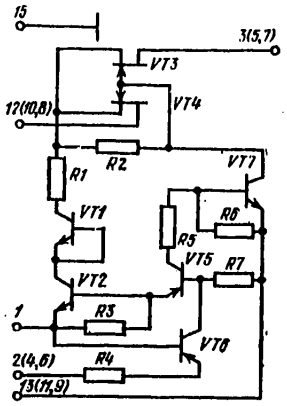


Figure 4.61. Basic electrical schematic of the 284KN1 switch.

When the series switches are turned on, the parallel switch does not influence the circuit operation because of the fact that its resistance is high as compared to the resistance of the turned-on switches. After the transistors of the series switches are cut off, the parallel switch transistor turns on, shunting the parasitic signal circuit with a low resistance, where this circuit is due to the influence of the interelectrode capacitances of the series switch and the resistance of the cut-off switch. In this case, a considerably attenuated signal acts on the next switch. Because of this, T-section switches can operate at a high switching frequency (with low noise). A drawback to such a switch is the large value of the resistance when turned on. However, this resistance does not depend on the magnitude and polarity of the voltage being switched.

MOS transistors (metal-oxide-semiconductor) are of the greatest interest for applications as analog switches. This is explained primarily by the high value of the input impedance of the device (up to 10^{15} ohms) for a signal of any polarity, something which assures good isolation between the controlling and switched circuits. Moreover, the fabrication technology for MOS devices is much simpler than the technology for bipolar transistors and field-effect transistors with a controlling p-n junction, while the MOS structures themselves are suitable for an increased level of integration.

Enriched p-channel MOS devices (the channel conductance rises with an increase in the gate-source voltage) are most frequently used in a semiconductor design.

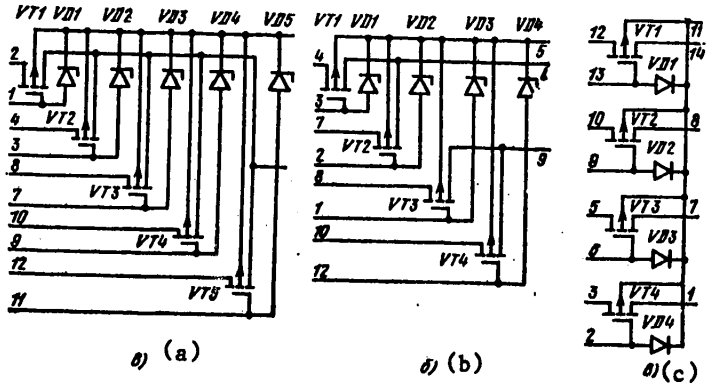
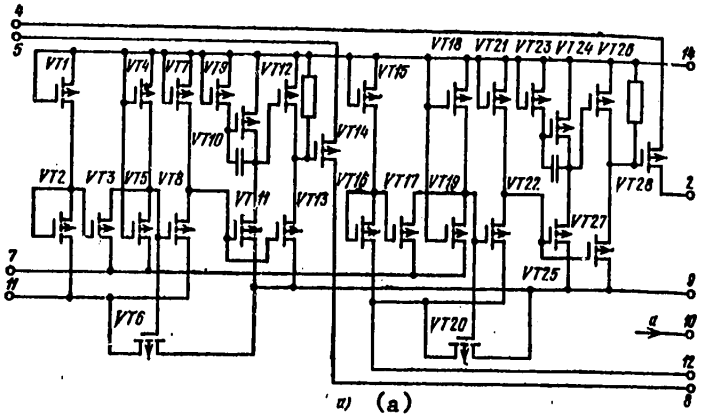


Figure 4.62. Basic electrical schematics of voltage switches.

a. The 190KT1 five-channel;
b. The 190KT2 dual two-channel;
c. The 168KT2 four-channel switch.



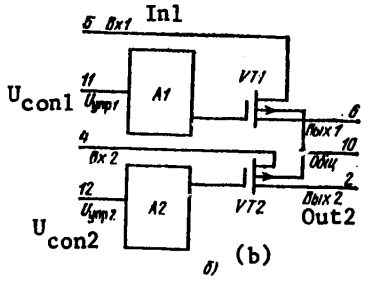


Figure 4.63. The 143KT1 dual channel MOS switch.

a. Basic electrical schematic;
b. Block diagram.

The 190 and 168 series IC's can serve as examples of integrated circuit switches and keyers using MOS transistors. There are two IC's included in the 190 series: the 190KT1 five-channel voltage switch (Figure 4.62a) and the dual two-channel 190KT2 switch (Figure 4.62b). These IC's make it possible to switch voltages of

up to 25 volts. The control signal amplitude may exceed 6 volts. The 168KT2 four-channel switch (Figure 4.62c) switches a voltage of up to 25 volts at a switching frequency of up to 1 MHz. The design of circuits where TTL integrated circuits are used in conjunction with the 190 and 168 series IC's is complicated because of the incompatibility of the output signals of these digital IC's with the input control levels for the p-channel MOS switches.

This drawback is eliminated in the 143KT1 two-channel MOS switch (Figure 4.63), in which the channel consists of the switch and the controller. The parameters of this switch are given in Table 4.9. The 143KT1 IC controller contains a circuit for matching the output TTL IC levels to the input levels for the MOS transistors as well as a logic amplifier with a push-pull output to provide for rapid charging and discharging of the input capacitance of the MOS switch.

4.8. Integrated Circuit Voltage Regulators

High precision in radioelectronic equipment is assured by the stability of the transfer functions of all of the equipment sections, which in turn are dependent on the stability of the supply voltages. Voltage regulators are used to obtain the requisite power supply conditions [28].

An integrated circuit regulator has the following main parameters. The voltage instability ratio is measured as the ratio of the change in the output voltage $\Delta U_{out\ 1}$ to the change in the input voltage which causes it. It is expressed in %/volt.

$$K_{ins\ U} = \Delta U_{out} 100\% / U_{out} \Delta U_{in}.$$

The current instability factor is measured as the ratio of the change in the output voltage, ΔU_{out}, to the relative change in the load current which causes it and is expressed in %:

$$K_{ins\ I} = \Delta U_{out\ U} \cdot I_{out} 100\% / U_{out} \cdot \Delta I_{out}.$$

The ripple smoothing factor is measured as the ratio of the amplitude value of the input voltage ripple ΔU_{in} to the amplitude value of the output voltage ripple. This factor is most often expressed in decibels:

$$K_{smooth} = 20 \log (\Delta U_{in} / \Delta U_{out}) \text{ [dB]}.$$

Moreover, to design the circuit configuration for integrated circuit regulators, it is necessary to know the power level dissipated by the device, P_{dis}, the maximum input $U_{in\ max}$ and the range of voltages to be regulated ΔU_{out}.

An important characteristic of a regulator is its speed, corresponding to the speed with which it handles jumps in the input voltage and load currents. Integrated circuit technology makes it possible to create various regulating devices [2]: from the simplest parametric regulators, for which one of the junctions of an integrated circuit transistor is used, up to complex compensation type regulators (Figure 4.64).

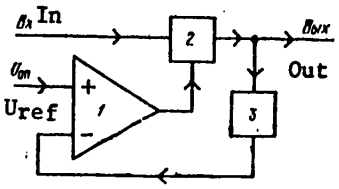


Figure 4.64. Block diagram of a compensation type regulator.

Key: 1. Error amplifier;
2. Regulating element;
3. Divider.

An error amplifier (usually one of the types of operational or differential amplifiers with a gain of about 1,000) amplifies the potential difference between a reference source and a center tap of a divider. The voltage divider and regulating element are inserted in a negative feedback circuit for this amplifier. Because of the fact that the gain is high, one can assume that the voltage at the regulator output is proportional to the transmission gain of the divider and the reference voltage level:

$$U_{out} = U_{ref}(R_1 + R_2)/R_2$$

where U_{ref} is the reference source voltage.

One of the types of zener diodes or a circuit based on current generators [2] is used as the element generating the reference voltage. The circuit which is depicted in Figure 4.64 operates as follows. An increase in the input voltage by the amount ΔU_{in} should cause an increase in the output voltage of the regulator by the amount ΔU_{out}. But the output signal increment is fed through a divider which attenuates it by a factor of $R_2/(R_2 + R_1)$, to the input of the error amplifier. The amplifier should generate a signal for reducing the current through the regulating element and thereby substantially compensate for the anticipated error at the output ΔU_{out}.

The regulating element can consist of one or more transistors, connected in a Darlington configuration. The number of transistors depends on the load current, the output power of the amplifier and the quality of the transistors themselves. As a rule, transistors are not connected to an integrated circuit regulator in the case of low load currents. With load currents of 1 to 5 A, it is necessary to connect two to three power control transistors to the IC. At the present time, several series of integrated circuit regulators are being produced, both semiconductor and hybrid, the electrical characteristics of which are summarized in Table 4.10.

The 275 series of hybrid integrated circuit regulators are a set of IC's with fixed output voltages, ranging from 1 to 24 volts. There are negative voltage regulators in this series. The use of temperature compensated internal feedback dividers is to be noted as a special feature of the 275 series of regulators. Such an approach makes it possible to reduce the impact of the ambient temperature on circuit operation, but at the same time reduces the applications flexibility of the device. In order to be able to make some adjustments, the center tap of the divider is brought out from the regulator circuitry.

The 275YeN1-6A,B positive voltage regulators (Figure 4.65) differ from one another in the nominal values of the divider resistors R11, R12 and R13. The

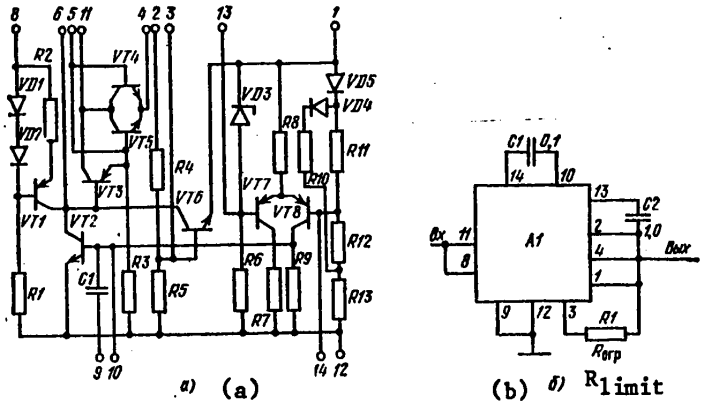


Figure 4.65. The 275YeN1-6A,B positive voltage regulators.

a. Basic electrical schematic;
b. Main circuit configuration.

regulating element in this circuit consists of matching transistor VT3 and transistors VT4 and VT5 which are connected in parallel. The error amplifier is designed around a differential stage (transistors VT7 and VT8) and a matching transistor VT2. The operating current of transistor VT1 is determined by the bias produced by means of diode string VD1 and VD2, as well as resistors R1 and R2. Transistor VT1 plays the part of an active load for the amplifying transistor. The built-in voltage divider is provided with a temperature stabilization network (diodes VD4 and VD5, as well as resistors R10 and R13). Resistor R3 serves for the leakage of the collector-base currents of the parallel transistor pair VT4 and VT5. The regulator circuitry includes a protection circuit, designed around transistor VT6, and resistive divider R4 and R5. The protective circuit operates with an external resistor R_{lim}. Capacitor C1 is intended for eliminating self-excitation of the regulator. The output voltage can be adjusted by varying the resistance of the internal divider by means of external resistors, which can be connected to pin 14.

To protect the IC output against excessive current when its load is short circuited, pins are provided for the connection of the limiting resistor R_{lim}. The load current, in passing through resistor R_{lim}, produces a voltage drop across it which is applied between the base and the emitter of transistor VT6. The load current increases until the voltage drop across resistor R_{lim} (about 0.7 volts) turns on transistor VT6, which limits the base current rise in transistor VT3. Thus, the rise of the emitter current of the regulating element is stopped (i.e., the output current of the integrated circuit). The nominal value of R_{lim} depends on the level of the permissible load current and is determined from the formula:

$$R_{lim} = U_{be}/I_{load/per} \approx 0.7\ V/I_{load/per} \approx 0.7(U_{in} - U_{out})/(P_{diss.per} \cdot 1.3),$$

where $P_{diss.per}$ is the permissible power dissipation of the regulator.

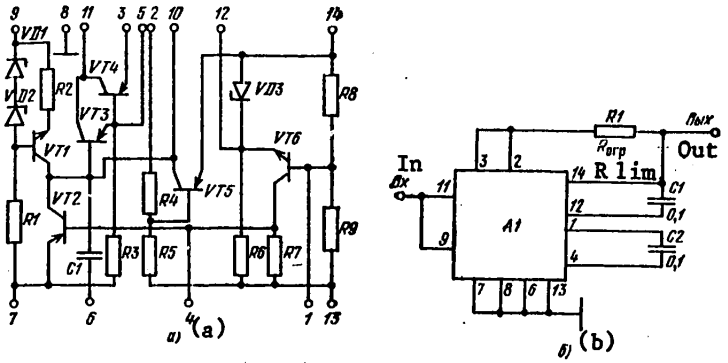


Figure 4.66. The 275YeN11A,B voltage regulator.

a. Basic electrical schematic;
b. Main circuit configuration.

In contrast to the circuit depicted in Figure 4.65a, in the circuit of the 275YeN11A,B regulator with an output voltage of +12 V (Figure 4.66), the mismatch signal is amplified by a two stage circuit (transistors VT6 and VT2). The voltage at the emitter of transistor VT6 (the reference level) is clamped by zener diode VD3 and the control signal is fed to the base of this transistor.

The 275YeN7A,B (Figure 4.67) negative voltage regulators (U_{out} = -6 volts) are similar in terms of their structure to the circuit shown in Figure 4.66a. However, the active elements are of the other type of polarity, and the regulating element (transistors VT3 and VT4) are designed in a Darlington configuration. The 275YeN12A,B negative voltage regulator is shown in Figure 4.68, while the basic circuit configuration is similar to the circuit shown in Figure 4.67b.

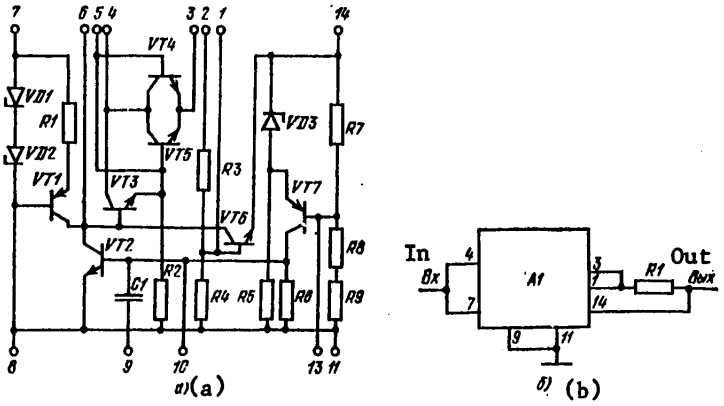


Figure 4.67. The 275YeN7 negative voltage regulator.

a. Basic electrical schematic;
b. Main circuit configuration.

Semiconductor regulators have significant advantages over hybrid ones, the active elements of which are discrete components. The merits of semiconductor regulators are expressed in the increased stability of the output voltage in a range of temperatures, with changes in the load and input voltage. This is obtained by virtue of the gain reserve and the thermal coupling which exists in semiconductor circuits.

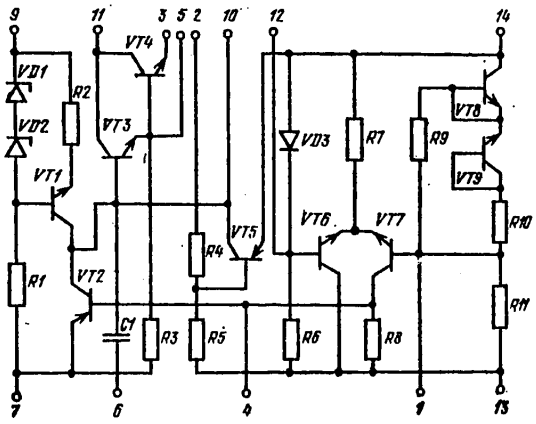


Figure 4.68. Basic electrical schematic of the 275YeN12A,B negative voltage regulator.

The 142 series of semiconductor IC's are compensation type regulators, which have a circuit for protecting against failure in the case of a load short circuit. An external divider is used in the 142 series regulators to adjust the output voltage. Such a circuit configuration makes it possible to extend the range of variable output voltages. A divider with a large division ratio degrades the value of the regulation factors, however, in a semiconductor circuit one can realize a gain reserve even with a large regulation range. For this reason, the temperature stabilization coefficient for the 142 IC series is no worse than for the IC's of the 275 series (Table 4.10).

The reference voltage supply circuit generates a reference voltage at a level of approximately 1.8 volts. Such an approach extends the control range of the output voltages of the IC in the low value range [26]. Moreover, the changes in the voltage across the emitter-base junction of transistor VT3 (-2.2 mV/°C) and the positive gradient of the voltage change across zener diode VD1 are compensated by means of diodes VD2, VD4 and the base-emitter junction of transistor VT2, which have a negative temperature coefficient of -2.2 mV/°C. A zero temperature coefficient can be obtained through the correct selection of the nominal values of divider resistors R1 and R2.

In the 142YeN1-2A,B voltage regulators (Figure 4.69), transistors VT6 and VT8 which are connected in a Darlington configuration, serve as the regulating element. The error amplifier is made as a differential stage (transistors VT3

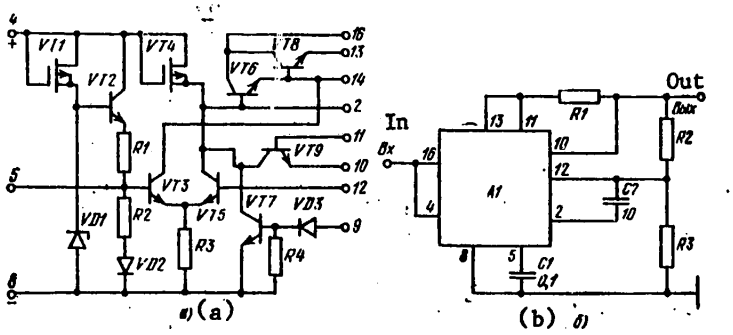


Figure 4.69. The 142YeN1-2A,B voltage regulator.

a. Basic electrical schematic;
b. Main circuit configuration.

and VT5), the loads for which are field-effect transistor VT4 and the base circuit of the regulating element. The differential amplifier is configured so that its full differential gain can be used.

Transistor VT9 performs the function of a regulator circuit protective element in the case of an output short-circuit. The input for the electrical turning off of the regulator or feeding control signals to it uses transistor VT7. In the normal mode, transistor VT7 is turned off. When a positive pulse is applied (for example, from a TTL switch), it turns on and cuts off the base current from transistor VT6, and the regulating transistor turns off.

The current sensor, resistor R1 (Figure 4.69b), is inserted in the circuit of the load current between the base and the emitter of transistor VT9 (Figure 4.29a). When the load current exceeds the set value, transistor VT9 turns on and shunts the regulating element. The nominal value of resistor R1 is chosen as a function of the maximum output current. Curves for the ripple smoothing factors K_{sm} for the 142YeN1A,B and 142YeN2A,B integrated circuits as a function of the ripple frequency of the power supplies and output voltages are shown in Figure 4.70a and b, while the switching and settling times are shown in Figure 4.70c and d as a function of the load capacitance.

The voltage traces of a regulator for the case of a pulsed change in the input voltage are shown in Figure 4.71a, while the traces for the case of a pulsed change in the output current are shown in Figure 4.72a. The curves for $t_1 = f(C_1)$; $t_2 = f(C_1)$; $(A_1/a) = f(C_1)$ and $(A_2/a) = f(C_1)$ for a change in U_{in} and I_{load} are shown in Figure 4.72b respectively. The given characteristics make it possible to estimate the speed of the regulators as a function of the nominal value of capacitor C1.

TABLE 4.10. The Parameters of the 142 and 275 Series Integrated Circuit Regulators

Тип ИС Type of IC	U_{out}, V $U_{вых}$, В	U_{in}, V $U_{вх}$, В	I, мА ном. Nom.	I, мА макс. Max.	$P_{рас.}$ при $T_{окр}$=25°С, Вт (1)	$K_{нU}$, %/В	$K_{нI}$, %	$\frac{TK\ U_{вых}}{\%/°C}$ (2)
142ЕН1 А/Б	3...12	9...20	50	150	0,8	0,3 / 0,1	0,5 / 0,2	0,01
142ЕН2 А/Б	12...30	15...40	50	150	0,8	0,3 / 0,1	0,5 / 0,2	0,01
275ЕН1 А/Б	1,2±10%	6...9	30	50	0,5	0,07	0,25	0,04 / 0,06
275ЕН2 А/Б	2,4±10%	7...12	20	50	0,5	0,09	0,25	0,04 / 0,06
275ЕН3 А/Б	3,0±10%	7,5...12	20	50	0,5	0,19	0,25	0,04 / 0,06
275ЕН4 А/Б	4,0±10%	8,5...12	20	50	0,5	0,1	0,25	0,02 / 0,04
275ЕН5 А/Б	5,0±10%	9,5...14	20	50	0,5	0,12	0,15	0,02 / 0,03
275ЕН6 А/Б	6,0±10%	10,5...15	20	50	0,5	0,12	0,15	0,02 / 0,03
275ЕН7 А/Б	−6,0±10%	10,5...15	20	50	0,5	0,12	0,15	0,02 / 0,03
275ЕН8 А/Б	6,3±10%	10,5,,,15	20	50	0,5	0,12	0,15	0,02 / 0,03
275ЕН9 А/Б	−6,3±10%	10,5...15	20	50	0,5	0,12	0,15	0,02 / 0,03
275ЕН10 А/Б	9,0±10%	13,5...19	20	50	0,5	0,15	0,1	0,01 / 0,02
275ЕН11 А/Б	12,0±10%	16,5...24	15	50	0,5	0,2	0,1	0,01 / 0,02
275ЕН12 А/Б	−12,0±10%	16,5...24	15	50	0,5	0,2	0,1	0,01 / 0,02
275ЕН13 А/Б	12,6±10%	17...24	15	50	0,5	0,2	0,1	0,01 / 0,02
275ЕН14 А/Б	−12,6±10%	17...24	15	50	0,5	0,2	0,1	0,01 / 0,02
275ЕН15 А/Б	−15,0±10%	19,5...20	15	50	0,5	0,22	0,1	0,01 / 0,02
275ЕН16 А/Б	24,0±10%	28,5...40	6	35	0,5	0,32	0,1	0,01 / 0,02

Key: 1. Power dissipation at 25° C, watts;
2. Temperature coefficient, U_{out}, %/°C.

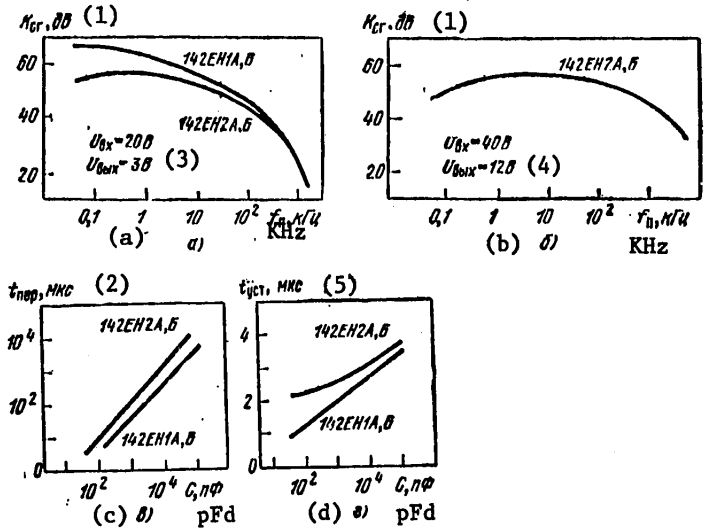


Figure 4.70. The ripple smoothing factor of regulators plotted for the 142YeN1 and 142YeN2 integrated circuits as a function of the supply ripple frequency (a and b) and the switching time [2] and settling time [5] as a function of the load capacitance (c and d).

Key: 1. Ripple smoothing factor, dB;
2. Switching time in microseconds;
3. U_{in} = 20 volts, U_{out} = 3 volts;
4. U_{in} = 40 volts, U_{out} = 12 volts;
5. Settling time in microseconds.

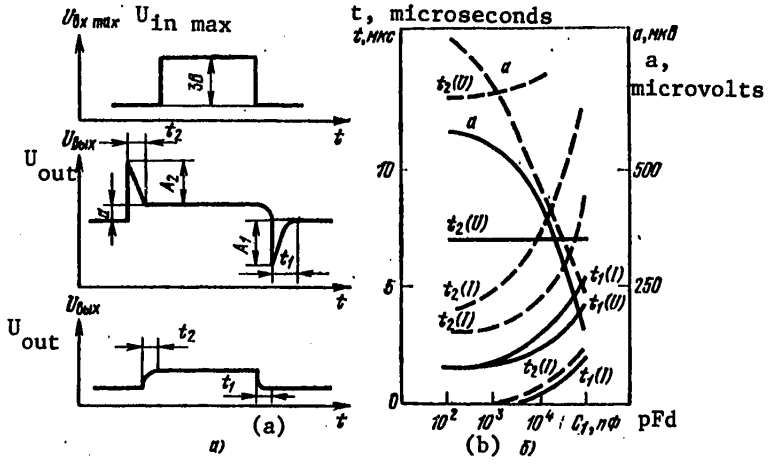


Figure 4.71. The change in the input voltage: a. Traces of the voltages and currents;

Key to Figure 4.71. [cont.]: b. The time constants for the 142YeN1-A,B (solid curves) and 142YeN2-A,B (dashed curves) integrated circuits.

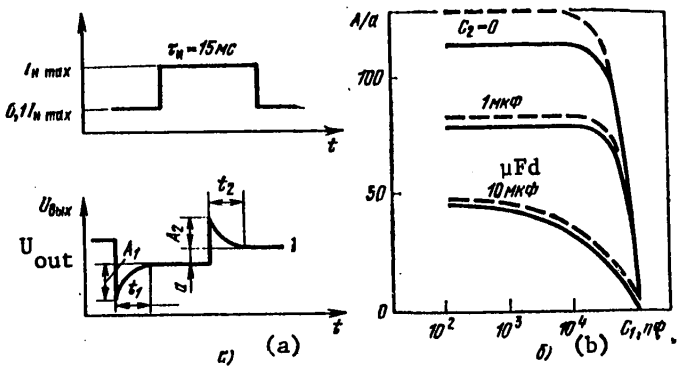


Figure 4.72. The change in the output current:

a. Traces of the voltages and currents;
b. The time constants as a function of the load capacitance for A_1/a (solid curves) and A_2/a (dashed curves).

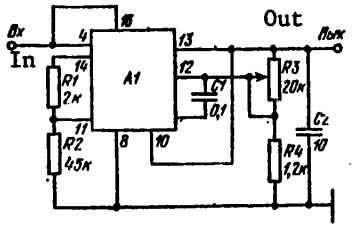


Figure 4.73. Modified circuit of a 142YeN1-2A,B integrated circuit voltage regulator with a short circuit protection circuit made using an external divider.

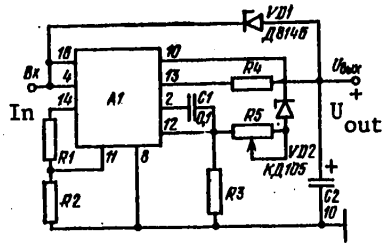


Figure 4.74. Schematic of a regulator with improved output characteristics.

Protection against a load short-circuit is accomplished by means of a divider (resistors R1 and R2 which control the base voltage of transistor VT9) (Figure 4.69a) in the voltage regulator based on the 142YeN1-2A,B integrated circuit (Figure 4.73). Such a circuit makes it possible to increase the speed of the short circuit protection circuitry. In this case, the nominal value of resistor R_{1im} can be computed from the equation: $R_{1im} \approx 0.5\ V/I_{out\ max}$, where $I_{out\ max}$ is the maximum value of the output current.

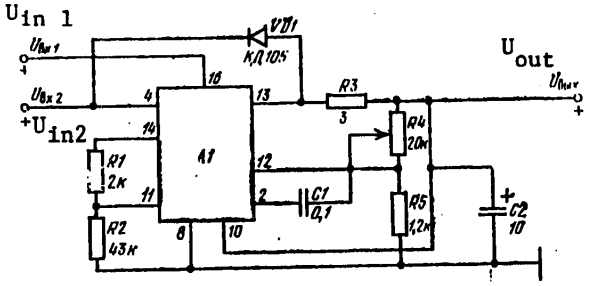


Figure 4.75. Schematic of a regulator with a reference voltage source powered from an external regulated voltage supply.

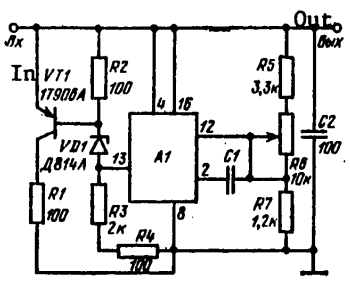


Figure 4.76. Schematic of a parallel voltage regulator.

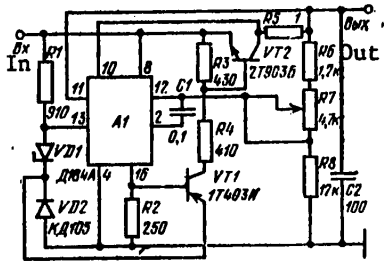


Figure 4.77. Schematic of a negative voltage regulator.

The characteristics of regulators can be changed by incorporating several discrete components in the circuitry. An improvement in the values of the coefficients $K_{load\ U}$ and $K_{load\ I}$ is achieved in the regulator circuit shown in Figure 4.74 by inserting elements VD2 and R_4 in place of the output resistive divider. In this circuit, the change in the output voltage ΔU_{out} is fed to the input of the error amplifier (pin 12) through the zener diode. The output voltage of the regulator is:

$$U_{out} = U_{VD2} + U_{ref}, \qquad U_{вых} = U_{VD2} + U_{оп},$$

where U_{VD2} is the zener diode voltage and U_{ref} is the internal reference source voltage. Diode VD1 is incorporated in the circuit to protect the regulator at the moment the input voltage is disconnected (the voltage across capacitor C2 can prove to be excessive). The average value of the relative instability of the output voltage in this circuit with a change in the input voltage of 1 volt amounts to 0.01%/volt, and with a change in the output current of from 5 to 50 mA, is equal to 0.03%.

An improvement in the relative instability is achieved in the circuit of the regulator shown in Figure 4.75 in that the reference voltage circuit is supplied from an external regulated voltage source, for which a second regulator designed

using the same circuit made be used. The condition $U_{in1} \geq U_{in2}$ should be satisfied for the given circuit.

A special feature of the parallel regulator circuit of Figure 4.76 consists in the fact that the current consumed by the IC from the input voltage source remains constant with a change in the output current. The circuit operates so that with an increase in the current, the output voltage increases by a certain amount and is fed to the input of the error amplifier (pin 12), which in turn leads to an increase in the current in the regulating element of the IC, in parallel with which a network is connected which consists of zener diode VD1 and the emitter-base junction of transistor VT1. The total current of diode VD1 and the regulating element of the IC flows through resistor R2. A change in the current of the regulating element entails a reduction in the diode current of VD1 and a decrease in the base and collector current of transistor VT1. Consequently, the changes in the load current and collector current have different signs.

A negative voltage regulator can be constructed using the 142YeN1-2A,B regulators (Figure 4.77). Just as in the preceding case, the 142EN1-2A,B integrated circuit is inserted in parallel with the load and transistor VT2 plays the part of a damping resistor, the dynamic resistance of which changes as a function of the load current. The regulating element of the IC operates as an amplifier having R2 as a load. With a change in the load current, the output voltage changes by the amount ΔU_{out}, which is fed through divider R6, R7 and R8 to the input of the error amplifier, and upon being amplified, appears across resistor R2. Transistor VT1 amplifies this voltage and controls transistor VT2 (i.e., the load current). The current in transistor VT2 changes so that the change in the voltage in the load is compensated. A bias voltage is produced by means of diode VD2 for transistor VT2. The resistor serves to produce the requisite working current for diodes VD1 and VD2.

The minimum output voltage level of the regulator is limited by the reference supply voltage. In order to extend the output voltage range, one must use the circuit shown in Figure 4.78. This regulator is designed around two integrated circuits, which operate from unregulated power supplies with different polarities. The circuit provides for output voltage regulation from zero up. One IC serves to regulate the voltage across the load, while the other serves to feed bias to the common lead in the first circuit. The amount of bias is equal to the internal reference voltage of the IC or exceeds it.

In many devices, a regulator is needed having a bipolar output voltage (for example, to power circuits using operational amplifiers). For these purposes, one can employ the circuit shown in Figure 4.79. The circuit consists of two regulators for different polarities, designed around the 140YeN1-2A,B integrated circuits, which are connected together. The negative voltage regulator circuit is similar to the circuit shown in Figure 4.77. The output current of the regulator is limited by the power dissipation of the IC, but it can be increased if an additional power transistor is introduced into the circuit.

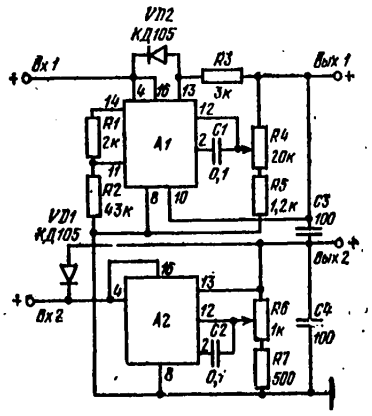


Figure 4.78. Schematic of a voltage regulator with an expanded output voltage range.

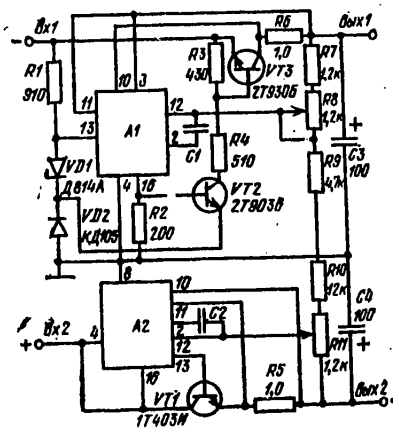


Figure 4.79. A regulator with a bipolar output voltage.

The circuit of a regulator with an increased output current is shown in Figure 4.80. The maximum output current level can be determined from the equation:

$$I_{out\ max} = I_{out} h_{21e}, \qquad I_{вых\ max} = I_{вых} h_{21э},$$

where I_{out} is the regulator output current and h_{21e} is the current gain of transistor VT1. It is frequently necessary to produce a regulated voltage which exceeds the maximum permissible input voltage for the IC. One must also use several additional outboard components in this case. A circuit is shown in Figure 4.81 in which the increase in the output voltage range is set by feeding a positive bias to the common lead of the IC (pin 8). This positive bias is provided by zener diode VD2. The regulated output voltage for the given circuit is determined as follows:

$$U_{out} = U_{ref}(R_1 + R_2)/R_1 + U_{VD2}$$

where U_{VD2} is the breakdown voltage of zener diode VD2. In this case, one must make sure that $I_{VD2} \geq I_{VD2\ min}$ (here, $I_{VD2\ min}$ is the minimum breakdown current of zener diode VD2). Keyed type voltage regulators (Figure 4.82) are used to increase the efficiency of regulators operating at elevated output currents (especially if the voltage drop across the regulating element is great). Transistor VT1 operates as a switch (either saturated or cut-off). When it is turned on, diode VD1 is cut off and the current in the inductance coil L1 increases:

$$I_L = \frac{1}{L}\int_{t_0}^{t_1} U dt.$$

Here, U is the voltage applied to the inductance.

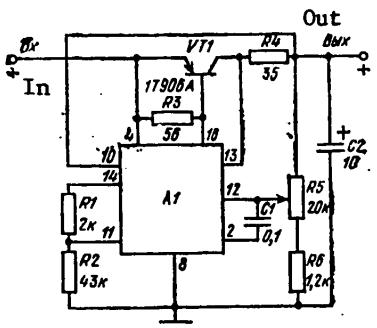


Figure 4.80. A regulator with an increased output current.

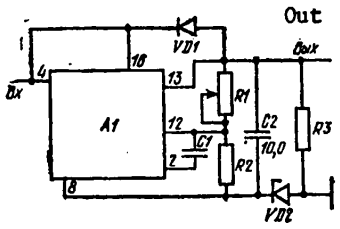


Figure 4.81. A regulator with an increased input and output voltage.

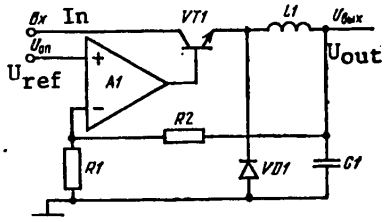


Figure 4.82. A keying type regulator.

The current through inductance coil L1 charges capacitor C1, which is connected to the inverting input, and feeds the current to the load. The output voltage increases until (capacitor C1 is charging) the reference voltage is exceeded at the noninverting input of the error amplifier. At this point in time, the error amplifier cuts off the power to the base of transistor VT1 and the unregulated input voltage is cut off. The energy stored in inductance coil L1 serves as the reason for the appearance of the voltage pulse U_X, which is negative. This pulse is absorbed by turned on damping diode VD1. The current of the inductance I_L is delivered to the load.

When the current in the inductance coil falls below the load current level, capacitor C1 begins to discharge and the level of the output voltage (and consequently also the voltage at the inverting input of the error amplifier) falls off. When the voltage at the inverting input U_0 drops below the reference voltage, the amplifier triggers the transistor switch (transistor VT1) and the cycle repeats. The output voltage of a switched regulator fluctuates about the voltage $U_{out} = U_{ref} (R_2 + R_1)/R_2$ with an amplitude which is determined by the sensitivity of the error amplifier and the ratio of the nominal values of divider resistors R1 and R2.

The 142YeN1-2A,B integrated circuits are used in the circuit of the switched regulator (Figure 4.83) as the device which controls transistor switch VT1. The self-oscillating mode in this circuit is determined by the 142YeN1-2A,B IC, choke L1, capacitor C2 which is inserted in parallel with the load, diode VD3 and zener diode VD2. The use of p-n-p transistor VT1, which does not require an additional power supply to cut off the switch, simplifies the circuitry. The voltage across diode VD1 provides for cutting off the switch. The circuit has the following parameters: average value of the relative instability of the output voltage with a change in the input voltage by 1 volt: 0.05%/V; with a change in the output current from 10 to 500 mA: 0.1%.

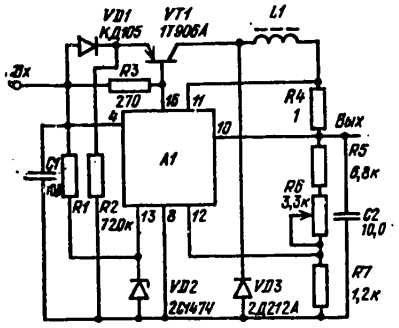


Figure 4.83. A keying regulator based on the 142YeN1 integrated circuit.

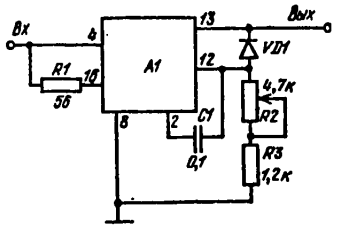


Figure 4.84. A threshold gate based on the 142YeN1-2A,B integrated circuit.

When designing a switched regulator, one must determine the values of L and C. The following regulator characteristics are specified for the calculation of L and C: the ripple level ΔU, the output voltage U_{out}, the frequency f and the maximum output current $I_{out\ max}$.

By solving equation (4.7) for the inductance L, and assuming $I_{out\ max} = 1.3\ I_L$, we obtain the value:

$$L = [1.3(U_{in} - U_{out})/I_{out\ max}f](U_{out}/U_{in}). \qquad (4.8)$$

As was shown earlier, regulator circuits have an internal amplifier with a gain of about 1,000 and an output current of up to 150 mA. Moreover, a regulator is suited for operation at high supply voltages (up to 40 volts), especially if it is equipped with a heat sink. The internal source provides a reference voltage which does not depend on temperature or power supply voltage changes. All of these factors make it possible to use the 142YeN1-2A,B regulators as either an amplifier or a threshold gate (Figure 4.84).

Its threshold voltage is the reference element voltage. The minimal output voltage of this device is governed by the load resistance, the internal load resistance and the internal reference voltage source resistance:

$$U_{out\ min} \approx (U_{ref} - 1)R_{load}/(R_{load} + R_1),$$

where $R_1 \approx R_1' \cdot R_2'/(R_1' + R_2')$, while resistors R1' and R2" [sic] comprise the reference source voltage divider. The maximum output voltage can be defined as:

$$U_{out\ max} = U_{supply} - U_{re}$$

where U_{re} is the minimum voltage drop across the regulating element.

Bibliography

1. Gram, "Proyektirovaniye i primeneniye operatsionnykh usiliteley" ["Design and Applications of Operational Amplifiers"], Moscow, Energiya Publishers, 1974.

2. Shilo V.L., "Lineynyye integral'nyye skhemy v radioelektronnoy apparature" ["Linear Integrated Circuits in Radioelectronic Equipment"], Moscow, Sovetskoye Radio Publishers, 1974.

3. Marshe Zh., "Operatsionnyye usiliteli i ikh primeneniye" ["Operational Amplifiers and Their Applications"], Moscow, Energiya Publishers, 1974.

4. Gutnikov V.S., "Primeneniye operatsionnykh usiliteley v izmeritel'noy tekhnike" ["The Applications of Operational Amplifiers to Instrumentation Equipment"], Moscow, Energiya Publishers, 1975.

5. Polonnikov D.Ye., "Reshayushchiye usiliteli" ["Resolver Amplifiers"], Moscow, Energiya Publishers, 1973.

6. Akmentyn'sh Ya.Ya., Zheyvome O.G., et al., "Integral'nyy operatsionnyy usilitel' s ponizhennoy potreblyayemoy moshchnost'yu" ["An Integrated Circuit Operational Amplifiers with Reduced Power Consumption"], ELEKTRONNAYA PROMYSHLENNOST' [ELECTRONICS INDUSTRY], 1975, No 11, p 35.

7. Aleksenko A.G., Didenko V.I., Lebedev A.A., "Chuvstvitel'nyye integral'nyye komparatory" ["Sensitive Integrated Circuit Comparators"], "Mikroelektronika", Edited by A.A. Vasenkov, Moscow, Sov. Radio Publishers, 1973, Issue 6, pp 190-201.

8. Lebedev A.A., "Ispol'zovaniye vzaimnykh komponentov i blokov dlya povysheniya bystrodeystviya integral'nykh komparatorov napryazheniya" ["The Use of Complementary Components and Units to Increase the Speed of Integrated Circuit Voltage Comparators"], ELEKTRONNAYA PROMYSHLENNOST', 1975, No. 11, p 20.

9. Akmentyn'sh Ya.Ya., Vartin' V.R., Matavkin V.V., Shenin' A.E., "Komparator napryazheniya 521SA1" ["The 521SA1 Voltage Comparator"], ELEKTRONNAYA PROMYSHLENNOST', 1974, No. 4.

10. Akmentyn'sh Ya.Ya., Vartin' V.R., Matavkin V.V., Shenin' A.E., "Komparator napryazheniya 521SA2" ["The 521SA2 Voltage Comparator"], ELEKTRONNAYA PROMYSHLENNOST', 1974, No 10.

11. Kerekesner I.P., Rysin V.S., Timonteyev V.N., Tkachenko V.A., "Analogovyy umnozhitel' tipa 140MA1" ["The 140MA1 Analog Multiplier"], ELEKTRONNAYA PROMYSHLENNOST', 1974, No. 4.

12. "Spravochnik po vysshey matematike" ["Reference Book on Higher Mathematics"], Edited by M.Ya. Vygodskiy, Moscow, Nauka Publishers, 1970.

13. Renschler E., "A New Basic Building Block Linear Four-Quadrant Multiplier", in Proceedings of the IEEE Linear IC Clinic, New York City, March 24, 1969.

14. "Application Data. Data Book", Motorola Company, 1969, MC 1496.

15. Khokhlov B.N.,"Dekodiruyushcheye ustroystvo tsvetnykh televizionnykh priyemnikov" ["A Decoder for Color TV Receivers"], Moscow, Svyaz' Publishers, 1973.

16. Sukhov N.N., Oldin A.F., Chistov V.M., "Primeneniye IS serii 224 v televizore tsvetnogo izobrazheniya" ["The Applications of the Series 224 Integrated Circuits in Color TV Receivers"], Moscow, Sovetskoye Radio Publishers, 1976, (The Series "Elementy radioapparatury" ["Radio Equipment Components"]).

17. Malyshev I.V., Tubeyev F.Ya., Arakelyan S.G., Kravchuk I.F., "Poluprovodnikovyye IS dlya priyemo-usilitel'nykh traktov radioapparatury" ["Semiconductor IC's for the Receiving and Amplifying Sections of Radio Equipment"], ZARUBEZH. ELEKTRON. TEKHNIKA [FOREIGN ELECTRONICS ENGINEERING], 1976, No. 18.

18. Zubachev S.G., Chaykin I.P., "Moshchnyy usilitel' nizkoy chastoty" ["High Power Low Frequency Amplifier"], ELEKTRONNAYA PROMYSHLENNOST', 1974, No .0, p 38.

19. Shakhgil'dyan V.V., Lyakhovkin A.A., "Fazovaya avtopodstroyka chastoty" ["Phase Locked Loop Frequency Control"], Moscow, Svyaz' Publishers, 1966.

20. Smirnov B.N., Trayto B.G., Trofimov M.M., "Integral'nyye skhemy giratornogo usilitelya" ["Gyrator Amplifier Integrated Circuits"], ELEKTRONNAYA PROMYSHLENNOST', 1973, No. 10, p 33.

21. "Spravochnik po tsifrovoy vychislitel'noy tekhnike" ["Digital Computer Engineering Handbook"], B.N. Malinovskiy, V.A. Aleksandrov, V.P. Bogan, Ye.N. Briokhovich et al., Kiev, Tekhnika Publishers, 1974.

22. Smolov V.B., Fomichev V.S., "Analogo-tsifrovyye i tsifro-analogovyye nelineynyye ustroystva" ["Analog-Digital and Digital-Analog Nonlinear Devices"], Leningrad, Energiya Publishers, 1974.

23. Zhulla R.N., Kenyausis A.M., Martsinkyavichus A.K., et al., "Analogovyye gibridnyye integral'nyye skhemy serii 240" ["The 240 Series of Analog Hybrid Integrated Circuits"], ELEKTRONNAYA PROMYSHLENNOST', 1975, No 8, p 50.

24. Nikolayevskiy I.F., Igumnov D.V., "Parametry i predel'nyye rezhimy raboty tranzistorov" ["Parameters and Ultimate Operating Modes of Transistors"], Moscow, Sov. Radio Publishers, 1971.

25. Stepanenko I.P., "Osnovy teorii tranzistorov i tranzistornykh skhem" ["Fundamentals of Transistor and Transistor Circuit Theory"], Moscow, Energiya Publishers, 1967.

26. Dodik S.D., "Poluprovodnikovyye stabilizatory postoyannogo napryazheniya i toka" ["Semiconductor DC Current and Voltage Regulators"], Moscow, Sovetskoye Radio Publishers, 1962.

CHAPTER 5. PROVIDING RELIABILITY OF IC [Integrated Circuits] IN THE PRODUCTION AND ASSEMBLY APPARATUS

5.1. Design-Technological Principles of High Reliability

High reliability of semiconductor IC is one of main reasons they became the basis of modern radioelectronic apparatus. The high reliability of IC is insured by the group method of producing IC elements, by a smaller number of interelement connections and the lower level of power consumed.

In the group production method, all IC elements are manufactured in one technological cycle under rigidly controlled conditions, and with a minimum use of manual labor. The physio-chemical compatibility of materials and processes provide equal reliability of all IC elements. The reliability of the functional device, assembled with discrete parts, depends on the quality of the complementing electric-radio elements (ERE) which are manufactured at many enterprises at different times on dissimilar equipment. The connections between the contact pads on the semiconductor IC chip are made by thermocompression (or ultrasonic) welding. Vacuum spraying of metal and thermocompression welding provide a reliable connection of the elements. If we compare a usual unit and an integrated circuit containing a thousand equivalent ERE, then in integrated circuits, the number of interconnections by the "usual" method is reduced to 1-100th-1/150th. As a result, the reliability of the apparatus is increased because the number of the most probable sources of failures -- interelement connections -- is reduced considerably, moreover, they are made by the most perfect methods.

A number of IC types are characterized by low power consumption. With low dissipation power, the operating temperature of a chip increases little compared to the ambient temperature and, therefore, conditions are favorable for retardation of the physio-chemical processes leading to failures.

The actual reliability of IC as the property to implement given functions and to preserve its parameters within given limits with time, determined by the operating conditions, depends on many factors: the perfection of the circuit, the quality of the initial materials and the complementing components, and the quality and stability of the technological process of IC manufacture.

In IC production, monitoring operations are carried out not only at the end of the final stage of manufacture, but are converted to a quality control operation over the entire technological process. However, the technological process control is clearly insufficient because in the IC manufacturing process, not only are operator errors possible but also random deviations, related to the quality of the materials and working equipment. Therefore, a single system of checks and rejections of the finished products is introduced in each technological process of semiconductor manufacture to detect IC with apparent as well as hidden defects if possible. For this purpose single norms and methods of boundary tests were established that make it possible to determine reserves of electrical and mechanical properties when developing new articles, and check the efficiency of these or other measures introduced in the technological process in series production of IC.

The true reliability of IC is determined only in operating the apparatus. First of all, it must be concluded that the reliability of IC in operating various series (made at various semiconductor plants) is practically the same in devices developed in one and the same apparatus enterprise. At the same time, the reliability of IC of one and the same series in apparatus, manufactured at various plants, is found to be very different. This is the result of differences in the technological standard of manufacture of the apparatus which can also be made in nonspecialized enterprises.

The use of highly reliable IC does not always automatically provide such reliable apparatus. The preservation of the reliability of IC in the apparatus is determined, to a considerable degree, by their proper use at all stages of development, production and operation. The proper use of IC here means the implementation of recommendations on electrical modes and assembling methods, a debugged technological process of manufacture of the apparatus and the use of measures to protect IC from static electricity, thermal and other effects. Achieving and maintain maximum operational reliability of IC (and consequently, the quality of the apparatus) depends greatly on the level of the processes of the design of the apparatus, its preparation for production and the tune-up of the equipment and the skill of the personnel.

The purpose of this chapter is to acquaint the reader with several measures taken to insure the reliability of integrated circuits, as well as to make the necessary recommendations on using IC when manufacturing the apparatus.

5.2 Operational Quality Control

To achieve a given level of IC quality in all production lots along with a thorough finishing off of the product design and the improvement of the technological process, a rigid operation by operation quality control is used in production. Due to this, an unsuitable product is rejected at certain stages of the production cycle. Moreover, constant quality control over the parameters of the technological process (for example, temperature, time intervals, gas consumption), technical condition of equipment, and a check of the skill of the operators is carried out.

Table 5.1 lists the basic stages of the technological processes, the monitored characteristics, and gives the criteria for evaluating the proper progress of the process. The number of monitoring stages, the volume and type of monitoring (continuous or selective) are determined in each concrete case depending upon the required level of reliability of the IC (standard or especially reliable), the type and importance of the stage of technological process.

The second stage of production quality control is establishing relationships between types of IC failures, the parameters of the technological process and developing recommendations to correct them. An analysis of causes for IC failures is objective information that makes it possible to improve the technological processes. Table 5.2 shows an example of the plan-schedule of measures directed toward the elimination of causes of failures of semiconductor IC. The data in Table 5.2 must be analyzed along with the figures, references to which are given in the table. These diagrams show the relative change in the share of IC failures of a certain type, depending upon the period of implementation of the measures. The measures in Table 5.2 are numbered for convenience of analysis. The effectiveness of the internal measures is illustrated in Table 5.3 where the dynamics of the reduction in IC failures for the three above-mentioned causes is shown.

5.3 Rejection Tests

IC manufacturers are interested in the best technological processes and strive to have thorough production quality control for the purpose of increasing the percentage of finished product yield, and reducing the rate of IC failures.

However, demands for reliable IC from the users cannot be satisfied only by improving the production process and the system of operation by operation quality control. A system of rejection tests of the finished product as a means of increasing the reliability of the product as compared to the level considered standard at the given moment plays a great role in solving such problems.

Rejection tests of IC are intended mainly for early detection of (preworking) failures, caused by operator error as well as by random deviations related to the quality of the initial materials and the operation of the equipment in the process of IC manufacture. The introduction of rejection tests for the entire product is based on the fact that the rate of IC failures, in the general case, decreases with time. Fig. 5.2 shows the characteristic distribution of IC failures in production and the tests of one of the samples of the apparatus. The greatest number of

failures (up to 80%) occurs at the stage of production and tests of small assembly units of the apparatus and decreases noticeably when these units are consolidated (curves 1, 2 and 3) as well as for the entire product (curve 4). With the rejection tests, it is possible to remove microcircuits from the production lot that have hidden defects and thus increase the reliability of the apparatus, "shifting" the failures of breaking in to the stage of rejection testing.

Table 5.4 shows an example of the composition and conditions of rejection tests to which 100% of the IC produced are subjected. As may be seen from Table 5.4, rejection tests are made in a logical sequence and are interdependent. Methods and modes are used for rejection tests that take into account the special features of the manufacturing technology and IC design. Here hidden IC defects are detected, but not failures that are not inherent in the given technology and design. The selection of methods and conditions of tests are based on the knowledge of the physical nature of the IC failures which originate at various kinds of climatic, mechanical and electrical effects. The levels of external effects are selected by the results of IC tests so that there remain certain stability reserves.

In setting up the sequence of carrying out the rejection tests, it proceeds on the basis that they must begin with such types of effects which will make it possible to eliminate immediately IC with hidden defects that cause the greatest percentage of failures in operation. At the final test stages, methods are used that will make it possible to eliminate poor IC whose defects were not detected in the previous tests from the production lots. Rejection tests include methods that facilitate the stabilization of electrical parameters and reduce the spread of their values.

The first rejection test is visual inspection after the operation of dividingthe wafers into chips and before the sealing operation. Experience shows that this type of inspection is one of the most important methods that makes it possible to detect many production defects which cannot always be detected electrically or in other types of tests.

Visual inspection makes it possible to reject IC in which the following violations were detected: defects of chip metal-coating (scratches and voids in metal-coated tracks and contact pads, signs of corrosion and flaking, unetched sections of metal coatings, shifting in the metal-coated layout), scribing defects (cracks in the active area of the circuit, under contact pads and metal coating, splits and damage to the chip) or diffusion defects (nonuniform and parasitic diffusion). In some places there may be no passivated protective oxide on a part of the p-n junction, shifts of layers in photolithography, and defects in the protective dielectric film may be seen (remnants of the dielectric film on contact pads, scratches and holes).

Insulation defects can be found in IC chips (absence of separating insulation, contamination of the surface of the chip), fixed or loose particles of foreign material on the chip's surface, defects of welded joints on the chip and housing leadouts, as well as defects of wire leadouts (the sag is greater or smaller than the norm; uneven flexibility of the wire, grooves, reduction in diameter; distance between wire leadouts that are less than the norm).

Table 5.1

Stages of the technological process and the approximate volume of operation by operation quality control, characteristic for IC production

Monitored characteristics	Evaluation criterion
Manufacturing of semiconductor wafers	
Thickness, plane-parallel, roughness	Percent of set value
Structure defects: linear, displacements, inclusions	Number per unit area
Surface orientation	Percent of average value
Specific resistance	Percent of set value
Equipment	Meeting technical condition requirements
Passivation (oxidation) of surface	
Equipment operation mode: change of temperature with time	Allowable deviation range
Velocity of gas flow up to the start and in the process of oxidation	Allowable deviation of gas flow velocity
Thickness of the raised (or precipitated) layer	Allowable deviation from norm
Density of microholes and cracks	Allowable number of defects per unit area
Size of microholes	Maximum allowable size of holes
Equipment	Meeting technical condition requirements
Photolithography	
Sizes, combination, quality of etching, microholes, presence of foreign particles	Meeting requirements of visual inspection
Properties of solvents; specific weight, viscosity, solid particle sediment, storage temperature	Correspondence to certificate
Modes of drying and exposing: temperature time	Allowable deviation from the norm
Exposition modes: intensity of light, time	
Adhesion quality	Force for peeling film
Modes of etching processes: density (frequency of etching sections), temperature, time (velocity of etching each level of passivation or metal coating).	Allowable deviations from the norm
Conditions for making each type of mask: relative humidity, temperature, dust in the environment; quality of surface (density and diameter of microholes, roughness of edges	Same Meeting requirements of visual inspection

Table 5.1 continued

Monitored characteristics	Evaluation criteria
Epitaxial build-up	
Conditions and storage time	Allowable deviation
Thickness of epitaxial layer	Percent of set value
Specific resistance	Same
Defects of packing, dislocation, holes, bulges, pits, depressions, scratches, irregular edges	Meets of requirements of visual inspection
Equipment mode: temperature of the epitaxial tube, composition and parameters of the gas flow	Allowable deviation
Diffusion	
Depth of diffusion junctions of emitter and base	Same
Specific resistance	Percent of set value
Equipment mode: temperature of diffusion tube, composition and parameters of the gas flow	Allowable deviation
Metal coating	
Purity of wafer, temperature of wafer and metal, film thickness (including along the edges of the contact windows) -- effect of shading	Meeting requirements of visual inspection and force for peeling the films
Scribing	
When scribing with a diamond cutter: slope angle, pressure, velocity and direction of cutter movement. When scribing by quantum optical oscillator beam: power and resolution capacity of beam; depth and width of scribing; mechanical damage; cracks, metal scaling, chips, scratches	Meeting requirements of visual inspection
Chip assembly	
Temperature, time, ultrasonic power, chip orientation, ambient parameters	Allowable deviations
Connection of internal leadouts	
Temperature, pressure, time for making connection, metal composition, rupture force, ambient parameters	Same

Table 5.2

Approximate plan-schedule of measures directed to the elimination of IC failures

Type of IC failure	Correcting measures	Period of introducing measures
1. Rupture of wire leadout due to failures of the thermocompression connection (see Fig. 5.1a)	1.1. Rejection of potentially unreliable IC by centrifuging	IV quarter of 1927
	1.2. Monitoring the rupture force of the gold wire	I quarter of 1973
	1.3. Monitoring the detachment force of the thermocompression connection	I quarter of 1973
	1.4. Change in the design of the welding tool (needle) to increase the detachment force of the thermocompression connection	
	1.5. Introduction of the technological operation of "dropping" an IC on an oaken board from a height of 1 meter	IV quarter of 1973
	1.6. Introduction of a process of continuous degreasing and annealing the gold wire	II quarter of 1975
2. Rupture of plating due to poor adhesion (Fig. 5.1b)	2.1 Introduction of a process for spraying on aluminum by an electron beam	IV quarter of 1972
	2.2. Introduction of group spraying on by electron beam from a water-cooled crucible	I quarter of 1974
3. Rupture of connection due to formation of intermetallic phases at the interface of dissimilar metals (see Fig. 5.1c)	3.1. Reduction in annealing temperature	IV quarter 1973
	3.2. Reduction of burn-in temperature of aluminum and replacing oxygen medium by nitrogen	IV quarter 1974
	3.3. Stabilization and monitoring the temperature of the tool and changing the heating mode in the process of setting the chip on the base	IV quarter 1974

Table 5.3

Dynamics of reducing IC failures

Type of failure	Share of IC failures of a certain type (% of all failures) by years			
	1972	1973	1974	1975
Rupture of wire leadout due to thermocompression connection defects	13.7	4.1	4.7	2.8
Rupture of plating due to poor adhesion	18.8	2.7	0	0
Rupture of connections due to the formation of intermediate phases at the interface of dissimilar materials	10.1	19.6	1.2	0

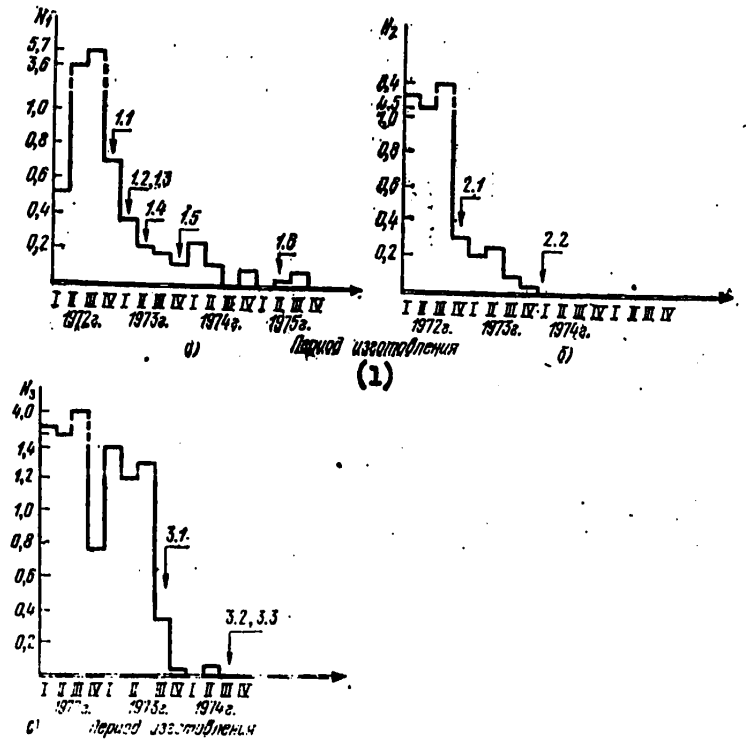


Fig. 5.1. Reduction in the number of IC failures (N) occurring for various reasons depending upon the use of correction measures: a -- break in thermopressure welding; b -- break in connections due to poor adhesion; c -- break in connections due to the presence of intermetallic phases. 1. Period of manufacturing.

Table 5.4

Rejection tests

Type	Conditions
Visual IC inspection before sealing	Inspection of chips under a microscope (not less than 80 magnification) to meet requirements on limiting the number of defects of each type and their total number, shown in specification
Annealing for parameter stabilization: before sealing	Hold IC at a temperature exceeding upper value in specification for 48 hours
After sealing	Hold IC at upper value of temperature for 24 hours
Cyclic temperature effect	Alternate effect of upper and lower values of ambient temperature (transfer from one chamber to another for not more than 3 minutes). Number of continuously following cycles - 5
Line loads	Effect of line loads with accelerations of 10,000... 20,000 g in the direction of the vertical IC axis for 1 minute
Seal check: small leaks	Check seal within $1x10^{-3}...1x10^{-7}$ liters. μ m/second by the mass-spectrometer method
Average leaks	Check IC seal, pressure-molded in Freon, in an indication liquid. Determine seal at $1x10^{-2}$ liters. μ m/second
Large leaks	Check seal in an indicator liquid
Measurement of electrical parameter	Monitor IC parameters according to specifications at normal temperature
Electrical thermal aging tests for higher reliability IC	IC test at constant electrical load and maximum allowable temperature
Measurement of electrical parameters	Check of meeting electrical parameters of IC in accordance with specification
Static parameters	Check at the lower and upper values of ambient temperature in specification
Dynamic parameters	Check at normal ambient temperature
Exterior visual inspection	Check of structural elements (welded and soldered seams and joints between glass and metal) under a microscope with magnification not less than 16. Visual inspection of coatings and labeling

Defects in chip connection (chip orientation not according to design drawing, leadout crosses, the eutectic covers less than the allowable part of the chip perimeters, too much paste and glass, defects of the housing base (deformation of the housing, peeling of the gold coating, shifts of the coating and eutectic), defects of the housing (absence of leadouts, corrosions, presence of drops of glue, tin on the flangeoof the housing on the side of the cover), as well as defects in assembly (chip on board glued too high, board bent) that originate in inaccurate assembling of IC.

After annealing to stabilize, parameters and sealing, IC are subjected, in turn, to the effects of their high and low values of ambient temperatures to detect a mismatch between thermal expansion coefficients of individual IC parts. After these tests, the IC must preserve their external appearance and the electrical parameters.

The mechanical integrity of the design is checked by testing on a centrifuge. The microcircuits are attached to the housing in a special device and are subjected to the effect of linear loads which produce forces along the vertical IC axis corresponding to accelerations of 10,000 g for hybrid, and 20,000 g for semiconductor microcircircuits. These forces are usually sufficient to detect defects of welded connections of internal leadouts and poorly attached chips.

In testing IC, devices with improper seals are rejected. The widest failure mechanism in such IC is due to the moist air penetrating the housing and water vapor condensing causing corrosion of the metal coating. Further electrical tests are made in which IC not corresponding to technical norm documentation (INTD) are rejected.

After that, IC which are to meet higher reliability requirements are subjected to special electrical thermal tests which are tested until they fail. This type of testing shows defects not detected in visual inspection very effectively. Typical defects which may be overlooked in visual inspection (but may be detected in thermal current tests) are scratches on the metal coating, thinner metal coating on the oxidation treads and microholes in the oxide under the metal-coated tracks. These defects may also include poor electrical contacts and surface contaminations that cause instability of IC parameters

The final type of test is an all-around investigation of basic IC electricl parameters under normal climatic conditions, as well as at the upper and lower values of the temperature in the specification. Electrical tests are also made at a combination of electrical modes (input signals, loads, feed voltages) which are the worst for the given type of test within the limits of specifications. Rejection tests are completed by checking commercial type IC, with special attention being given to inspecting the quality of welded and soldered joints, glass in the metal joints, the labeling and integrity of the coatings of the leadouts and the housings.

By analyzing typical experimetal data that characterize the effectiveness of rejection tests in the process of production (Table 5.5), it is possible to conclude that the complex of rejection tests makes it possible to detect a considerable number (including 43.2% of the number tested) of potentially unreliable IC and thus raise considerably the quality of IC lots supplied for use in the REA.

Table 5.5

Effectiveness of rejection tests

Type of test	Share of defective IC	Basic types of defects and their share, %
Visual inspection of quality of connecting leadouts	5	Absence (unwelded) connection -- 26.4 Repeated thermocompression -- 17.0 Shift of leadout beyond area of contact pad -- 13.6 Pinched leadout -- 10.6 Shift of welded joints on the crosspieces -- 8.0 Others -- 24.4
Visual inspection of chips	3.7	Splits -- 10.7 Photolithography defects -- 10.7 Others -- 29
Annealing for stabilizing parameters:		
before sealing	0.0	-
after sealing	0.0	-
Cyclic effect of temperature	0.0	-
Linear loads	0.0	-
Leak tests:		
small leaks	7.0	Not in accordance with norm
medium and large leaks	1.9	same
Monitoring electrical parameters at normal conditions	7.4	-
Electrical thermal aging	0.7	-
Electrical tests:		
check of static parameters at higher temperature	0.6	-
Check of static parameters at lower temperatures	4.7	-
Check of dynamic parameters	1.6	-
Inspection of exterior of IC	10.6	Splits and cracks in housing -- 54.4 Twisted leadouts -- 16.0 Labeling defects -- 9.4 Damaged coatings -- 20.2

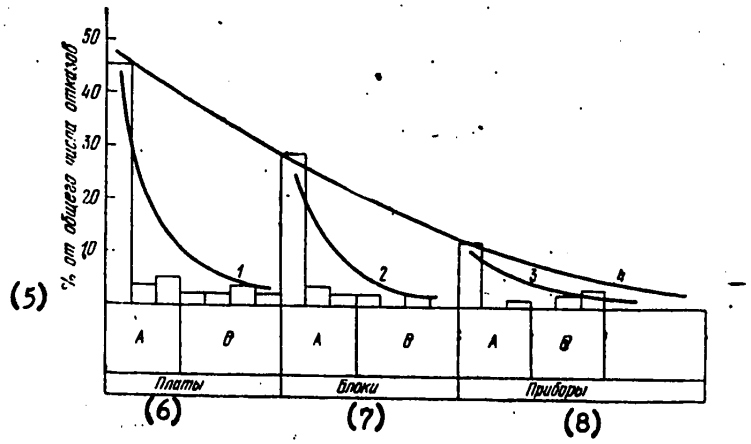


Fig. 5.2. Distribution of IC failures in production and testing of apparatus:

1. failures of printed boards
2. failures in units
3. failures in devices
4. total number of failures
A. shop test stage
B. stage when product is released to quality control department
5. % of total number of failures
6. circuit boards
7. units
8. devices

Inasmuch as rejection tests using above-cited methods are compulsory for all manufccturing plants, the IC quality of various suppliers is equalized to a considerable extent. Now IC that have passed through one and the same "rejection barrier" at various plants have a similar quality level.

5.4 Effect of External Factors on Apparatus Production

A typical technological process of apparatus manufacture using small-scale mechanization tools is shown in Fig. 5.3.

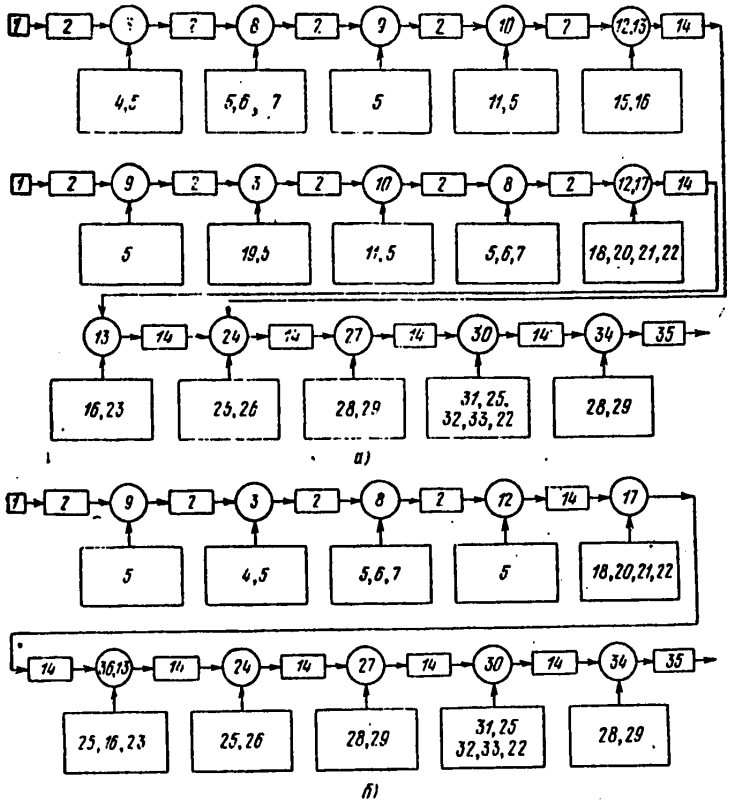


Fig. 5.3. Technological route of passage of IC circuit in manufacturing apparatus in housings types 1 and 3 (a) and housings type 4 (b):

1. IC
2. technological packing
3. forming and trimming leadouts
4. die for forming and trimming the size
5. magnetic vacuum or optic tweezers
6. crucible with thermal regulator
7. device for tinning
8. tinning leadouts
9. making up sets
10. trimming inactive leadouts
11. die with keying device
12. installation
13. soldering
14. board
19. die forming and trimming to size
20. spatula
21. device for gluing
22. thermostat
23. semiautomatic soldering device
24. cleaning flux from boards
25. brush
26. vat
27. regulation
28. control panels, devices
29. hot-cold chamber
30. protection against moisture
31. paint and varnish
32. centrifuge
33. pulverizer

Key to Fig. 5.3. continued

15. device for soldering IC without gluing
16. electric soldering device single-core
17. gluing
18. injector
34. functioning and control check
35. assembly unit
36. fluxing

The sequence of operations and transfers indicated in the technological routes of circuits may change depending on the special design features of the assembly units and the specifics of production. In passing over these routes, the IC are subjected to the effects of various external factors: mechanical, temperature, chemical and electrical (Table 5.6).

Mechanical forces are applied to IC in assembly operations, forming and trimming leadouts, and mounting and gluing the IC to the printed circuit board. Forces acting on leadouts and their insulation may damage the sealing of the housing. Temperature effects are related to the operations of tinning, soldering and dismantling. In these operations, heat passes through the leadouts to the chip or substrate and produces heating of the structural elements of the IC. Chemicals affect the plating material of the housings and the IC labeling when fluxing, cleaning the flux off the printed circuit boards, applying moisture protection and dismantling. And, finally, electrical effects are related to discharges of static electricity through the IC. This effect also takes place at all technological operations if no special measures are taken to reduce and remove static electricity charges from production areas.

As may be seen from Table 5.6, IC are subjected many times, although to a different degree, to effects of external factors in the environment. The most dangerous of them are the actions of the operator because they depend to the greatest degree on the individual preparation of the operator and they are the most difficult to control.

In the process of apparatus production, if the modes and equipment quality do not correspond to the problem of producing highly reliable apparatus, various kinds of IC defects and failutes may originate (Table 5.7).

5.5 Forming and Trimming Leadouts

One basic requirement that the IC housing must satisfy is the preservation within it of comparatively dry air during its entire service life. The presence within the housing of moisture, chemically active and electrically incompatible with semiconductor substances facilitate the origination of sudden, as well as gradual, failures. They happen due to the corrosion of metals and their alloys and intercontact connections, and the deterioration of electrical characteristics caused by changes in the surface and volumetric conductivities and ionic contamination.

Under normal conditions, any surface of a substance is covered by a thin moisture of from 0.01 to 0.001 micrometers. Due to the small values of a molecule of

Table 5.6

External factors acting on IC in the process of apparatus assembly

Source of action	Assembly	Forming and trimming leadouts	Fluxing and tinning wires	Mounting and gluing IC on circuit board	Fluxing and Soldering
Operator	E, M	E	E	E,M	E
Material covers of working positions and rooms	E	-	-	E	E
Packing	E,M	E,M	E,M	E.M	-
Assembly tools	E,M	E,M	E,M,T	E,M	E,M,T
Technological Equipment	-	M,E	E	M	-
Flux	-	-	Kh	-	Kh
Solder	-	-	T	-	T
Washing liquid	-	-	-	-	-
Varnish solvent	-	-	-	-	-
Equipment and materials for moisture protection	-	-	-	-	-

	Cleaning off flux	Regulation	Moisture protection	Functioning test	Disassembly
Operator	E	E	E	E	E,M
Material covers of working positions and rooms	-	-	-	-	E
Packing	-	-	-	-	E,M
Assembly tools	-	-	-	-	E,M,T
Technological equipment	M,E	E	E	E	-
Flux	-	-	-	-	Kh
Solder	-	-	-	-	T

Table 5.6 continued

External factors acting on IC in the process of apparatus assembly

Source of action	Cleaning off flux	Regulation	Moisture Protection	Functioning test	Disassembly
Washing liquid	Kh	-	-	-	-
Varnish solvent	-	-	-	-	Kh
Equipment and materials for moisture protection	-	-	E,M	-	-

Note: designations of actions: E -- electrical; Kh -- chemical; T -- temperature; M -- mechanical.

2.7×10^{-10} meters and the low viscosity of water, moisture is able to penetrate even the intermolecular spaces of complex inorganic compounds. In this case, mechanical destruction of materials occurs, along with a change in the electrical properties of the surfaces, corrosion of metals and their alloys. To avoid this, the sealing of microcircuit housings is usually done in an atmosphere of dry nitrogen in which the water content does not exceed 10 parts per million.

Metals, glass and ceramics used in manufacturing IC housings are practically impenetrable to gas and moisture. Most plastics are hygroscopic to some degree. To preserve a dry inert atmosphere within the housing, the seams between unlike metals should be maximally sealed. According to the adopted norms, a good soldered seal passes not over 1 cm^3 of gaseous helium at a pressure difference of 1 atmosphere in 30 years (practically, this means absolute air impenetrability).

Metals are joined to metals by soldering with soft or brazing solders, hot or cold welding or their combination. Soldering of glass to glass or ceramics is done by melting them at high temperatures, or gluing with low-melting glass. Sealing a metal-glass seam which insulates the leadouts electrically from the IC housing is a complex technical problem. This is because most of the common glass has low coefficients of linear expansion and heat conductivity, while most metals conduct heat well and have high linear expansion coefficient. The difference in the speeds of the heating and cooling of glass and metal parts og soldered joints, and the difference in the linear expansion coefficients leads to mechanical stresses and damage to the joints. As far as IC operatng conditions are concerned, glass and metal are considered compatible if the difference in their linear expansion coefficients do not exceed 4×10^{-7} per centigrade degrees [4].

Usually, in sealing IC leadouts where they come out from the housing, crystallizable glass solders (for example, of the "Piroceram" type) are used. The technology of obtaining such a sealed joint by soldering is based on the formation of a glass-ceramic joint with the crystallization of boron lead-zinc glass. In this method,

the glass is melted by the heat and spreads thoroughly, wetting the joined surfaces of the ceramics, glass and metals like the metallic solder wets and joins metal parts in common soldering).

When the soldered glass is heated further "devitrification" occurs and centers and crystallization of the seam material are produced. The sizes of the crystals formed are proportional to the time and temperature of the process. The strength of such a sealing seam is determined by its crystalline structure and is twice that of a seam from amorphous glass. Moreover, at mechanical loads, microscopic cracks are formed in joints with noncrystallized glass which create paths for moisture penetration into the housing through the glass. In crystallizable glass, however, the microscopic cracks end at the crystals and do not pass through the joint. By regulating the content of the crystalline phase of the seam material, it is possible to change its temperature linear expansion coefficient (TKR) from $40x10^{-7}$ to $120x10^{-7}$ per degree centigrade which agrees well with the TKR values for a great number of glass, ceramics and metals used to make housing parts.

The Kovar alloy (iron, nickel, and cobalt) or the Silmet alloy (iron, nickel and chromium) are most frequently used for IC leadouts. These alloys have low TKR values that agree well in the working and technological temperature range with the expansion coefficients of most glass (the TKR for Kovar is $47x10^{-7}$ per degree centigrade and for glass - - $46x10^{-7}$ per degree centigrade).

An essential special feature of most types of IC housings is that part of the leadout length is under the cover of glass (or ceramics). This cover should not be damaged in forming the leadouts.

Contradictory demands are made on the IC housing. Thus, the housing must be sufficiently strong mechanically to withstand loads originating in the apparatus production and operation and, at the same time, it must be as small as possible with a shape permitting the greatest density of REA assembly. This contradiction must be taken into account, providing a complex of technical measures for preserving the reliability of the microcircuits in designing and producing the apparatus.

In implementing the technological operations on preparing the IC for assembling on the printed circuit board (straightening, forming and trimming leadouts), the leadouts are subjected to stretching, bending and compression. In this case, the stretching force P_1 is applied to the most sensitive mechanical forces zone of the housing -- the seal inlet (Fig. 5.4). If the stretching force is excessive, cracks may originate in the glass or ceramics of the housing where the leadouts pass the housing leading to an immediate, or what is worse, a subsequent loss of housing seal.

The die design for forming and trimming leadouts (Fig. 5.5) must insure the production of independent and sequential forces for clamping P_2, forming P_3 and trimming P_4. The values of these forces are selected so that they insure the integrity of leadout plating, apply the minimal stretching force along the leadout axis and obtain a given configuration. In forming and trimming the IC leadouts, it is

Table 5.7

Possible types of IC failures under various effects

Oject of effect	Technological operation	Effect factor parameter	Type of possible violation and failures
		Mechanical	
IC leadouts	Straighten, forming and trimming	Pulling force Clamping force	Insulator cracking, causing loss of housing seal; leadout deformation (pinching, twisting, breakage)
Insulator, housing base, flexible connections, chip or substrate	Mounting and gluing IC to the board, dismantling	Static force of clamping housing to board	Insulator cracking, causing loss of housing seal. Deformation of housing bottom causing cracking and separation of chip, substrate and breakage of flexible conductors. Destruction of housing
		Temperature	
Leadout coating	Input control straightening, forming and trimming	Force of clamping leadout	Dents and scratches on leadouts leading to corrosion
Leadout insulator, chip, sugstrate, active elements and flexible leadouts	Tinning, soldering, dismantling, drying	Overheating the leadout or solder	Insulation cracking, causing loss of housing seal. Peeling of substrate or chip (in case they are glued) from the mounting surface of the housing, causing breakage of leadouts
		Increased operating temperature	Thermal deformation of protective coatings of chips, causing breakage of flexible leadouts
		Chemical	
Coating and labeling	Fluxing, cleaning, moisture-proofing, dismantling	Chemical activity	Corrosion of coating or basic material of leadouts and housing, and destruction of labeling designations and paint-varnish coatings

Table 5.7 continued

Possible types of IC failures under various effects

Object of effect	Technological operation	Effect factor parameter	Type of possible violation and failures
		Electrical	
Passive and active IC elements, metal coating, p-n junctions, protective oxide	All technological operations	Electrical charge (number of effects, capacitance and resistance in the discharge circuit, voltage difference)	Puncture of oxide, degradation of IC parameters due to puncture in the semiconductor structure

permitted to leave tool traces (prints) on the IC leadouts, that do not damage the plating on the leadouts. Table 5.8 shows allowable values of clamping and forming forces at which damage of plating does not lead to corrosion. Depending upon the cross section of the IC leadouts, the value of stretching force P_1 should not exceed the values shown in Table 5.9.

Table 5.8

Allowable forces of forming and clamping

Sequence of force actions	Cross section of housing leadouts, mm	Clamping N	Clamping microPa	Forming N	Forming MicroPa
Weak traces of working parts of the die on the surface of leadouts in the form of compacting the coating	0.1x0.3	13.7	30.4	18.6	29.4
	0.15x0.45	19.6	30.4	27.4	29.4
Maximum allowable traces of die parts on leadout coating	0.1x0.3	17.6	39.2	24.5	39.2
	0.15x0.45	27.4	39.2	37.2	39.2
Impermissible damage of leadout coating in the form of dents	0.1 x 0.3	21.6	48.0	31.3	49.0
	0.15x0.45	32.3	48.0	46.0	49.0

The die design should profice rigid fastening of each IC leadout outside the glass or cermaics buildup. A leadout section of 1 mm from the body of the housing should not be subjected to bending or twisting deformations. Allowable bending radii should be maintained in forming. Forming IC leadouts of a rectangular cross section should be done with a bend radius of not less than two leadout thicknesses, while leadouts with a round cross section -- with a radius not less than two diameters.

Table 5.9

Maximum values of stretching forces

Leadout cross section, mm	Stretching force per one leadout, Newton
Up to 01	0.245
Above 0.1 to 0.2	0.49
Above 0.2 to 0.5	9.8
Above 05 to 2.0	19.6

The IC leadouts inside the housing or leadouts not used in the circuit of its application and not affecting the working capacity of the IC, may be trimmed 1.0 mm from the housing body; however, it should be taken into account that a considerable part of the heat is removed over IC leadouts (especially of small sizes).

In a typically improper design of a technological device, the formation of leadouts of type 4 housings (Fig. 5.6b), a gap (not less than 0.5 mm from the body of the housing), necessary to preserve the integrity of the ceramics was not left. A die of such design may damage the housing seal of the IC.

Fig. 5.7 shows another typical assembly error. We will assume that the forming of IC leadouts, intended for installation on a multilayer printed circuit board with open contact pads, was done at the depth of the second-third layer (Fig. 5.7a). Actually, however, it was necessary to solder them to other layers. In assembly, the leadouts were bent manually at the inlet of the seal (the bend angle in the vertical plane may reach $\pm$ 60%). Straightening the leadouts made without rigid fastening of the leadout zone on a section 1 mm from the body of the housing (i.e., without using the technological device) may lead to damage of the leadout at the housing. With such a method of assembly, the IC may lose its seal during the consequent mechanical forces when operating the apparatus because the deformed leadouts are in a stressed condition (Fig. 5.7b).

5.6 Tinning and Soldering

In the production of radio electronic apparatus, group methods are widely used to implement individual technological operations, for example, tinning IC leadouts by "dipping into melted solder" or soldering by means of a "wave of solder." These modes of operations (temperature of the melted solder, contact time between the solder and the housing leadouts, area of the contact zone of the leadout with the solder), selected without taking into account the heat transfer characteristics of concrete types of IC housings may lead to a destructive effect of heat shocks on IC.

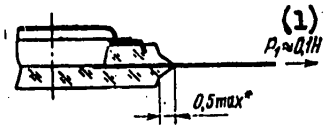


Fig. 5.4. Direction of stretching force in forming and trimming leadouts
1. $P_1 \approx$ 0.1 Newton

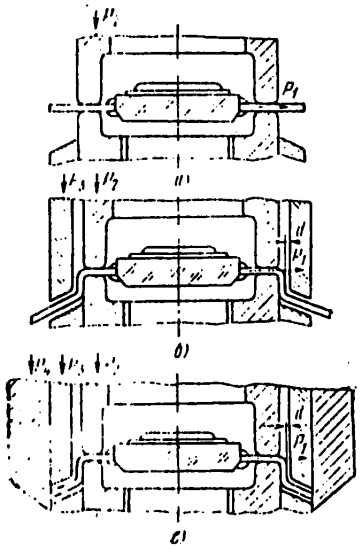


Fig. 5.5. Forming and trimming IC leadouts:
a -- clamping the leadouts; b -- forming the leadouts; c -- trimming the leadouts.

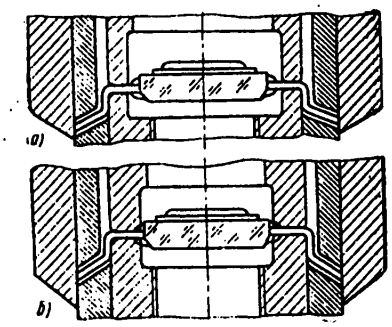


Fig. 5.6. Correct (a) and incorrect (b) forming leadouts of a planar housing

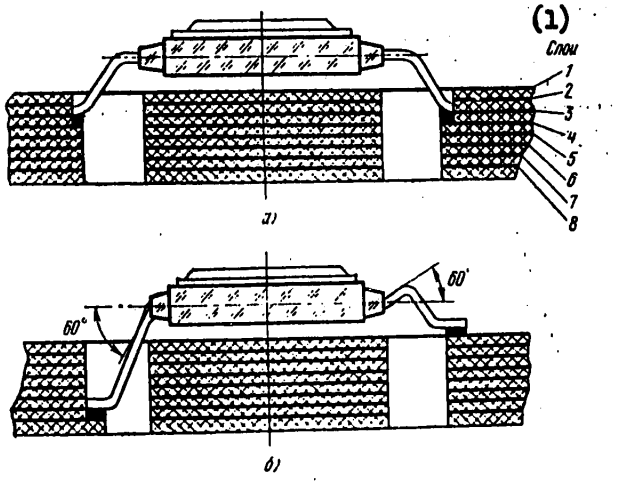


Fig. 5.7. Correct (a) and incorrect (b) assembly of planar housings on a multilayer printed circuit board with open contact pads.

1. Layers

Fig. 5.8 shows schematically individual elements of IC design which are subjected to thermal effects and participate in heat transfer. A temperature gradient is produced along the IC leadout in contact with the melted solder causing the transfer of heat. The heat exchange is implemented from the soldering zone (zone A) through the leadout metal to the ceramic base of the housing body (2) and further to the IC chip (4). The heat flow is also transmitted to the chip from the inner part of the leadout (zone B) through the internal connecting conductor (3).

The speed of heat transmission depends on the temperature difference, on the heat conductivity of the material and the configuration of the IC structure elements. The heat conductivity coefficient is calculated by formula

$$\lambda\,[w/(\text{м}\cdot{}^\circ\text{C})] = Q/\Delta t \cdot S \cdot \Delta T/\Delta l, \qquad (5.1)$$

where Q is the amount of heat, joules; ΔT -- temperature gradient, °C; l -- distance from heat source; $S = \Delta Q/T$ -- system entropy, joules/degree. Formula (5.1) contains the specific heat of the system $c = Q/\Delta t$ and the temperature gradient grad $T = \Delta T/\Delta l$. Values of heat conductance coefficients of several materials used in the IC structure are shown below.

Material	λ, watts/(meters. °C
Silver	460
Copper	390
Beryllium oxide	208
Aluminum	203
Silicon	83.5
Aluminum	19.6
Kovar	19.7
Glass (borosilicate)	1.1
Laminated epoxy plastic	0.28

To evaluate the degree of the heat effect in tinning and soldering, it is necessary to know the material heat transfer coefficient of IC structure elements

$$a = \lambda/cp, \qquad (5.2)$$

where λ -- coefficient of heat conductivity, c -- specific heat, joules (kg.°C); ρ -- density, kg/m^3. This coefficient is determined experimentally for each type of IC housing and a given maximum temperature of elements in individual structures.

Fig. 5.9 shows diagrams of heat distribution for five housing designs. Isotherms are shown on these figures that characterize the degree of heating of IC elements when tinning leadouts. This data was obtained by thermal melting indicators whose action is based on the irreversible and sharp change in color when a certain

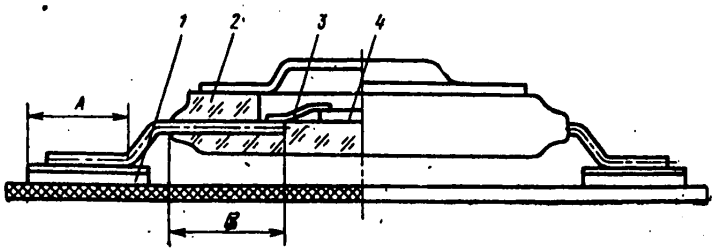


Fig. 5.8. Heat exchange circuit in tinning and soldering external IC leadouts:

1. contact pad
2. housing
3. internal connecting conductor
4. IC chip

critical temperature is reached. In the experiment, thermal melting indicators with various critical temperatures were coated on the substrate or bottom of the IC. Then the IC was enclosed by covers, and fastened in a special holder made of textolite, and the tinning operation was done by dipping the leadouts in melted solder (temperature of the melted solder was 260° ± 5°C), distance from housing to solder surface was 1 mm, the contact time between the leadouts and solder was 3 seconds.

The devices used in the experiment provided a minimal removal of heat from the IC housing; in this case, the linear shifts perpendicular to the surface of the solder were held to an accuracy of ± 0.2 mm.

To determine the precise temperature values (the thermal melting indicators gave only limits of temperature changes), and to evaluate the changes of this temperature with time, temperature measurements were made on the most typical IC elements (leadouts, substrate, chip) by a thermal electric method for different modes of tinning and soldering. The temperature was measured by a low-inertia copper-constantan thermocouple with an 0.06 mm electrode diameter which made it possible to reduce the measurement error and the thermocouple effect on the true value of the temperature. In the experiment, the thermocouple was attached to the measurement point, then the housing cover was closed and sealed by "cyacrin" glue. The thermocouple indications were recorded by a high-speed self-recording device.

The relationships between the temperatures of the IC elements of various types in the process of tinning and the tinning time and the distance to the solder surface are shown in Fig. 5.10.

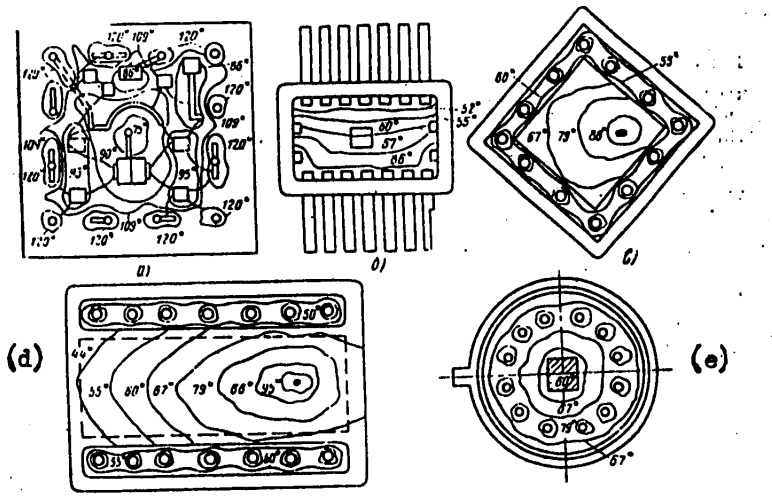


Fig. 5.9. Temperature distribution of IC housing heating when tinning leadouts: a -- type "Tropa" housing; b --planar housing 401.14-1; c -- housing 151.15-1; d -- type "Po ol" housing; 3 -- round housing 301.12-1.

In this figure temperature zones obtained by thermal indicators of melting, are shown for comparison. The test results show that temperature values obtained by the thermoelectrical method are in the temperature zone determined by the thermal indicators of melting. An analysis of the experimental data indicates that the temperature difference of heating IC elements when tinning and soldering reaches 10...20°C and for all housing types 301.12-1, the tinning mode is more "rigid." Tinning parameters are shown below.

Parameters of tinning mode	Norm
Max. soldering temperature, °C	250
Max. time the leadouts are in the melted solder, seconds	2.0
Min. distance from housing "body" to boundary of solder along the leadout length, mm	1.3
Max. allowable number of dippings of the same leadouts into the solder	2
Minimum interval of time between two dippings of the same leadouts into the solder, minutes	5.0

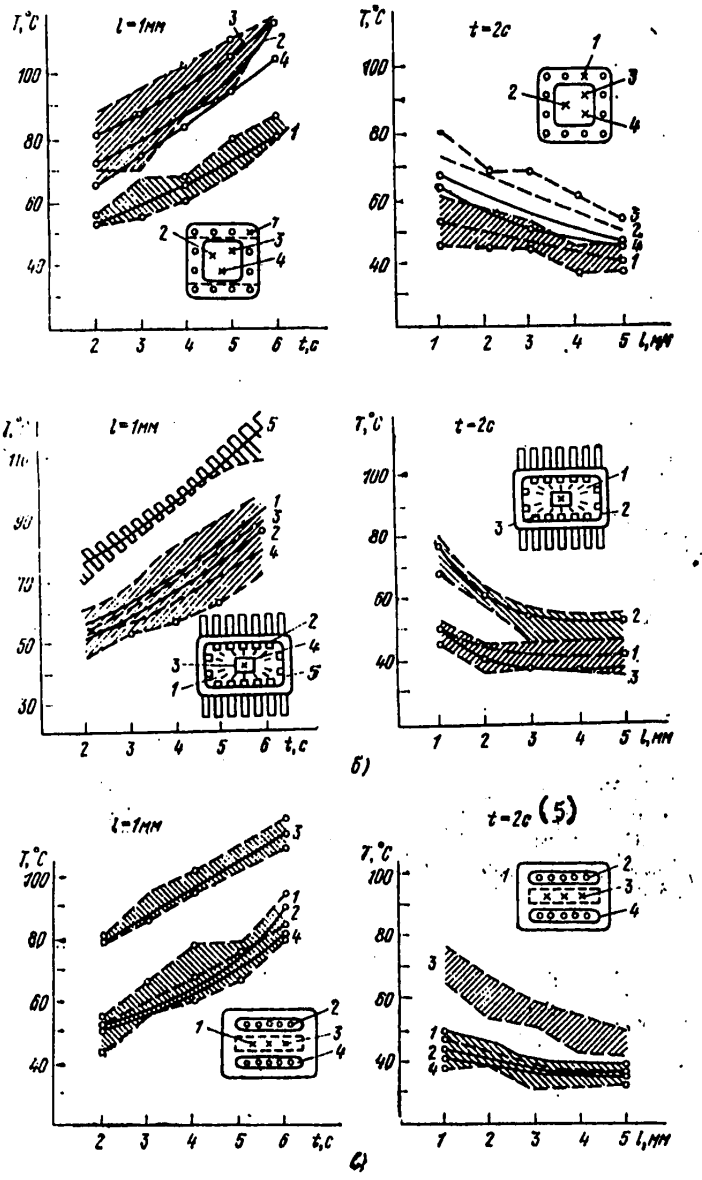


Fig. 5.10. also continued on the next sheet

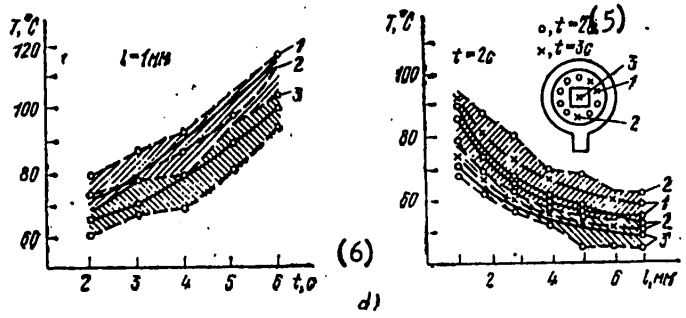


Fig. 5.10. (continued from previous sheet) Relationship between temperature of IC elements in the process of tinning and tinning time (t) and the distance (l) between the level of solder for housings series 217 (a), 106 (b), 218 (c) and 122 (d). The numbers on the curves correspond to the points of the IC elements at which the measurement is made; solder temperature is 260 ± 5°C.

5. t = 2 seconds 6. t, seconds

In tinning, the solder should not touch the seal inlets of the housing. The solder should not fall on glass or ceramic parts of the IC housing. The boundary of solder flowing on leadouts should be no closer than 1 mm to the body of the housing (Fig. 5.11a); however, some nonuniformity of tinning along the length of the leadout is allowed. The minimum length of the tinning section along the leadout length from its end must be no less than 0.6 mm (Fig. 5.11b), but "icicles" on the ends of IC leadouts are permitted (Fig. 5.11c).

It is necessary to make sure that connections are not formed between the leadouts and the soldering surface should be continuous without cracks, pores and untinned sections (Fig. 5.11d).

Equipment used for tinning must insure the setting and measuring of the temperature with an error no greater than ± 5°C.

The quality of soldered connections should be determined by the following criteria: the soldered surface should have a light or mat finish without dark spots and foreign inclusions. The shape of the soldered connections must have concave fillets of solder along the seam (without an excess of solder). The contours of the leadouts should come through the solder. In soldering IC housings with planar leadouts the following is permitted: a flooding form of soldering in which contours of individual IC leadouts are fully hidden under the solder on the soldered side of a connection (Fig. 5.11e, f), partially covering the surface of the contact pad with solder along the soldering perimeter, but in no more than two places,

not exceeding 15% of the total area (Fig. 5.11g), solder bits of conical shape (Fig. 5.11h) and rounded shape (Fig. 5.11i) where the soldering tool is removed, a small shift of the leadout within the contact pad (Fig. 5.11j) and the spread of solder (only within the boundaries of the leadout length, suitable for wiring).

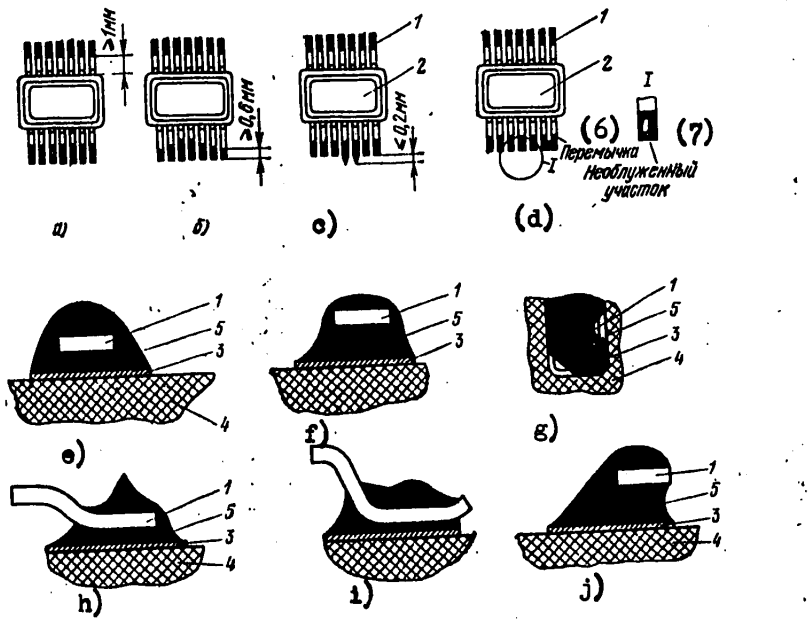


Fig. 5.11. Examples of tinning and soldering leadouts of a planar housing: a -- zone of solder flow; b -- allowable nonuniformity of tinning; c -- presence of "icicles"; d -- nonuniform tinning and false connections; e, f -- flooding form of soldering; g -- partial tinning of contact pad; h, i -- conical shape solder beads; j -- small shift of leadouts; 1 -- leadout; 2 -- housing; 3 -- contact pad; 4 --printed circuit board; 5 -- solder; 6 -- connection; 7 -- untinned section

When soldering IC leadouts into metal-coated holes, the soldered connections must be according to the sketches shown in Fig. 5.12a-d. The solder on the side of the housings should not spread beyond the boundaries of the contact pads. The leadout end may be untinned. The metal-coated wiring holes must be filled with solder to a height of not less than 2/3 of the thickness of the board. The correction of defective connections from the side of the IC mounting on the board is not permitted.

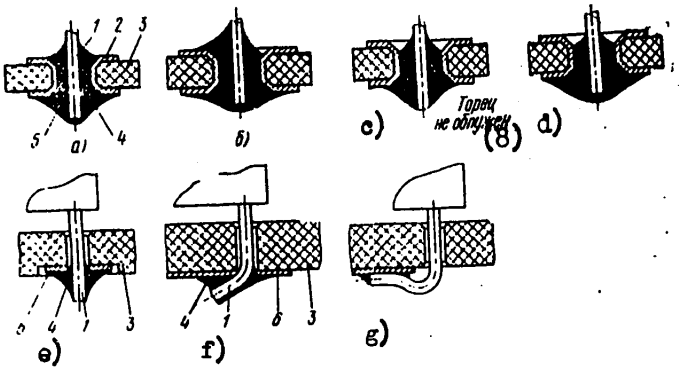


Fig. 5.12. Examples of soldering housings with plug-coupler leadouts: a, b, c, d -- soldering in metal-coated holes; e, f, g -- soldering in nonmetal-coated holes; 1 -- leadout; 2 -- metal-coated hole; 3 -- printed circuit board; 4 -- solder; 5 -- cavity in solder; 6 -- contact pad; 7 -- end not tinned.

When soldering IC leadouts to contact pads of printed circuit boards with holes not coated with metal, the soldered connection must be made according to the sketch (Fig. 5.12e-g). The spreading of the solder along the IC leadouts should not reduce the minimum distance from the housing to the soldering point, i.e., it should be within the zone suitable for the wiring shown in the specification. There need be no solder at the ends of the leadouts.

The equipment and fixtures used in soldering must provide the following; automatic maintenance and control of the melted solder temperature with an accuracy of $\pm$ 5°C when implementing the "soldering wave" operation; maintenance and periodic control (every 1 to 2 hours) of the temperature of the soldering bit with an accuracy of $\pm$ 5°C in the individual method of soldering; control of the time the IC leadouts are in contact with the soldering bit or with the molten solder in group soldering; also control of the distance from the housing body to the boundary of the solder along the length of the leadout. The soldering bit must be gounded (the ground resistance should be no greater than 5 ohms). Table 5.10 shows the recommended modes of IC soldering using single-bit and group methods.

Table 5.10

Recommended IC soldering mode

Parameter	Soldering IC with planar leadouts		Soldering IC with plug-coupler leadouts	
	1-bit method	group method	1-bit method	group method
Max. temperature of soldering iron core, °C	265	-	280	-
Max. contact time of each leadout, seconds	3.0	-	3.0	-
Min. time interval between soldering of adjacent leadouts, seconds	3.0	-	3.0	-
Max. temperature of molten solder, °C	-	265	-	265
Max. contact time of each leadout with solder	-	2.0	-	3.0
Min. distance from housing to solder along leadout, mm	1.0	1.0	1.0	1.0
Min. time between two repeated solderings of same leadouts, min.	5.0	5.0	5.0	5.0

5.7. IC Assembly on Printed Circuit Boards

The following are the design features of IC housings: the presence of seal inlets and sealing seams, and a relatively "thin" housing base (0.1...0.2 thick), to which are fastened the substrates or the chip, determine a whole number of specific requirements which must be implemented in assembling IC on printed circuit boards. All precautionary measures, in this case, are reduced to protecting the IC housing from impermissible deformations.

On one hand, the assembly method must provide mechanical strength that would guarantee resistance to mechanical loads expected in operation but, on the other hand, "rigid" attachment of the housing is impermissible because the deformation of the printed circuit board (if its deflection is even several tenths of a millimeter) may result either in the cracking of the sealing joints of the housing, or in the deformation of the bottom and the rupture of the substrate or chip.

In most cases of IC application, mechanical stability is insured only by soldering all leadouts to contact pads. The necessity and methods for additional fastening of the IC to the board are determined by the rigidity of the operating conditions of the apparatus, as well as the weight and size of the IC housings.

The design of the apparatus must insure efficient removal of heat by air convection and heat-removing metal buses. The convection is provided by using housings with the maximum permissible gaps between the plane of the board and the bottom of the housing. The housing arrangement on the printed circuit board must provide the possibility of coating it with moisture-protective varnish without having it fall into places that should not be coated, and have free access for dismantling any IC. Taking into account the necessity of preserving the integrity of the housing and to provide for heat removal, recommendations are given below for using various types of IC.

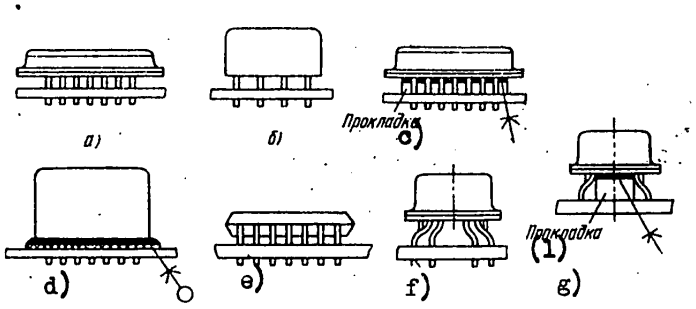


Fig. 5.13. Variations of mounting various housings on the print circuit board with metal-coated holes:
a,b -- housings with plug-coupler pins without additional fastening;
c,d -- housing with plug-coupler pins with additional gastening;
e -- plastic housing; f -- cylindrical housing without additional fastening; g -- cylindrical housing with an electric insulation spacer

1. Spacer

Fig. 5.13a,b shows variations of mounting housings with plug-coupler pin leadouts (housings 151.15-4 and 151.15-6). These housings are mounted in metal-coated holes. The IC do not have leadouts. The gap, equal to 1 - 0.5 mm, is chosen to insure IC stability in the entire range of mechanical loads and the preservation of the integrity of the housing (at smaller gaps, it is possible to damage the seal inlet of metal-glass housings due to the thermal effect of soldering).

IC in housings 151.15-2, 151.15-3 (Fig. 5.13c) and "Aktsiya" (Fig. 5.13d) require additional fastenings. IC in housings 151.15-2 and 151.15-3 are glued to insulation spacers, for example, made of DSV-2-R-2M (GOST 17478-72) or AG-4 (GOST 10087-62). The spacers must be fastened rigidly to the printed circuit board. In choosing the dimensions of the insulation spacers, it is necessary that they be as close as possible to the area of the IC housing base and that the integrity of the seal inlet be preserved. The IC in the "Aktsiya" housing (Fig. 5.13d) is mounted against an LN cement, placed along the perimeter. Cover should be provided with a two-sided arrangement of conductors in the board under the electric insulation of the IC housings.

IC in housings 201.14-1 are mounted on boards with a single-side or a two-sided arrangement of printed conductors into metal-coated holes with a gap insured by the design of the leadout (Fig. 5.13e). Fir. 5.13f,g shows variations of mounting IC with housings 301.8-1, 301.8-2 and 301.12-1 with formed leadouts. They are mounted with a gap of 3+0.5 mm (Fig. 5.13f). If the apparatus is subjected to higher mechanical forces in operation, rigid spacers of electrical insulation material must be used. The spacer should be glued to the board and the base (to the bottom) of the IC (Fig. 5.13g). The design of the spacer must also insure the integrity of the seal inlets of the microcircuit. IC with cylindrical housings without leadouts are mounted onto metal-coated holes with a 1+0.5 mm gap.

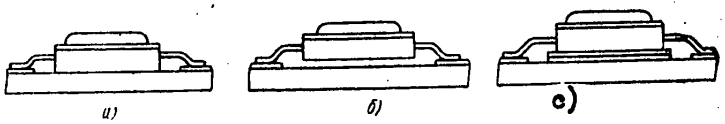


Fig. 5.14. Variations of mounting planar housings:
a -- against the printed board; b -- with gap; c -- against a spacer

IC in housings 401.14-1 and 401.14-2 with shaped leadouts may be mounted on the boards with a single-side or a two-sided arrangement of printed conductors by the following methods: against the printed board or on a spacer (Fig. 15.14a,c) or with a gap of up to 0.3 mm (Fig.15.14b). In this case, the additional fastening is provided by coating with varnish. The gap may be increased to 0.7 mm, but then the IC housing must be fastened additionally to the board by glue.

Planar housings must be glued to the entire plane of the housing base. The thickness of the seam is determined by the chosen variation of forming the leadouts (the distance from the plane of the IC base to the board), but the gaps between the IC and the board must all be filled with glue. When IC are mounted on planar

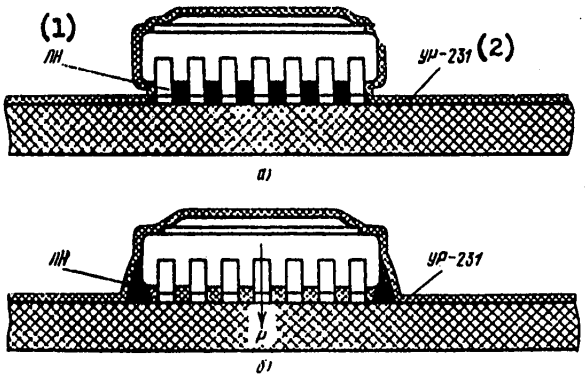


Fig. 5.15. Example of proper (a) and improper (b) mounting of a planar housing on a printed circuit

1. LN 2. UR-231

housings a shift of the free ends of the leadouts in the horizontal plane is permitted within ± 0.2 mm for matching with the contact pads. Free ends of leadouts may be shifted within ± 0.4 mm in the vertical plane from the leadout position after forming.

The use of glues VK-9(ShchI0.026.400TU) or AK-20 (TU 6-10-1293-72), as well as cement LN (TU MKP. 3052-55) to glue IC to printed boards is recommended. The drying temperature of materials used for fastening IC to the board should not exceed the permissible temperature for operating IC. The recommended drying temperature is 65 ± 5°C. In gluing IC to the printed board, the squeezing force should not exceed 0.08 microPa. It is not permissible to glue IC with glue or cement applied at individual points on bases or at the ends of the housings.

Fig. 15b shows an impermissible variation of IC mounting which is glued to the end of the housing (this may be done for simplifying the dismantling of IC). In this method, the gap between the bottom of the IC and the board is partially filled with cement. In implementing the moisture protection operation, UR-231 varnish may get into the gap which, by polymerization, may be able to cause the deformation of the bottom of the housing (0.1...0.15 mm thick), the ungluing of the chip or breakage of the internal connections of the IC. In all cases of installation of IC on printed circuit boards, no force should be applied that leads to the deformation of the housing of the IC.

5.8. IC protection Against Electrical Effects

The degree of integration of the IC (i.e., the density of the grouping of elements on one wafer) is increasing with time because of the development of a technology that makes it possible to reduce the dimensions of the elements, as well as those areas by means of which the elements are electrically insulated from each other on the IC wafer. Such an increase in the density of the elements on the surface of the wafer makes it possible to improve the electrical and functional parameters of the IC, but is accompanied by a reduction in allowable electrical loads, and increases the sensitivity of the microcircuits to static electricity discharges. Table 5.11 shows comparative typical characteristics of transistors manufactured by different technological processes.

Table 5.11

Some parameters of various designs of transistors

Technical characteristics	Planar epitaxial technology	"Izoplanar-1" technology	"Izoplanar-II" technology
Dimensions of emitter area, micrometer	25x38	5x25	2.5x12.5
Breakdown voltage emitter-collector, volts	23	7	5
Breakdown voltage collector-base, volts	55	22	14

Actually, an analysis of IC that failed in the process of production indicates that the cause of failures of up to 40 to 50% of such IC is electrical overload.

In damaged IC there is detected a deterioration of the steepness of the volt-ampere slope or a complete breakdown of the p-n junction although there are no changes in the metal coating visible under a microscope. Emitter junctions are damaged more frequently than others. Externally the defect is manifested in that the value of the reverse current increases by several orders of magnitude, while the current amplification coefficient decreases essentially (by 70%). In this case, the electrical overloads cause irreversible changes in the p-n junction structures leading to the deterioration of the efficiency of the emitter. A typical volt-ampere characteristic of the junction for a reverse bias is shown in Fig. 5.16. The emitter current (curve 2) is almost linear which may be due to the appearance of an ohmic shunt on the surface, or in the volume of the p-n junction.

A partial or complete burn-out of the metal coating and the formation of jumpers between adjacent tracks may occur, along with highly visible traces of p-n junctions breakdowns on the surface or under the passivating layer.

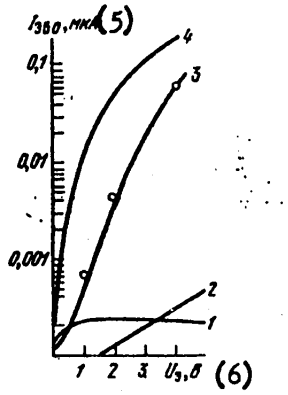


Fig. 5.16. Volt-ampere characteristics of emitter junctions of two transistors without housings:
1,2 -- transistors in working order; 3,4 -- transistors after a 600-volt discharge through the emitter junction in the reverse direction;
5 -- microamperes; 6 -- volts

IC that failed due to electrical overloads are characterized by the melting and spattering of aluminum (when boiling) and the formation of short-circuited adjacent sections of the metal coating. The burn-outs occur most frequently at the "weakest" points of the current-carrying tracks that have local thinning (at the "steps" of the oxide).

One cause of IC failures of the above-indicated types may be the effect of discharges of static electricity originating during various technological operations due to the wide use, under production conditions, of strongly electrifiable synthetic and other insulation materials. Moreover, due to poor grounding of device housings and technological tools, considerable network noise inductions may occur.

The origination of static charges is due to several generating mechanisms and the value of these charges depends on many factors. The values of static voltages (U_{CT}) on the surface of the dielectric, independently of the mechanism of their generation are always proportional to the specific surface resistance of the (ρ_s). This can easily be seen by analyzing the experimental data on the value of static voltages originating on the surface of several materials at a relative humidity of 50% (Table 5.12).

Fig. 5.17 shows the relationship between the static voltages and the relative air humidity of two types of material used widely for the special working clothes of production personnel -- Lavsan and cotton cloth. The relative humidity of the air is used as the parameter when measuring the voltages. In analyzing these relationships, it should be noted that static potentials at low relative humidity of the air (40 to 50%) reach 3 to 10 kilovolts. The static voltage on Lavsan is higher than on cotton cloth and depends strongly on the relative himidity of the air (at 65% humidity the voltage on cotton is zero, while on Lavsan, it exceeds 3 kilvolts).

In developing measures to protect IC from the effect of static electricity discharges, it is necessary to take into account also the ability of insulating materials to retain charges accumulated on their surfaces for a certain time. As the charge retention time is assumed the time (τ_y) during which the accumulated static voltage reduces to a half or a third.

τ_y may be measured as follows: the surface of the tested material is charged (for example, by rubbing) to a certain voltage and a flat metallic contact electrode is applied to the surface of the material. The electrode is connected to a type S-95 static voltmeter and then the time it takes for the voltage to drop to half or a third is recorded. The charge retention time is proportional to the specific surface resistance of the materials exactly the same as the values of the static voltages.

Table 5.12.

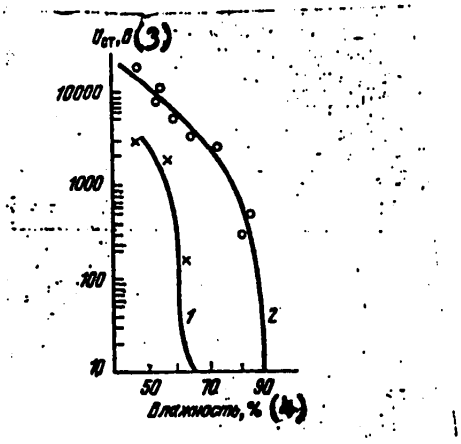
Static voltages and surface resistance of various materials

Material	U_{CT} Kvolts	ρ_s, ohms
Polyvinyl chloride	1.3 - 2.8	1×10^{14}
Wood	0.7	1.4×10^{13}
Glass	0.6 - 0.8	9.6×10^{12}
Getinaks	0.45	4.3×10^{12}

Table 5.13

Charge retention time on various surfaces

Material	τ_y, seconds	ρ_s, ohms
Paper	25	$(3.3 - 9.8) 10^{11}$
Varnished wood	1200	1.4×10^{13}
Polyvinyl chloride	7800	1.0×10^{14}
Glass	9000	2.2×10^{15}
Synthetic linoleum	12000	4.0×10^{14}



5.17. Relationship between the value of static and relative humidity of air for cotton cloth (1) and Lavsan cloth (2)
3. Volts 4. Humidity

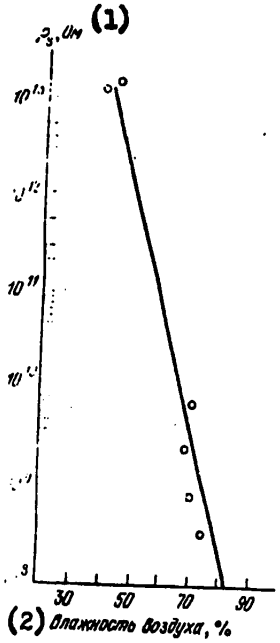


Fig. 5.18. Relationship between specific surface resistance (ρ_s) of polyvinyl chloride and the level of the relative humidity of the air,
1. Ohms 2. Air Humidity, %

Table 5.13 shows experimental data on charge retention time at the relative humidity of the air of 65%. The time retention time on the surface of synthetic linoleum was measured at a lower humidity (60%).

It may be concluded from Fig. 5.18 that an increase in humidity from 40 to 83% reduces the specific surface resistance of polyvinyl chloride by five orders of magnitude.

In organizing apparatus production using IC, it must be remembered that considerable static voltages, from hundreds to several thousands of volts, are produced on the hands of the workers when doing various technological operations. The value and polarity of these voltages depend on many various factors, including the humidity

of the air in the room, the material of the clothing worn, the materials used to cover the table and chairs, the technological and test equipment and the degree of insulation of the worker from the "ground" (materials of shoes and floor) Fig. 5.19).

An analysis of the data in Fig. 5.19 shows that with working shoes with rubber soles (curves 2), the static voltage on the hands of the workers is 2 to 2.5 times higher than when working in leather shoes (curves 1). This is due to the fact that the leakage resistance of shoes with rubber and leather soles differs by almost two orders of magnitude (leakage resistance of shoes with rubber soles is 1.8×10^8-2.8×10^9 ohms, while on leather soles -- it is 5.6×10^6 to 1.9×10^7). It should also be noted that high values of static voltages on the workers' hands correspond to the case where dielectrics with high specific surface resistance are used at the working position.

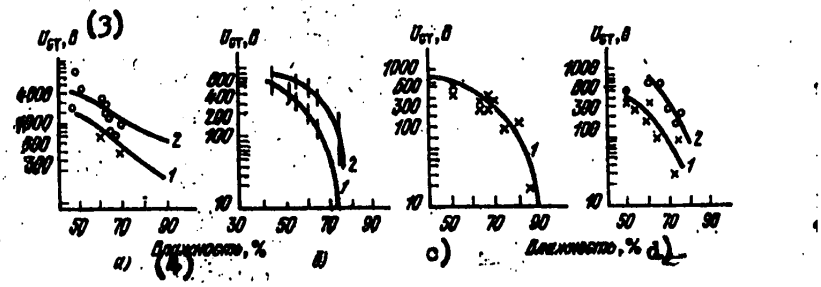


Fig. 5.19. Relationship between the static voltage originating on the workers' hands when rubbing different materials and the relative level of the humidity of the air for the table surface being of polyvinyl chloride (a); varnished wood (b), textolite (c), covered with glass (d). Workers' shoes with leather (1) and rubber soles (2).

3. Volts 4. Humidity, %

When the workers walk on a floor covered with synthetic linoleum, charges are also accumulated on them (Fig. 5.20). The prevention of static electricity charges in the production process should proceed in two directions: first reduction of the possibility of static electricity charge generation and, secondly, insurance of the removal of accumulated charges from the production and technological equipment and workers.

In organizing apparatus production sections where IC are used the use of finishing materials with high specific surface resistance is not recommended. The use of finishing materials for production furniture, floors, testing and technological equipment materials with low -- not over (1 to 5)10^9 ohms, insures the necessary conditions for the rapid draining of the static electricity charges.

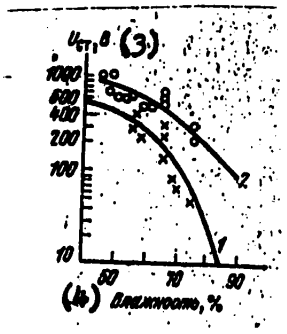


Fig. 5.20. Relationship between static voltage on the worker at various values of the relative humidity and degree of insulation from the floor, if the workers' shoes have leather (1) or rubber (2) soles.

3. Volts 4. Humidity, %

Table 5.14

Relative characteristics of two types of linoleum

Type of synthetic linoleum	ρ_s, ohms	ρ_v, ohm.cm	τ_y, seconds
Common	4×10^{14}	5.9×10^{17}	12000
Antistatic	5×10^{9}	2.4×10^{9}	0.5

A special antistatic linoleum is recommended to cover surfaces. The comparative electrical parameters -- specific surface (ρ_s) and volumetric (ρ_v) resistances and the time of charge retention (τ_y) of common and antistatic linoleums are shown in Table 5.14.

The use of antistatic linoleum eliminates the possibility of charge accumulation on the worker: a contact by the worker's hand with a surface covered by the antistatic linoleum before doing the next technological operation insures draining of the charge in 1 second. Synthetic cover P-2-E-S-5 has the best antistatic properties: specific surface resistance of the material is 10^6 ohms. The use of such material insures the complete destruction of the static charges because the draining time of a charge from a person is only 2×10^{-4} seconds.

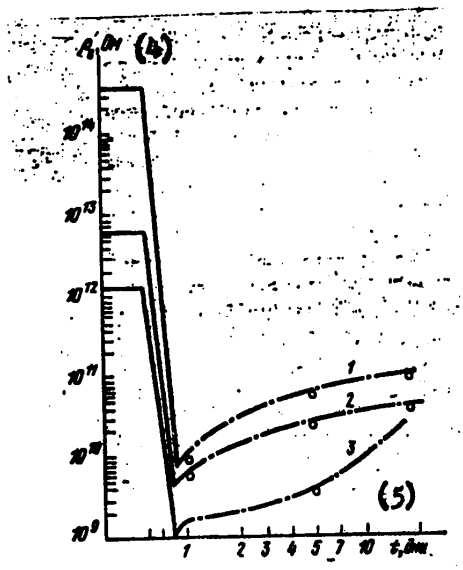


Fig. 5.21. Relationship between specific surface resistance (ρ_s) of various materials and time before (———) and after (— · —) their treatment by "Charodeyka" paste:

1. synthetic linoleum
2. textolite
3. cardboard
4. ohms
5. days

One of the methods recommended to reduce the specific surface resistance of covers is to use surface-active substances (PAV), for example, "Charodeyka" paste (TU-6-15-604-71), which is applied in a thin layer on the working dielectric surfaces of tables, test and technological equipment, packing for storing IC and assembly units, and is used to mop floors and wash paper covers for production furniture. The antistatic properties of the paste with respect to time are characterized by experimental data (Fig. 5.21).

The increase in surface resistance with time of the processed surface is due to the natural drying and aging of the paste and also to its being rubbed off in operation. The resistance increases by an order of magnitude in 10 to 15 days; therefore, the interval between applying the paste should be determined on the basis of concrete productions. In the case of using antistatic linoleum, as well as

in using PAV to drain charges, it is necessary to insure good electrical contact of one-two points of the processed surface (contact area not less than 1 cm^2) with the "ground."

To reduce the surface resistance of covers at working positions, it is recommended to insure the maximum relative humidity in the production areas (a satisfactory result may be achieved at 65 to 70% humidity).

Materials with surface resistances of 10^6 and 10^8 ohms are recommended for interoperation packing. The packing material may be coated with aluminum current-conducting paint. The paint layer does not prevent charge draining because it has a low ρ_s.

The continuous oontact between the worker and the "ground" should be provided by a special antistatic bracelet, connected through a high-voltage resistor (for example, the KLV type 10 kilovolt resistor). However, it should be taken into account that the use of an antistatic bracelet is effective only when the working position, packing and fixtures are made of materials with low surface resistances that prevent the accumulation of static electricity charges. Otherwise the possibility of IC damage is high. Actually, charges of static electricity on a high resistance surface, for example, on interoperation packing, may produce a voltage of up to several thousand volts on the packing itself, as well as on the IC in it. At the moment of contact between the worker and the IC when there is a current circuit "IC-worker-ground" the pulse of the discharge current may cause the failure of the IC [2].

The workers' clothes should be made of cotton cloth, be laundered with antistatic "Charodeyka" paste or other surface-active substance. The workers should wear leather or semiconducting rubber soles.

5.9. Dismantling

In manufacturing apparatus, it frequently becomes necessary to dismantle IC. The following are recommended for this operation. If IC with planar leadouts are to be disassembled, it is necessary to: remove the varnish at points of leadout soldering (if needed); unsolder the IC leadouts using a mode that does not exceed the soldering mode specified in the IC certificate; lift the ends of the leadouts from where they were fixed in the seal inlet; remove the IC from the boards thermomechanically by means of a special device. (This device is heated to a temperature that prevents the IC housing from overheating above the temperature indicated in the certificate. The heating time should be sufficient to remove the IC and not permit cracks, chipping and damage to the housing).

When removing an IC with pin leadouts, it is necessary to: remove varnish at the points of soldering of the leadouts; unsolder the leadouts with a special soldering tool (the solder should be drawn off according to a mode not exceeding the soldering mode, specified in the IC certificate, until all IC leadouts are freed from connection with the metal-coated printed circuit board); remove IC from the board (not permitting cracks, chipping of glass or deforming of the housing and the leadouts). In this case also, if necessary, it is permitted (if the housing is fastened

to the board with varnish or glue) to use a thermomechanical method to remove the IC that prevents overheating of the housing, or chemical solvents that have no effect on the coating, labeling and material of the housing.

BIBLIOGRAPHY

1. Integrated Circuits. Principles of Design and Production. Translated from the English. Edited by A. A. Kolosov. Moscow. Sovetskoye radio, 1967.

2. Kaverznev, V. A.; Zaytsev, A. A.; Ovechkin, Yu. A. "Static Electricity in the Semiconductor Industry." Moscow. Energiya, 1975.

2291
CSO: 1863/209

Table of Contents

Foreword

Chapter 1 Page

Terminology in microelectronics and classification of integrated circuits 6

1.1. Introduction 6
1.2. Terminology in microelectronics 7
1.2.1 Integrated circuits, elements of components (7). 1.2.2 Elements of design (7). 1.2.3. Simple and complex IC (9). 1.2.4. Microassemblies and microunits (10).

1.3. IC classification 11
1.4. System for conventional designations of IC 12

Chapter 2

Integrated circuit manufacturing methods 18

2.1. Film and hybrid technology 18
2.1.1. Materials for hybrid IC (19). 2.1.2. Manufacturing of hybrid IC elements (22). 2.1.3. Wiring of electrical connections in hybrid IC (24).
2.2. Semiconductor technology 24
2.2.1. Materials for elements of semiconductor IC and their manufacture (36). 2.2.2. Manufacture of integrated circuits (29). 2.2.3. Division of wafers into chips, wiring of IC (35). 2.2.4. Sealing IC chips (36). 2.2.5. Manufacture of IC housings (37).
2.3. Special features of high degree of integration of IC technology 40

Chapter 3

Digital integrated circuits 46

3.1. Purpose and application 46
3.2. Logic functions obtained by digital IC 46
3.3. Classification of digital IC and their basic electrical parameters 51
3.4. Transistor-transistor logic circuits 56
3.4.1. Basic electrical parameters of type TTL IC (70). 3.4.2. Functional composition of TTL series (72). 3.4.3. Some features of using TTL type IC (78)
3.5. Emitter-connected transistor logic [ESTL] 83
3.5.1. Functional composition of the ESTL series (80). 3.5.2. Basic electrical parameters and typical characteristics of type ESTL IC (99). 3.5.3. Some features of applying type ESTL IC (103).

3.6. Digital IC made of MOS 109
3.6.1. Principle of IC operation with p-channel MOS transistors (111). 3.6.2. Static circuits with p-channel MOS transistors (113). 3.6.3. Quasistatic and dynamic circuits (116). 3.6.4. Principle of IC operation with complementary MOS transistors (119). 3.6.5. Basic IC series with MOS transistors (123).
3.7. Integrated circuits of memory units 130
3.7.1. Memory elements with bipolar transistors (131).
3.7.2. Memory elements with MOS transistors (134).
3.7.3. Memory elements with complementary MOS transistors (135).
3.7.4. Memory elements with MNOP transistors (136).
3.7.5. Memory elements with "silicon on sapphire (138).
3.7.6. Memory elements using new materials (138)
3.7.7. Basic IC memory units and their functional composition (141).
3.8. Perspectives of digital IC development 142
3.8.1. Integrated injection logic (143).
3.8.2. MOS circuits with n-channels (144).
3.9. Microcalculators 146
3.10 Microprocessors 149
3.10.1. Microprocessor characteristics (150)
3.10.2. Medium speed microprocessor set (153).
3.10.3. High speed microprocessor set (159).

Chapter 4

Analog integrated circuits 200
4.1. Purpose and application 200
4.2. Operational amplifiers 200
4.2.1. Operational amplifier with a two-stage circuit (207).
4.2.2. Amplifiers with field transistors at the input (214).
4.2.3. Amplifiers with super-beta transistors (215).
4.2.4. High current operational amplifier of the 153UD5 type (219). 4.2.5. Quick-acting operational amplifiers (221). 4.2.6. Micropower operational amplifiers (223).
4.3. Integrated comparators 227
4.4. Integrated analog multipliers 231
4.5. Analog IC for radio receivers 241
4.5.1. Differential amplifiers (243). 4.5.2. Low frequency amplifiers (UNCh) (244). 4.5.3. Specialized IC (248). 4.5.4. IC for designing selective devices (255).
4.6. IC for mutual conversion of digital and analog data 257
4.7. Analog switches 273
4.8. Integrated voltage stabilizers 278

Chapter 5 Page

Providing IC reliability when they are manufactured and installed in apparatus 293
5.1. Design-technological principles for high IC reliability 293
5.2. Operational monitoring 295
5.3. Rejection tests 295
5.4. Effect of external factors in apparatus manufacture 305
5.5. Forming and trimming leads 307
5.6. Tinning and soldering 313
5.7. Mounting IC on circuit boards 320
5.8. Protecting IC from electrical effects 323
5.9. Dismantling 329

Conclusion 331

2291
CSO: 1863/209

- END -