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USSR Report

CYBERNETICS, COMPUTERS AND AUTOMATION TECHNOLOGY

(FOUO 14/82)

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CONTENTS

HARDWARE

UDC 681.335.7

COMPONENT BASE OF HIGH-PERFORMANCE COMPUTER

Moscow VESTNIK AKADEMII NAUK SSSR in Russian No 3, Mar 82 pp 62-75

[Article by Corresponding Member of USSR Academy of Sciences K. A. Valiyev and Candidate of Technical Sciences A. A. Orlikovskiy]

[Text] One of the most important problems of modern computer equipment is development of powerful high-performance computers designed to solve important national economic and scientific research problems with minimum time expenditures.

The productivity of this computer system should reach one billion operations per second, which is guaranteed not only by innovations in computer configuration but also by development of high-performance large and superlarge integrated circuits (BIS and SBIS) for processors and memory systems, that is, the component base of the computer.

Three independent approaches to development of processor BIS and SBIS have now been established. First, this is development of specialized circuits--a large set of integrated circuits which cannot usually be used for processors of other types is developed for a specific processor.

Another approach is development of microprocessor modules that are low-digit processors (4, 8, 16 and so on) with microprogram software. The sphere of influence of microprocessors is extremely broad--from control systems of mechanisms to mini- and large computers. The processors of large computers can be developed on the basis of microprocessors with supplementary use of a number of circuits, usually of standard series of digital integrated circuits.

The third direction is development of matrix BIS and SBIS that are matrices of logic cells with multilayer connections. The first layer guarantees connection of transistors to the logic component. The second guarantees connection of several logic components to cells, for example, flip-flops. The third guarantees connection of cells to the circuit of the functional unit. In this case the nomenclature of the functional units based on a typical base crystal can be extensive and can number 200-500 circuits of different types. The second and third of these directions have been developed most intensively and the use of matrix BIS and SBIS is preferable for high-performance computers.

The component base of the internal memory of high-performance computers will be semiconductor BIS and SBIS of the internal (with random access), read-only (programmable) and associative memories.

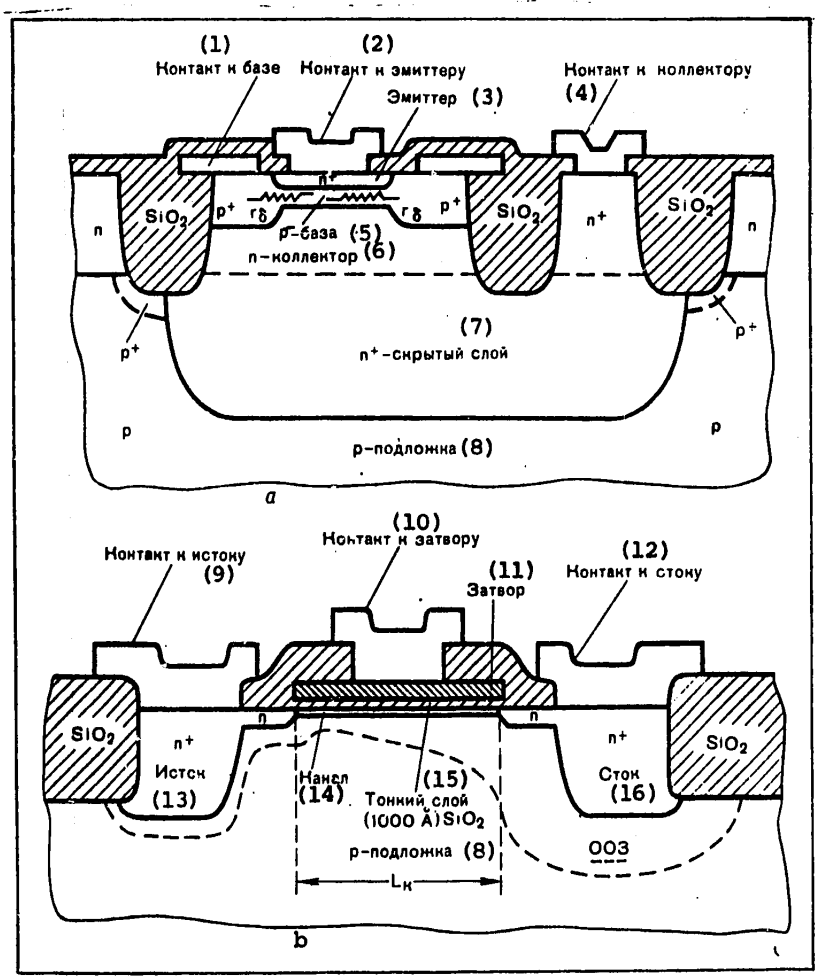

Figure 1. Structures of Bipolar (a) and MPD (b) Integrated Transistors: the bipolar transistor (a) is formed in a thin (approximately 1 μm) epitaxial layer. The base and emitter domains on the order of 0.3 and 0.15 μm thick, respectively, are created by ion implantation and diffusion methods. The MPD transistors with n-type channel (b) is developed by ion implantation to a high-resistance substrate. The domain of the channel is separated from the gate by a thin (less than 100 nm) layer of SiO_2. To eliminate spurious contacts between the transistors in the integrated circuit, each of them is surrounded by a layer of SiO_2. The length of channel L_k is limited due to the possible coupling of the channel and source space charge (003) domains with a value on the order of 0.1 μm /MPD - metal-dieletric-semiconductor/

[Key on following page]

[Key continued from previous page]

1. Contact to base
2. Contact to emitter
3. Emitter
4. Contact to collector
5. P^--base
6. n-collector
7. n^+-concealed layer
8. p-substrate
9. Contact to source
10. Contact to gate
11. Gate
12. Contact to drain
13. Source
14. Channel
15. Thin layer of (1,000 Å) SiO_2
16. Drain

The basic material of modern microelectronics is silicon. The two main varieties of silicon BIS and SBIS are determined by the physical principles of their design. These are bipolar and MPD transistors. Their structure, realizable in an integrated circuit, is presented in Figure 1. Amplification in bipolar transistors is based on control of base current by the value of the collector current and that in MPD transistors is based on control using the voltage on the gate through a thin semigate oxide with a value of channel current. Unlike MPD integrated circuits, bipolar integrated circuits have higher speed (by a factor of 2-10), but are inferior to them in the degree of integration, that is, by the maximum number of components located on the chip. Along with the use of silicon to create integrated circuits, the capability of using new materials having better electrophysical parameters than silicon is being studied extensively. One of these promising materials is gallium arsenide, in which electron mobility in weak fields is 2-5-fold higher than in silicon. This essentially permits one to achieve higher speed of transistors and circuits based on them.

The most important parameters of integrated circuits are the delay time per logic component t_z, the number of gates on the chip N and the power P consumed by the circuit. The power consumed by the chip is limited by the capability of heat dissipation in high-speed semiconductor circuits. Thus, the maximum dissipation with air cooling should not exceed 2 W per chip, while that with liquid cooling should not exceed 20 W. The relationship of output to the speed of the component is determined by the physical operating principles of the active instrument on the basis of which the circuit is constructed. These relations are basic in nature and will be considered with respect to specific devices.

One can assume in the first approximation that the delay time in a component is inversely proportional to output. Therefore, in attempting to achieve high speed, the developer is forced to restrict the power consumed by the chip by the number of components located on a single chip. It is obvious from these arguments that all three parameters are interrelated. Therefore, the quality of the logic component is usually characterized by switching energy $Pt_z/N = P_0t_z$, obviously dependent on all three parameters.

The two main channels of development of microelectronics are related in one case to achieving the maximum possible speed and is related in the other case to achieving the highest degree of integration. In the first case we will talk about very high speed integrated circuits (SSIS) and in the second case we will talk about very large integrated circuits (SBIS).

The capabilities of bipolar and MPD transistors are far from exhausted in both directions, but are limited by the minimum topological dimension. The evolution of the minimum topological dimension is illustrated by the curve presented in Figure 2. It is obvious from the figure that the minimum topological dimension in industrial production of integrated circuits now comprises approximately 3 μm, which is guaranteed by the methods of optical lithography. Taking into account that the resolution in formation of a drawing cannot be less that the wavelength of the light used for exposure, one can conclude that the efficiency of optical lithography is sharply reduced upon crossing the boundary of 1 μm. Methods of cathode-ray, ion-beam and X-ray lithography are being developed for industrial production of integrated circuits with minimum topological dimension of not more than 1 μm. The resolution is not directly related to the wavelengths of these emissions, but is limited by the effects of interaction of the radiation with matter. Along with development of precision methods of creating the drawing of devices and the connections between them, development of precision methods of microstructuring, specifically of methods of ion alloying of supersmall domains, ion and plasma etching[1] and so on, is required to achieve such small dimensions.

Main attention will be devoted in this paper to analysis of alternative directions for development of very high-speed integrated circuits--the component base of high-performance computer systems. Among these directions are bipolar and MPD-silicon integrated circuits, circuits based on field-effect transistors with Schottky barrier based on gallium arsenide and superconducting integrated circuits based on the Josephson effect, considered as the future base of supercomputers.

Components of Bipolar Integrated Logic Circuits

Let us return to the structure of a bipolar transistor (Figure 1, a). Side dielectric domains (SiO_2) that usually cover a thin (approximately 1 μm) epitaxial layer, are used to insulate the transistors in the integrated circuit. The transistors on the substrate are insulated from each other by a closed "concealed layer-substrate" p-n junction. The base and emitter domains are created by ion implantation and diffusion methods. The high speed of bipolar transistors in digital circuits is determined by the transit time of electrons τ_{pr} through the thin base (0.1-0.15 μm), the recharging time of the barrier capacitors of the p-n junctions and the accumulation and scattering time of the minority charge carriers in the domain of the base. Bipolar transistors in higher speed circuits do not operate in the saturation domain; therefore, the inertia related to accumulation and scattering in the base of electrons injected from the collector is eliminated. The high speed of this circuit is determined primarily by the length of recharging the barrier capacitors of the emitter ($C_{e.b}$) and collector ($C_{k.b}$) p-n junctions through the resistance of the base.

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[1] See: K. A. Valiyev, "Problems of Developing the Component Base of Very High Degree of Integration for Computers," MIKROELEKTRONIKA, Vol 9, No 6, 1980, p 483-490.

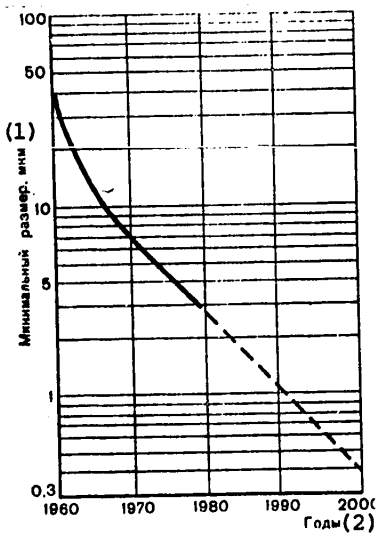

Figure 2. Variation of Minimum Topological Dimension in Integrated Circuits Limited by Capabilities of Lithography: The maximum capabilities of photolithography comprises approximately 0.5 μm when using a light source with wavelength of approximately 200 nm. The use of X-ray sources and electron and ion beams is required to create a drawing with the smallest possible topological dimension (0.1 μm)

Key:
1. Minimum dimension, μm
2. Years

The time constant of this process is

$$\tau_б = r_{э.б}(C_{э.б} + C_{к.б}). \quad (1)$$

The process of establishing the current in the collector is equivalent to the process of charging the co-called diffusion capacitor

$$C_{диф} \sim \tau_{пр} \cdot I_0/\varphi_т, \quad (2)$$

which is also charged through the resistance of the base with time constant

$$\tau_{диф} \sim r_б \cdot \tau_{пр} \cdot I_0/\varphi_т. \quad (3)$$

Here ϕ_t is the temperature potential and I_0 is the current switched by the logic component.

The output voltage is shaped on the load resistor in the collector circuit. The inertial of voltage variation on the load resistor is determined by the recharge time of the barrier capacitors of the "collector-base" junction ($C_{k.b}$) and "collector-substrate" junction ($C_{k.p}$) through the load resistor R_k. The constant of this process is

$$\tau_к = R_к(C_{к.б} + C_{к.п}). \quad (4)$$

Taking into account that the logic drop on the load resistor is

$$\Delta U_л \cong I_0 \cdot R_к, \quad (5)$$

the function of τ_k on current is easily found

$$\tau_к \cong \Delta U_л \cdot (C_{к.б} + C_{к.п})/I_0. \quad (6)$$

The time constants τ_b (1), τ_{dif} (3) and τ_k (6) are contained in the general expression for the delay time with some coefficients which are equal to unity by an order of magnitude. Without calculating the values of these coefficients, let us present the general form of function t_z (I_0) in Figure 3. Since the power consumed by the component $P_0 = I_0 U_{i.p}$ ($U_{i.p}$ is the voltage of the power supply source), then the dependence presented in Figure 3 is similar to the dependence of the delay time on consumed power P_0. It is rather general in nature and valid for any digital bipolar circuits. If the transistors in the circuit are contained in saturation, the delay is increased by the scattering time of the surplus electrons in the base, which is equivalent to the shift of the curve in Figure 3 to the domain of greater values of t_z.

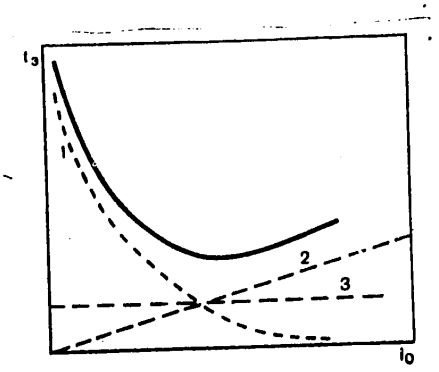

Figure 3. Dependence of Delay Time of Logic Component in Bipolar Transistors on Value of Switched Current: the dashed line indicates the dependence of some components of delay time on current: 1--time of voltage variation on collector in whose circuit the load resistor is connected to resistor R_k; 2--time of establishing the collector current, determined by the time of accumulation of electrons in the base injected from the emitter; 3--time of establishing the voltage on the "base-emitter" junction due to the effect of the input voltage generator in the circuit of the transistor base

It is clear from the given arguments that the values of the barrier capacitors $C_{e.b}$, $C_{b.k}$ and $C_{k.p}$, the resistances of the base body r_b and the transit time

of the electrons through the base τ_{pr} must be reduced to guarantee high speed of bipolar logic circuits. This is achieved by reducing the dimensions of the transistor in the plane of the chip. The resistance of the base is reduced by additional alloying along its periphery (see Figure 1, a). The value of constant τ_k is reduced by reducing the voltage of the power supply $U_{i.p}$ and of the logic drop ΔU_l.

Let us consider the experimental dependence of the time delay in the current switch on bipolar transistors[2] (Figure 4), which correspond to two types of transistors with emitters having an area of 1 X 3 μm and 2 X 5 μm and resistance of the base of 360 and 290 ohms, respectively. The logic drop was selected as equal to 450 mV. The depth of alloying the "emitter-base" and "collector-base" junctions was 0.15 and 0.30 μm, respectively. It is obvious from Figure 4 that the minimum values of the time delay comprised 0.29 and 0.39 ns at consumed power of 1.48 and 1.85 mW, which corresponds to values of the product $P_0 \cdot t_z$ 180 and 310 fJ.

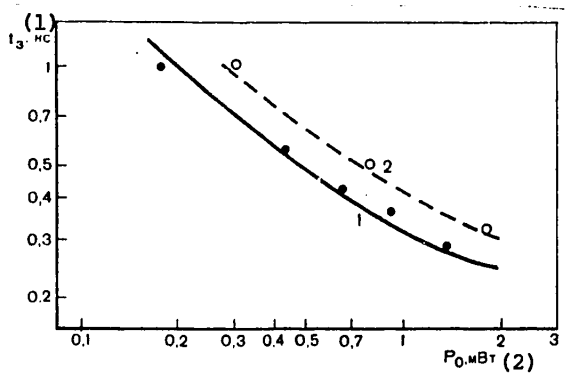

Figure 4. Experimental Functions of Time Delay in Logic Component Based on Bipolar Transistors: 1--corresponds to transistors with emitter having area of 1 X 3 μm; 2--with emitter having area of 2 X 5 μm

Key:
1. Nanoseconds
2. mW

The reserves for further reducing the delay time in bipolar logic components include reducing the value of the logic drop to approximately 4 ϕ_t, reducing the power supply voltage to values on the order of 1 V and reducing the barrier capacitors of the p-n junctions to values less than 10^{-14} F, which is quite achievable with minimum topological dimension of 1 μm. As indicated by estimates,[3] the delay time in bipolar logic components can be smaller than 10^{-10} s while the product $P_0 t_z$ can be less than 10^{-13} J.

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[2] See: H. Nakashiba, I. Ishida, K. Aomura and T. Nakemura, IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol SC-15, No 4, 1980, p. 455-459.

[3] See: A. A. Orlikovskiy, MIKROELEKTRONIKA, Vol 10, No 3, 1981 p 195-205.

Silicon Integrated Circuits With MPD Structure

The speed of a logic component based on MPD transistors is determined first by the inertia of channel formation in the connected transistor, that is, by the accumulation time of electrons injected from the channel and source domains in the channel and, second, by the recharge time of the total load capacitor, consisting of the self-capacitances of the transistors which form the logic component and the input capacitances of the following logic stages. The storage time of the basic carriers in the channel is short. It is equal to Maxwell relaxation time by an order of magnitude. Therefore, one can assume in the first approximation that

$$t_з \sim C_н \cdot U_{н.п.}/I_0 \tag{7}$$

and the product

$$t_з P \sim C_н \cdot U_{н.п.}^2 \tag{8}$$

Here, as before, $U_{i.p}$ is the voltage of the power supply source and I_0 is the switched current. The logic drop is $\Delta U_1 = U_{i.p}$ in the considered circuits with MPD structure.

The proportionality of $t_z \cdot P_0$ to the square of the power supply voltage has been confirmed experimentally.

Taking into account that the current of an MPD transistor (see Figure 1, b) is proportional to its transconductance and by expressing the transconductance by the "gate-channel" capacitance C_0, the electron mobility in channel μ_p and the length of the channel L_k, we find the expression for the delay time

$$t_з \sim \frac{C_н}{C_0} \cdot \frac{L_к^2}{\mu_н}. \tag{9}$$

It is obvious from (9) that, by keeping the ratio C_n/C_0 constant, one can reduce t_z by reducing the length of the channel L_k. Therefore, when developing SSIS, one must guarantee the maximum possible short lengths of the channels of MPD transistors. The parameters of MPD logic components for L_k = 1 μm are presented in Table 1, where data on bipolar logic components with the same minimum topological dimension are also reported.

Table 1. Parameters of Higher Speed MPD and Bipolar Logic Components[4] for Minimum Topological Dimension of 1 μm

Parameters	Bipolar Component	MPD-Component
t_z, ps		
at N_n = 1	70	115
at N_n = 4	115	230

[Continued on following page]

[4] See: P. A. H. Hart, T. Van't Hof and F. M. Klassen, IEEE TRANSACTIONS, Vol ED-26, No 4, 1979, pp 421-429.

[Table continued from preceding page]

Parameters	Bipolar Component	MPD-Component
$P_0 t_z$, fJ at N_n = 1		
Minimum dimensions:		
Emitter	1 X 2.5 μm	--
Width of contact to base	1 μm	--
Effective length of channel	--	0.5 μm
Length of gate	--	1 μm

Note. N_n is the number of identical logic components connected to the output of the component being investigated.

It is obvious from the table that a bipolar logic component has the highest speed with equal energy expended for switching and with identical minimum dimension, while the advantage with respect to the MPD component becomes a multiple of 2 as the number of loads increases to 4.

As can be seen from (9), the additional capacity of increasing the speed of MPD components includes the use of MPD transistors with cavity channel. The channel in these devices is arranged in the semiconductor where electron mobility can be 2-3-fold higher, rather than in the surface of the domain. The lowest achieved delay time[5] for a logic component based on MPD transistors with micron cavity channel comprised 72.5 ps at P_0 = 43 mW per component, which corresponds to $P_0 \cdot t_z = 3.15 \cdot 10^{-12}$ J.

Unlike bipolar components, the delay time in MPD-components is inversely proportional to the power supply voltage. This is explained by the fact that the current to be switched $I_0 \quad U_{i.p}^2$ since the current of the MPD transistor in the sloping part of its characteristics is proportional to the square of the voltage on the gate with respect to the source. Taking this into account, we find from (7) that

$$t_a \sim C_{\text{н}}/U_{\text{н.п}}. \tag{10}$$

Therefore, record low values of delay time have been experimentally at power supply voltages of 10-14 V, unlike values of 3.3-5.2 V in bipolar circuits. It follows from (8) and (10) that the power consumed by an MDP-component increases in proportion to $U_{i.p}^3$ as $U_{i.p}$ increases. This feature of MDP-components can hardly be regarded as favorable for design of SSIS based on them.

A significant decrease of the "source-substrate" and "channel-substrate" capacitances is achieved in the "silicon on sapphire" structure. This permits one to reduce the delay time by reducing the value of C_n. The experimental

[5] See K. Nishiuchi, H. Shibayama, T. Nakamura et al, IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol SC-15, No 5, 1980, pp 809-816.

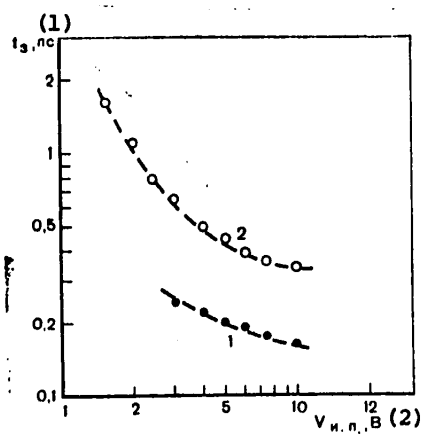

Figure 5. Experimental Dependence of Delay Time of Logic Component Based on MDP-Transistors on Power Supply Voltage for Transistors with Different Lengths of Channels

Key:
1. ps
2. V

dependence of t_z on power supply voltage is presented in Figure 5. As can be seen, a delay time of 200 ps is achieved with power supply voltage of 5 V and L_k = 0.5 μm. The minimum delay of 170 ps is achieved with power supply voltage of 10 V. An attempt to develop devices with channel length of 0.3 μm did not lead to an increase of the speed of the component since it became necessary in this case to reduce $U_{i.p}$, the value of which is limited due to the effect of coupling of the space charge domains (OOZ) of the "source-substrate" and "channel-substrate" p-n junctions. Thus, the maximum speed is achieved in silicon MDP-components in "silicon on sapphire" structures with minimum topological dimensions of 0.3-0.5 μm and with sufficiently high power supply voltages (approximately 10 V).

Very High-Speed Integrated Circuits Based on Gallium Arsenide

Gallium arsenide has a number of advantages over silicon. First, it has higher electron mobility in weak fields (3,500-7,000 $cm^2/V \cdot s$) and higher maximum drift velocity of electrons ($1.5 \cdot 10^7$ cm/s). Second, gallium arsenide has a wider forbidden zone (1.52 eV), which permits one to produce high-resistance material (up to 10^8 ohms·cm), which has excellent dielectric properties and can be used in insulating substrate for an integrated circuit.

Interest in gallium arsenide as a material for integrated circuits arose during the early 1970s with regard to the attempt to develop very high-speed integrated circuits based on Gann devices in thin epitaxial layers and later with regard to the capability of producing planar Schottky field-effect transistors in gallium arsenide. The Schottky field-effect transistor in modern integrated circuits based on gallium arsenide is the basic component.[6] The

[6] See: K. A. Valiyev, L. N. Kravchenko, A. A. Orlikovskiy et al, MIKROELEKTRONIKA, Vol 5, No 5, 1976, pp 378-392.

structure of a Schottky transistor is presented in Figure 6. This structure is realized by using promising processes of ion implanatation (double Se^- and S^- ions) in a high-resistance substrate (i-GaAs), electronic lithography and plasma or ion methods of etching. This essentially permits one to realize the submicron dimensions of the channel and gates between the gate and resistance contacts to channel and source domains.

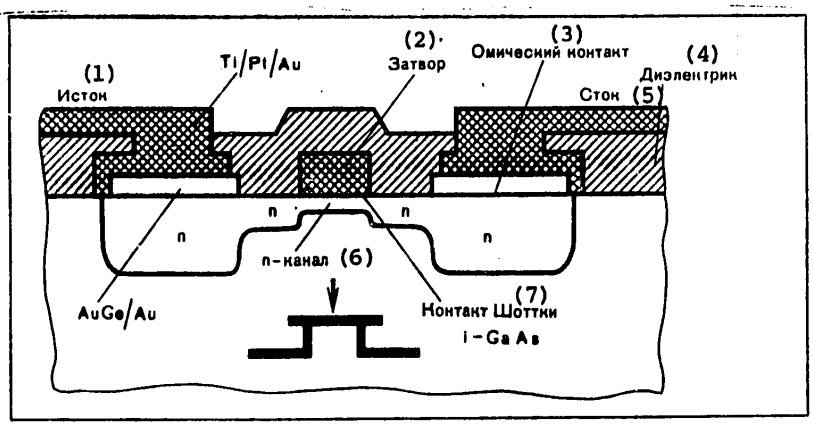

Figure 6. Structure of Field-Effect Transistor with Metal Gate Formed with Domain of Schottky Contact Channel

Key:
1. Source
2. Gate
3. Resistance contact
4. Dielectric
5. Channel
6. n-channel
7. Schottky contact

With electron concentration in the channel on the order of 10^{17} cm^{-3}, the thickness of the space charge domain in a Schottky diode is equal to 0.1 m by an order of magnitude under equilibrium conditions. The thickness of the channel in a field-effect transistor should be the same. Development of such thin homogeneous high-quality layers by the epitaxy method is clearly problematical; therefore, it is preferable to use ion alloying.

The inertia of a "gate-channel" Schottky diode is determined by the product of the barrier capacitance of the gate by the resistance, which consists of the resistance of the channel and source, including the resistance of the ohmic contacts. Therefore, one attempts to reduce the length of the channel L_k and the dimensions of the gaps between the gate and contacts to the channel L_s and source L_i and to increase the degree of alloying of the channel (up to 10^{17} cm^{-3}).

If one assumes that the resistance of the channel and source are equal to zero, the time of switching an "ideal" field-effect transistor is determined as

$$t_з \approx \Delta Q / I_0. \tag{11}$$

Here ΔQ is charge variation under the gate and I_0 is the current to be switched.

According to estimates,[7]

$$t_з \approx \frac{L_к + 2h}{v_s}, \tag{12}$$

where h is the thickness of the channel and v_s is the maximum velocity of electron drift in weak fields, equal to approximately $1.5 \cdot 10^7$ cm/s. It is easy to see that t_z is equal to 10^{-11} s by an order of magnitude at L_k = 1 μm and h = 0.1 μm. The value of t_z decreases to $3 \cdot 10^{-12}$ s with a decrease of L_k to 0.2 μm. This estimate may be assumed maximum for a delay time of switching a field-effect transistor.

Circuits based on normally closed transistors in which the channel current is equal to zero with zero voltage on the gate with respect to the source, have the lowest energy expended for switching among the different types of circuits based on Schottky field-effect transistors. This circuit engineering also has greater simplicity with minimum dimensions of L_k < 0.5 m--the lowest speed due to lower values of capacitances introduced by the connections between transistors.

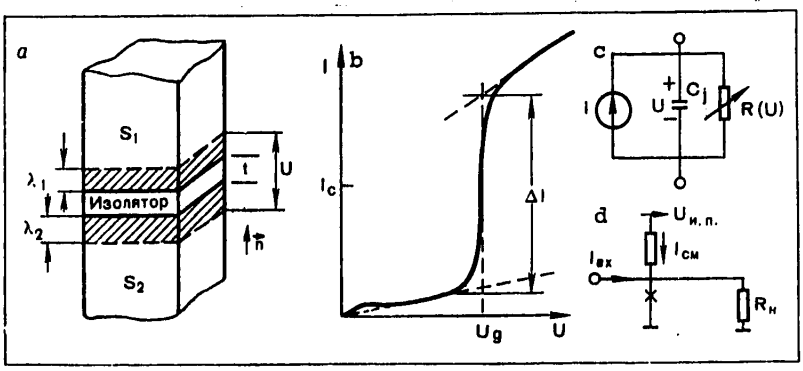

Figure 7. Josephson Tunnel Junction: a--structure of tunnel junction between two superconductors S_1 and S_2 separated by thin dielectric layer (t ≈ 1 nm); b--volt-ampere characteristic of Josephson junction; c--equivalent circuit; d--circuit of simplest switch based on Josephson device with tunnel junction

With the dimensions L_k = 1-2 μm now achievable, the highest speed is achieved in circuits based on normally open transistors due to the high currents that

[7] See V. I. Starosel'skiy, L. N. Kravchenko and A. N. Sapel'nikov, MIKROELEKTRONIKA, Vol 9, No 5, 1980 pp 387-400.

guaran ee recharging of the "gate-channel" capacitor. The typical parameters of logic components now achievable at L_k ~ 1 μm in logic components based on normally open and normally closed field-effect transistors are presented in Table 2.

Table 2. Typical Parameters of Components of Logic Integrated Circuits Based on GaAs with Minimum Length of Channel of 1 μm

Parameters	On Normally Open Transistors	On Normally Closed Transistors
Delay time t_z, ps	90	700
Consumed power P_0, mW	20	0.15
Logic drop ΔU_1, V	2.5	1
$P_0 t_z$, pJ	1.8	0.1

Gallium-arsenide integrated circuits with medium degree of integration (frequency dividers, counters, ring generators and so on) are now going through the stage of development and testing. Development of large SSIS based on GaAs becomes possible after industrial assimilation of production of high-resistance substrates and the technology of normally closed field-effect transistors with minimum dimension of the gate less than 0.5 μm, which will make it possible to achieve $t_z \approx 5 \cdot 10^{-11}$ ps at $P_0 t_z \approx 10^{-10}$ to 10^{-13} J.

Taking into account that gallium arsenide has a number of disadvantages (high cost, comparatively low mechanical strength and plate diameter less than that of silicon by a factor of 2-3), one can assume that the economic factor becomes decisive when selecting gallium-arsenide or silicon circuits of the component base for modern development of large high-performance components. Gallium-arsenide circuits may become the main component base of the processors of supercomputers during the period 1985-1990.

Superconducting Integrated Circuits Based on Josephson Junctions

A Josephson junction is an almost ideal switch with a sharp threshold, supersmall switching delay (10^{-11} s) and very low dissipation (10^{-6} W).

The main Josephson device, on the basis of which some types of logic circuits have been studied, is the tunnel junction containing two superconducting layers S_1 and S_2. They are separated by a thing insulating layer with thickness t (Figure 7, a) in which exchange of Cooper pairs between superconductors is possible. As a result, when the voltage on the junction is equal to zero, the current of the Cooper pairs I_c can pass through it and in this case the junction can be in two states--with voltage U = 0 and current $I \leq I_c$ and with finite resistance (with single-frequency tunnelling) in which the voltage proportional to the sum of the widths of the slits of the superconductors $\Delta_1 + \Delta_2$ drops.

The well-known Josephson equations are easily valid for this type of junction

$$I = I_c \sin\varphi, \qquad (13)$$

$$U = (\hbar/2e)\,\partial\varphi/\partial t. \tag{14}$$

$$\operatorname{grad}\varphi = (2e/\hbar)\cdot(\lambda_1 + \lambda_2 + t)\cdot(\mu_0 \mathbf{H} \times \mathbf{n}). \tag{15}$$

Here ϕ is the phase difference of f_1 and f_2 wave functions in superconductors S_1 and S_2, U is the potential difference, λ_1 and λ_2 are the London lengths of penetration for superconductors S_1 and S_2, H is the vector of magnetic field intensity, n is the unit vector, μ_0, e and h is the magnetic permeability, electron charge and Planck's constant. Piecewise linear approximation of the volt-ampere characteristic of the juncion is used for analysis of the logic circuits (Figure 7, b). The slope of the first segment is determined by the resistance $R_j = U_m/I_c$ and the slope of segment 2 is assumed equal to zero with current drop ΔI at voltage of $U_g = (\Delta_1 + \Delta_2)/e$. For example, the typical parameters are I_c = 50 μA, U_m = 27 mV, U_g = 2.8-2.9 V and ΔI = 70 μA for tunnel junctions 2.5 μm in diameter (based on Pb alloys). This junction is an equivalent circuit (Figure 7, c) with current generator

$$I = I_c \sin \int (2e/\hbar)\, U\, dt, \tag{16}$$

shunted by capacitor C_j and nonlinear resistor R(U). For the example presented here, C_j = 0.2 pF, which corresponds to approximately specific capacitance of 10^{-5} F/cm^2.

The Josephson tunnel junction is used in logic circuits as the threshold device controlled by current. Calculations show that the simplest switch based on a single Josephson tunnel junction (Figure 7, d) with the parameters presented above drops as a result of switching current with delay $5\cdot10^{-12}$ s to the load R_n at power supply voltage of $U_{i.p}$ = 10 mV, bias current I_{sm} = 35 μA and input current I_{vkh} = 35 A and dissipates power of $0.35\cdot10^{-6}$ W, which corresponds to an energy of $1.75\cdot10^{-18}$ J expended on switching. These values are better than the corresponding values for semiconductor integrated circuits. The low logic drop (approximately 1 mV) determines not only the low level of dissipation, but also the high speed since it permits one to use low load resistances (approximately 10 ohms).

However, the circuit shown in Figure 7, d cannot be used as a logic component since the output is not determined from the input and the component has poor load capacity ($N_n \approx 1$) due to the technological difference of current I_c.

Two directions were formulated to develop logic components with tie-in of the inputs and high load capacity ($N_n \geq 3$).

SKVID (Superconducting quantum interference devices), which are a combination of two or three Josephson junctions, are used in the first of them. The input line is connected to the SKVID by a magnetic flux. These components are called components with magnetic coupling.

The main disadvantages of logic components with magnetic coupling based on SKVID includes the relatively large area occupied by them on the chip and the high sensitivity to external random magnetic fields. If the minimum topological dimension is 2.5 μm, a logic component based on a three-junction SKVID

occupies an area of 4,400 μm^2, and approximately 80 percent of its area is occupied by inductive components.

An alternative method of coupling is to use Josephson devices in the input circuits as nonlinear uncoupling components.

Both magnetic and direct couplings are realized in the higher speed logic components based on Josephson devices that utilize the phenomenon of quantification of the magnetic flux in SKVID. The typical area of these components is approximately one-third less than the area of components with inductive couplings. A delay in the range of $(3\text{-}4)\cdot10^{-11}$ with minimum topological dimension of 2.5 μm and consumed power equal to approximately $5\cdot10^{-6}$ W per component is achieved in these components.

By comparing the record results achieved with silicon and gallium arsenide logic components with minimum dimension of 1 μm to the results found for components based on Josephson junctions with minimum dimension of 2.5 μm, one can see that components based on Josephson junctions have one-half the values of the delay time and are characterized by lesser energy expended for switching (10^{-16} J) by more than a factor of 2.

However, it would be erroneous to assume that all problems of developing SSIS on the basis of Josephson components have been solved. Producing tunnel junctions is a complex technological problem due to the need to guarantee high reproducability of a thin dielectric layer (3 nm) by tunnelling. The integrated structure of a circuit based on Josephson components together with the shielding superconducting layers has 10-12 thin-film layers.

Therefore, along with Josephson tunnel junctions, so-called bridge junctions are being studied intensively. A section with weak superconductivity, which is a thin "bridge" between two superconducing shores (Figure 8), is used in these devices instead of the tunnel barrier. Niobium with T_c = 8.9 K, the thin layer (0.1 μm) of which is applied to a silicon substrate, is used as the superconductor in the example in Figure 8. Thinning in the film is created by the electronic lithography and plasma or ion etching method. It is desirable in this case to achieve a length of the microbridge of $l < \xi$, where ξ is the length of coherence. The value of ξ is usually approximately 10 nm. For example, ξ = 25 nm in niobium at T = 4.2 K. Achieving these dimensions in the plane of the chip is still extremely difficult. As shown by K. K. Likharev, characteristics similar to those of ideal bridges can be observed in microbridges with length l, for which the following condition is fulfilled

$$\xi \ll l \leqslant \lambda_{\text{эф}}, \qquad (17)$$

where $\lambda_{ef} = \lambda\cdot\coth(d/2\lambda)$, d is the thickness of the bridge and λ, as before, is the London length of penetration.

To increase the logic drop in microbridges, one attempts to reduce the cross-section of the bridge and thus to increase its resistance in the nonsuperconducting state (R_N). The IBM Company, for example, has developed microbridges with record small dimensions (30 X 30 nm) based on niobium.

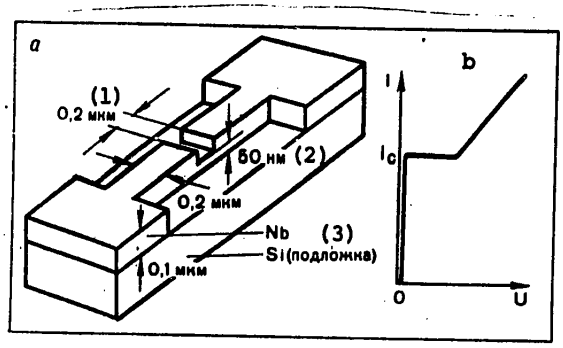

Figure 8. Josephson "Bridge" Junction: a--structure of device manufactured from niobium on silicon substrate; b--volt-ampere characteristic of junction.

Key:
1. μm
2. nm
3. Substrate

Another direction of research is to develop tunnel junctions with thick barrier (approximately 100 nm) from a degenerate semiconductor or normal metal. Weak induced superconductivity is observed in these junctions in degenerate semiconductors in the domain on the order of the length of coherence of the semiconductor. Narrow-zone materials, for example, InSb and InAs, in which the carriers are not frozen at helium temperatures and have mobility on the order of 10^6 cm^2/Vs, are of great interest for these junctions. Thus, the problem of selecting the component base for a Josephson supercomputer cannot be considered solved.

The systems engineering problems are of organizing processor and storage subsystems have not yet been solved for supercomputers based on Josephson components. The development of supercomputers will be preceded by development of small test Josephson computers. According to estimates, the test minicomputer based on Josephson components will include 50 SSIS of $5 \cdot 10^3$ components in each and a memory with capacity of $64 \cdot 10^3$ bits. The computer[8] will consume a power of approximately 1 W and will occupy a volume of (3 X 3 X 3) cm^3.

According to estimates available in the literature, supercomputers based on Josephson devices will contain a processor on 10^6 logic components, a high-speed memory with capacity of 64 kbytes and main internal storage with capacity of 64 or 128 Mbytes. The processor can be made in the form of 10^3 chips of 10^3 components each, SOZU (high-speed memories) of 32 chips of 16 kbits each and an OZU [internal storage] of $8 \cdot 10^3$ or $16 \cdot 10^3$ chips of 64 kbits each.

[8] See: S. Hasuo, H. Suzuki, T. Imamura and T. Yamaoka, Proceedings of the 12th Conference on Solid-State Devices, Tokyo, 1980, in JAPAN INSTITUTE OF APPLIED PHYSICS, Vol 20, No 20-1, 1981, pp 323-329.

The chips can be located on 100-200 square silicon cards with side of 10 cm. The cards in turn are connected to a single block measuring 15 X 15 X 15 cm. The total dissipation of the computer may be equal to 10 W. Realization of this computer requires development of digital systems equipment and technology of SSIS based on Josephson components, development of the technology of assembly of SSIS into blocks, protection of the computer against external noise and cooling supercomputers to helium temperatures.

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REDUNDANCY OF FINITE AUTOMATA IN UNIFORM COMPUTING ARRAYS

Moscow AVTOMATIKA I TELEMEKHANIKA in Russian No 4, Apr 82 (manuscript received 12 Mar 81) pp 139-149

[Article by G.G. Asatiani and V.G. Chachanidze, Moscow]

[Excerpts] A computer algorithm is discussed for global redundancy of finite automata in uniform computing arrays (UCA's) with the existence of faulty cells in them. The method provides an acceptable solution by means of a practicable exhaustive search. The solution sought is arrived at by using an almost twofold smaller number of redundant UCA cells than with other known methods.

1. Introduction

Uniform computing arrays (UCA's) are promising facilities for constructing computers of various classes and for various purposes [1-3].

One problem of designing automation and computer hardware facilities based on UCA's resides in the development of methods of providing redundancy of finite automata in UCA's. By providing redundancy of finite automata in UCA's we mean the process of reordering the array for the new implementation of a specific finite automaton while bypassing faulty cells, whose coordinates have been determined at the testing stage. Traditional methods of providing redundancy of finite automata are not very acceptable for solving this problem, since by their means it is difficult to take into account the arrangement of the elements and interelement links of a UCA. Of interest chiefly are redundancy methods which can be implemented by fairly simple systems for automatic restructuring of a UCA, i.e., methods which make it possible to produce a new adjustment program by uncomplicated transformations of the original program; in mind here is the fact that methods exist for inserting an arbitrary graphic representation of a specific finite automaton in a UCA with faulty cells [4].

In implementing finite automata based on UCA's, because of the existence of topological restrictions on the arrangement of cells in the structure, a certain number of cells in good working order are usually contained in the structure, positioned both in the section of implementation of a finite automaton and outside it and not

taking part in implementation of a finite automaton, i.e., a UCA is characterized by the existence of natural redundancy [5]. Conventional methods of providing redundancy in a UCA either introduce artificial redundancy into the structure (local redundancy methods), i.e., are similar to traditional methods of providing redundancy [6], or utilize just the natural redundancy of the array (global redundancy methods) [7]. In connection with this, conventional methods of providing redundancy in the first instance work with high redundancy factors, and in the second are ineffective because of the small amount of redundancy employed, which is not always sufficient for finding the UCA reordering program sought.

The purpose of this paper is to study and develop a computer method of providing redundancy of finite automata in a UCA, taking into account reduction of time and the redundancy factor, as well as limitations on moving the structural diagrams of finite automata over the UCA's field.

Use of the algorithm suggested presupposes, in the detection of faulty UCA cells at the testing stage, the single reordering on another computer of all statements implemented in the structure.

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CHOICE OF THROUGHPUT OF PROCESSOR SERIES IN DESIGNING FAMILY OF SPECIAL-PURPOSE COMPUTING SYSTEMS

Moscow AVTOMATIKA I TELEMEKHANIKA in Russian No 4, Apr 82 (manuscript received 18 Dec 80) pp 150-159

[Article by V.A. Vedeshenkov, N.A. Vlasenko and A.F. Volkov, Moscow]

[Excerpts] The problem is solved of determining the throughput of a series of processors intended for designing a family of special-purpose multiprocessor computing systems. The cost/throughput ratio is used as the optimality criterion for various variants of the design of central units of multiprocessor systems. An algorithm is developed which makes it possible to solve the problem.

In designing automated systems for controlling entities or processes of the same type, special-purpose computing systems are often necessary, having various processor capacities, information input/output facility capacities and memory capacities. Furthermore, economic requirements dictate that both the principles of the structural design of these computing systems and the principles of the structure of their software be identical. A promising way of creating such a series of special-purpose computing systems is their implementation in the form of multiprocessor systems. The fact that in recent years a new elementary computer hardware base--microprocessors--has appeared speaks in favor of using this method of designing special-purpose systems. Microprocessors, which have relatively limited computing capabilities, make it possible by uniting them into multiprocessor systems to create sufficiently large-capacity computing complexes.

An important characteristic of multiprocessor computing systems is their basic modularity. Because of this it is possible to construct on the basis of a single set of functional modules computing systems which, although of identical structure, nevertheless differ in the throughput of their central units, memory capacities and carrying capacities of input/output facilities. By the term "central unit" is meant the combination of general-purpose processors. Of course, an increase in the number of functional memory modules and input/output processors results in practically a linear increase in the respective capacities of the special-purpose system. However, increasing the number of general-purpose processors in the central unit does not produce a linear increase in throughput [1-3]. This fact is explained by the following reasons.

1. By conflicts in the simultaneous access of several processors to their facilities for linking with memory modules. The probability of such conflicts is especially great if a shared line, which is typical of multimicroprocessor systems, is used as the communication facility.

2. By conflicts in access of processors to the same memory modules. Losses of the central unit's throughput are thereby inevitable, since the majority of problems solved in a special-purpose multiprocessor system are heavily related in terms of initial data.

3. By the impossibility of completely loading with assignments all processors of the system at any moment of time. This takes place on account of the limited capabilities for multiprocessing of problems solved in the system. Multiprocessing capabilities are especially limited in high-reliability multifunctional computing systems.

In developing multiprocessor computing systems oriented toward functioning in the control circuits of ASU's [automated control systems] for entities of the same type, the requirements for the real throughput of central units of systems, first, are known, and, second, differ strongly from one another. Therefore, the problems of determining the optimum values of the throughput of various types of processors from which central units are made up and of determining the number of processors of a specific type in specific configurations of computing systems satisfying specific requirements are of interest. This study is devoted to solving these problems. Here the "cost/throughput" ratio is used as the optimality criterion for different variants of the design of central units of multiprocessor systems.

The results of solving this problem according to the algorithm presented are shown in the table [not reproduced]. It is obvious from the data of this table that for fulfilling the problem's conditions it is necessary to use three types of basic processors. Here the breaking down of requirements into groups is performed in the following manner: $\{Q_1\}$, $\{Q_2\}$, $\{Q_3, Q_4\}$, and the total percentage loss for this variant of designing central units as compared with the optimum solution equals 10 percent.

For the purpose of comparison, in the last section of the table analogous data are presented for the implementation of all required central units in single-processor variants. The advantages of multiprocessor organization of central units of computing systems are clearly evident from comparing these data with the data of other variants of their implementation.

The use of the method developed for determining the throughput of general-purpose processors and their number in central units of computing systems makes it possible to make a valid choice of the structure of central units at their rough design stage. Because of this, designing time is shortened and the quality of design solutions is improved.

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FORMALIZED APPROACH TO OPTIMIZATION OF INTERNAL CONFIGURATION OF MICROCOMPUTERS

Riga AVTOMATIKA I VYCHISLITEL'NAYA TEKHNIKA in Russian No 2, Mar-Apr 82 (manuscript received 15 Oct 80) pp 15-19

[Article by L. Ya. Lapkin and V. G. Nosov]

[Text] One of the directions of microcomputer development is development of them on the basis of the processor sections of multicrystal microprocessors (MP) with microprogram emulation of some authoritative instruction system. Analysis of the literature shows that the given direction of microcomputer design is achieving ever greater development. The internal configuration of a microcomputer designed on the basis of microprocessors--a set of series K589 and compatible with the M-6000 minicomputer--is described in [1] and a microcomputer developed on the Intel 3000 microprocessor set and program-compatible with the series of PDP-11 minicomputers of the DEC Company, is described in [2] and the design features of a microcomputer compatible with the YeS EVM [Unified Computer System] are described in [3].

The role of microprograms will increase sharply in development of microcomputers with the use of microprocessors and microprocessor sets. Microprograms in combination with microprogrammable microprocessors provide great capacilities to the developer for selecting the internal configuration of the microcomputer being designed. The developer can follow different goals in selection of the internal configuration as a function of the postulated design problem: design of a general-purpose microcomputer or design of a microcomputer oriented toward a specific class of algorithms. The purpose of the given paper is to develop a formal method of optimizing the internal configuration of microcomputers.

When developing the configuration of microcomputers, the designer solves the traditional problem of resource distribution of the microcomputer being designed between the hardware and microprogram levels. On one hand, the characteristic features of the instruction system being emulated are taken into account and on the other hand the results of analyzing the realized algorithms and restrictions placed on the microcomputer being designed in the volume of equipment, productivity, weight, consumed power, reliability, cost and so on are taken into account.

Let us call the aggregate of functional assemblies of a microcomputer, the communications between them and the corresponding microprograms the internal configuration of a microcomputer.

Let us also introduce the concept of features of internal configuration that determine the elementary functions (indivisible at the selected level of consideration) of a microcomputer which can be realized by hardware or microprograms and from which the "configurational" appearance of the microcomputer is made up.

The set of features of the internal configuration is determined, on the one hand, by the selected instruction system and on the other hand, by the selected type of microprocessor.

Features can assume different values. If the set of microcomputers under consideration with different configuration is denoted by the letter A and if the number of the configurations is denoted by the letter N, then each configuration is assigned its own number $i = 1, 2, \ldots, N$ and the values of all its features. In the considered case the features x may assume three values:

$$A_x = \begin{cases} 0, \text{ if the function is fulfilled by microprograms;} \\ 1, \text{ if the function is fulfilled by hardware;} \\ y, \text{ if the function is not included in the configuration.} \end{cases}$$

The representation $x: A \to A_x$ that compares the value $x_i \in A_x$ to each object $A_i \in A$ is understood as a feature. The problem of selecting the internal configuration of a microcomputer with fixed set of functions for all versions of the configuration is subsequently considered. Feature x in this postulation assumes only two values {0, 1} from set A_x and is a boolean variable.

The versions of the internal configuration of a microcomputer having m features are determined by the set of vectors $\{X_i\}$ of features of the internal configuration, where $X_i = (x_{1i}, \ldots, x_{mi})$. The vector of features of the internal configuration will be denoted $X = (x_1, \ldots, x_j, \ldots, x_m)$ for simplicity.

Each feature of the internal configuration x_j, $j = \{\overline{1, m}\}$, is characterized by the time of microprogram realization τ_j and by the equipment expended for its hardware realization q_j. The time estimate of the feature is found at the microprogramming stage by determining the product of the number of microinstructions fulfilled in realization of the given feature and the time of the machine cycle. Parameter q_j is determined by the number of housings of integrated circuits (IS) expended for hardware realisation of the feature.

Let us introduce the time and hardware expenditure vectors: $T = (\tau_1, \ldots, \tau_m)$ and $Q = (q_1, \ldots, q_m)$.

Let a system of instructions of a microcomputer $K = \{k_1, \ldots, k_i, \ldots, k_n\}$ be selected for which the communication matrix $M = \{m_{ij}\}$ is determined,

$$m_{ij} = \begin{cases} \tau_j, & \text{if the functional transformation assigned by the j-th feature is fulfilled in instruction } k_i \text{ by microprogram;} \\ 0 & \text{in the opposite case.} \end{cases} \quad (1)$$

The times of fulfillment t_i of instructions k_i for a selected value of X are determined by the formula

$$\begin{pmatrix} t_1 \\ \vdots \\ t_n \end{pmatrix} = M\bar{X},$$

where $\bar{X} = (1-x_1, \ldots, 1-x_j, \ldots, 1-x_m) = (\bar{x}_1, \ldots, \bar{x}_j, \ldots, \bar{x}_m)$.

Let us also introduce the vector X_T--the transported vector X. The effective productivity of the microcomputer is determined by the formula

$$W_{эф} = \frac{1}{\sum_{i=1}^{n} f_i t_i}, \quad (2)$$

where f_i is the frequency of using the i-th instruction in realization of the algorithm fulfilled by the microcomputer.

A Gibson mixture is used when calculating W_{ef} of a general-purpose microcomputer [4] and the specifics of the problems being solved by it are taken into account when designing a problem-oriented microcomputer.

Let $F = (f_1, \ldots, f_n)$, then the mean time of performing the operation is

$$\frac{1}{W_{эф}} = F \cdot M \cdot \bar{X}. \quad (3)$$

Let vector X contain only "changed" features, i.e., those which can assume both a unit and zero value. Let us denote by τ_{j0} the times of fulfilling the functions corresponding to the unchanged features that assume only a zero value and let us denote by j_0 the number of the unchanged feature. The time of fulfilling instruction k_i can then be expressed by the formula:

$$t_i = \sum_{j_0} m_{ij_0}\tau_{j_0} + \sum_{j=1}^{m} m_{ij}\tau_j\bar{x}_j = t_i^0 + \sum_{j=1}^{m} m_{ij}\tau_j\bar{x}_j. \quad (4)$$

Here t_i^0 is the time of fulfilling the "core" of the instruction--the part of it which is always fulfilled on a microprocessor by feeding the corresponding microinstructions with any version of configuration.

Taking (4) into account, one can write (3) in the form

$$\frac{1}{W_{эф}} = T_0 + FM\bar{X}, \tag{5}$$

where $T_0 = F \cdot \begin{pmatrix} t_1^0 \\ t_n^0 \end{pmatrix}$ is the time of realizing the algorithms in the case when all the features of the internal configuration are realized by hardware.

Hardware expenditures to realize a microcomputer are determined by function Z:

$$Z(Q, X) = Q_0 + Q \cdot X_T, \tag{6}$$

where Q_0 is the minimum equipment expenditures for the version of internal configuration of the microcomputer being designed when all the features of the internal configuration are realized by microprogram.

Expressions (5) and (6), which yield estimates of the basic characteristics of the microcomputer, are linear functions of boolean variables x_j. The possibility of finding similar functions is determined by selection of independent features of configuration, by realization of microprogram control in the modern BIS [large integrated circuit] of the PZU [read-only memory], in which the PZU expenditures in microprogram realization of the features of configuration are incomparably lower than the expenditures for hardware realization of these features; the length of the machine cycle of the microcomputer is selected with regard to all the possibilities of introducing hardware that realizes the features of the configuration.

Based on (5) and (6), one can formulate the following problems of designing the internal configuration of a microcomputer, described by the vector $X = (x_1, \ldots, x_m)$, $x_j = 0$ or 1, $j = 1, \ldots, m$.

1. The problem of achieving the given productivity with minimum equipment expenditures. $Z = Q \cdot X_T \to \min$ and $FM\bar{X} \leqslant T_{dop} - T_0$. Here $T_{dop} = 1/W_{dop}$, W_{dop} is the requirement on the microcomputer being designed with respect to productivity.

2. The problem of achieving given productivity for applications of the microcomputer in several different systems with minimum equipment expenditures.

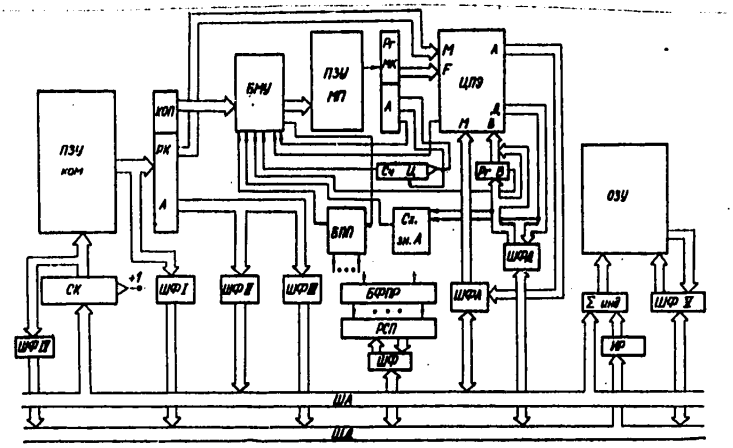
$$Z = Q \cdot X_T \to \min,$$

$$\begin{cases} F_1 M\bar{X} \leqslant T_{1доп} - T_{10}, \\ \vdots \\ F_k M\bar{X} \leqslant T_{kдоп} - T_{k0}. \end{cases}$$

Here $T_{k\ dop} = 1/W_{k\ dop}$, F_k is the requirements on the microcomputer and the characteristics of problems of the k-the system and $T_{k0} = F_k \begin{pmatrix} t_1^0 \\ \vdots \\ t_n^0 \end{pmatrix}$.

3. The problem of achieving maximum productivity with given restrictions on equipment. $FM\bar{X} \to \min$, $Z = Q \cdot X_T \leq Q_{dop} - Q_0$. Here Q_{dop} is the maximum permissible equipment of the microcomputer.

Thus, the problems of optimizing the internal configuration of a microcomputer can be reduced to problems of linear programming with boolean variables.



Block Diagram of Microcomputer. Functional assemblies: PZU kom--read-only memory of instructions; SK--instruction counter; RK--instruction register; ShF1, ShF2, ShF3 and ShF4--bus shapers for issue of information from corresponding functional assemblies; BMU--microprogram control unit; PZU mp--read-only memory of microprograms; RgMK--microinstruction register; TsPE--central processor element; SchTs--cycle counter; RgV--external shift register; ShFA--address bus shaper; ShFD--data bus shaper; ShA--address bus; ShD--data bus; OZU--internal storage; Σ_{ind}--index adder; IR--index register; ShF^5--OZU data bus shaper; BFPR--unit for forming result features; RSP--processor status register; BPP--piority interrupt unit

In real problems of microcomputer design, the number of features of internal configuration may exceed 10-20, which makes it impossible to solve the indicated problems by direct selection and determines the necessity of using standard programs that solve linear programming problems with boolean variables by the Balash method [5] or by other methods [6, 7].

As an example, let us consider the internal configuration of a microcomputer designed on a microprocessor set of series K589 and that is program-compatible with computers of the SM EVM series. A block diagram of the computer is presented in the figure. The functional assemblies SK, SchTs, Skh.zn.A, RgV, Σ_{ind}, IR and BFPR are hardware realization of the features of internal configuration of the microcomputer.

Development of the indicated microcomputer with regard to the specifics of problems of processing information coming in from analytical devices permits one to establish the following characteristics for solving linear programming problems: 1) $Q_0 = 45$, 2) $F = (f_1, f_2, f_3, f_4, f_5, f_6) = (0.45, 0.05, 0.13, 0.02, 0.25, 0.1)$, where f_i is the frequency of using the following instructions in fulfilling a given algorithm: f_1 is addition-subtraction, f_2 is shift, f_3 is multiplication, f_4 is division, f_5 is control transfer and f_6 is logic operations, 3) $Z_{max} = 67$, 4) parameters τ_j and q_j are according to the table and 5) $W_{max} = 200$ ops/s at vector F, corresponding to item 2, $(T_{sr})_{max} = 1/W_{max} = 5 \cdot 10^{-6}$ second.

Estimates of Figures of Internal Configuration with Respect to Equipment q_j and With Respect to Time τ_j

(1) № пп.	(2) Функциональный узел	Затраты оборудования q_j (корпус 155 (3) серии)	Затраты ПЗУ в мк (микрокоманды) (4)	(5) Затраты времени τ_j в нс	(6) Примечание
1	СК (7)	4	2	400	—
2	ИР+$\Sigma_{инд}$ (8)	6	3	600	—
3	Сх.зн.А (9)	3	10	2000	— (13)
4	БФПР (10)	4	11	2200	При операции сложения—вычитания
5	СчЦ (11)	1	2	6400	При выполнении операции умножения (14)
6	РгВ (12) →	4	2	6400	При выполнении операции умножения (14)

The times are given for machine cycle of 200 nanoseconds.

Key:
1. Number of item
2. Functional assembly
3. Equipment expenditures q_j (housing of series 155)
4. PZU expenditures in mk (microinstruction)
5. Time expenditures τ_j in nanoseconds
6. Remarks
7. Instruction counter
8. Index register plus index adder
9. Circuit of value A
10. Unit for forming result features
11. Cycle counter
12. External shift register
13. During addition-subtraction operation
14. During multiplication operation

Estimates of the features of the internal configuration of a microcomputer with SM EVM [International Small Computer System] instruction system are presented in the table with respect to q_j in IMS [integrated microcircuit] housings of series 155 and with respect to time τ_j in number of microinstructions.

Solving the linear programming problem described above, replacing the hardware realization by certain features and entrusting fulfillment of their

functions to the corresponding microprograms, one can find the versions of internal configuration that satisfy the specifications for productivity and equipment.

The internal configuration presented in the example is the highest-speed version of a microcomputer that at the same time requires the highest equipment expenditures. The given version of a microcomputer is the result of solving problem 3 for achieving the maximum productivity with given restrictions on equipment with the input data presented above.

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HIGHLY PRODUCTIVE COMPUTER EQUIPMENT FOR DATA PROCESSING

Novosibirsk VYSOKOPROIZVODITEL'NYYE VYCHISLITEL'NYYE SREDSTVA DLYA OBRABOTKI DANNYKH in Russian 1981 (signed to press 15 Jul 81) pp 2-4

[Annotation, table of contents and foreword from the collection "Highly Productive Computer Equipment for Data Processing" edited by Vadim Yevgen'yevich Kotov, Vychislitel'nyy tsentr SO AN SSSR, 299 copies, 90 pages]

[Text] Annotation

The topical collection "Highly Productive Computer Equipment for Data Processing" includes articles devoted to works carried out at the Computer Center by the MARS [Modular Asynchronous Developed System] and TsOGI [Center for Geophysical Information Processing] projects.

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Foreword

The success of microelectronics permits a considerable expansion of the nomenclature of computer equipment and development of computers of different designation with diverse structure that corresponds more optimally to the different spheres of their application. The fields of application of computer equipment and methods of using it--highly productive universal computers for solving large problems of mathematical physics, computers for large information systems, field computer complexes, video information processing systems, computers as components of collective-use networks and systems, problem-oriented laboratory computer systems and so on--are being expanded constantly. Scientific research work is being conducted at the Computer Center, Siberian Department, USSR Academy of Sciences in the configuration of parallel computers and complexes. Articles that illuminate some preliminary results of investigations on the equipment components of the MARS (Modular Asynchronous Developed System) and TsOGI (Geophysical Information Processing Center) projects and the seismic data gathering and processing system are included in the present collection.

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CONFIGURATION AND PRINCIPLES OF ORGANIZATION OF PARALLEL PROCESSOR FOR NUMERICAL PROCESSING

Novosibirsk VYSOKOPROIZVODITEL'NYYE VYCHISLITEL'NYYE SREDSTVA DLYA OBRABOTKI DANNYKH in Russian 1981 (signed to press 15 Jul 81) pp 5-13

[Article by Yu. L. Vishnevskiy, V. Ye. Kotov and A. G. Marchuk from the collection "Highly Productive Computer Equipment for Data Processing" edited by Vadim Yevgen'yevich Kotov, Vychislitel'nyy tsentr SO AN SSSR, 299 copies, 90 pages]

[Text] An approach that includes the design of specialized computers intended to solve one or another class of problems has gained wide distribution during the last few years in design of computers of high and superhigh productivity. A wide diversity of specialized processors with very high productivity and that solve specific problems in real time, related mainly to image processing, processing of radar signals, trajectory calculations and so on, has appeared. These processors have given a good account of themselves and the diversity of specialized processors will probably increase even more in the future.

The greatest advances in the increase of productivity in the field of numerical processing are related to effective realization of a number of vector operations. However, scalar calculations are carried out in this case with a considerable loss in productivity. As a result the efficiency of a specialized processor depends considerably on the percentage of scalar calculations in the problems being solved. The situation also changes slightly when a scalar processor of traditional configuration is added to the computer system.

A new configuration of a numerical data processor, based on the concept of modular asynchronous developed systems (MARS) [1] and that permits new solution of the problems of efficiency both for scalar and vector calculations, is proposed in the given article. The main features of the processor are:

hierarchical structure (system, subsystems, functional devices and basic components levels) and functional specialization at all levels by sharing control, memory, processing and switching functions;

parallellism at all levels, asynchronous interaction of subsystems, combination of fragments, parallel execution and a conveyor;

synchronous microprogram realization of subsystems;

a basic method of combining functional devices--the switching method;

development of a local memory structure and multi-access common memory;

hierarchical microprogramming;

configurational independence of machine language;

high level of system language;

parallel operating system.

Structure of Processor

The processor consists of four main subsystems--control subsystem, address and computing subsystems and also memory subsystem.

The processing subsystems of the processor are constructed on the unified principle. They consist of conveyor type individual functional devices (FU) specialized to perform specific operations. The functional devices interact by means of a controlled high-speed switchboard. The subsystem control device guarantees parallel operation of the functional devices and parallel execution of several (possibly different) fragments in the subsystem that realize specific macrofunctions. The programs of these fragments are stored in the subsystem instruction memory. Functional delay devices were used in the subsystems for temporary storage of intermediate results.

In the information sense, the subsystems are divided into several layers of data to be processed, belonging to independent fragments in the general case. The functional devices share these layers in time, which permits combination execution of scalar fragments to increase the degree of useful loading of the subsystems.

The unified structural principle, which includes the fact that the separate module at each level of the hierarchy consists of functionally oriented submodules that perform processing, storage, control and switching functions, is followed in design of individual subsystems, the processor as a whole and the system that combines several processors.

The figure presents an overall representation of the processor structure.

The functioning of the entire processor is based on the flow or conveyor principle. The control subsystem (UPS) forms the line of operators ready for execution. The operator is a list of names of fragments, consisting of the names of address fragments and the names of the computing fragments and their relationships according to the initial calculating formula. The names of the fragments are accordingly entered in the address subsystem (APS) or computing subsystem (VPS). In the general case an individual address fragment realizes a nontrivial function of sampling data elements of complex structure and generates address flows by which operands should be read from the data memory or by which the results of calculations should be written in the memory. The

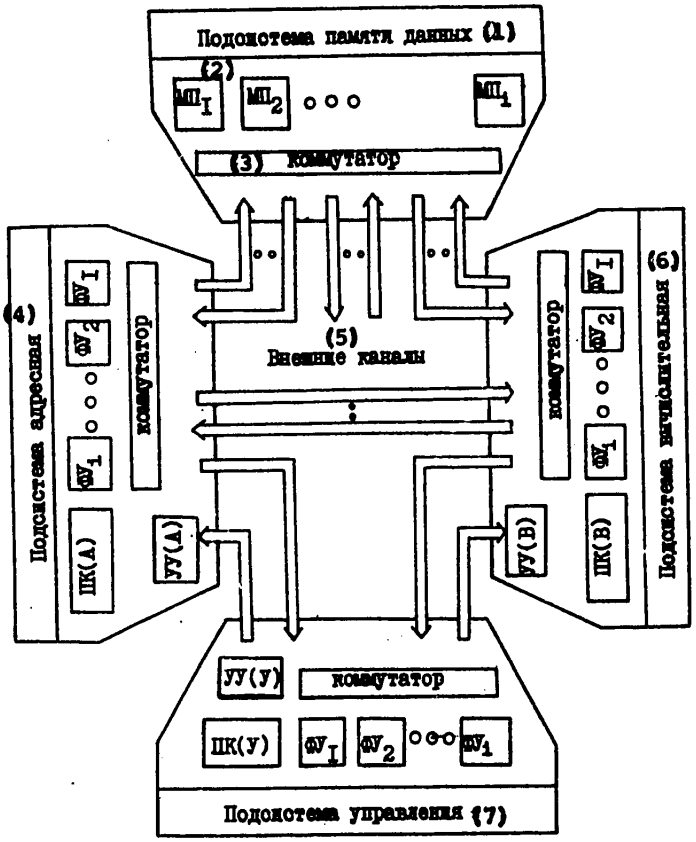

Figure 1. Overall Structure of Processor

Key:
1. Data memory subsystem
2. Memory module
3. Switchboard
4. Address subsystem
5. External channels
6. Computing subsystem
7. Control subsystem

computing fragment realizes some computing function on vector independent variables. It processes input data flows and forms output flows of results, part of which is sent back to this same subsystem as input flows for other fragments and part of which is written in the memory. The control subsystem permits several interpretation processes to be carried out in the layers of the subsystem, forming fragments in the computing and address subsystems and monitoring their execution.

Organization of Subsystems

An important configurational concept is that of the subsystem. A subsystem is a functionally self-contained module of a system connected to other

subsystems by asynchronous exchange channels (AK). One-way transmission of information from one subsystem to another is accomplished through the asynchronous channel; therefore, writing and reading channels are distinguished. The same channel for a single subsystem is a reading channel and the same channel for another subsystem is a writing channel.

A subsystem, as noted above, generally realizes nontrivial processing functions. These functions are programmed in the subsystem and represent functionally complete program modules, so-called fragments. We shall sometimes understand a fragment as a program itself and sometimes as the process of executing this program in the subsystem. A fragment usually realizes some typical microfunction, partially used in user programs. No special restrictions on the algorithmic complexity of fragments are introduced. They can realize both simple processing diagrams and those containing cycles and conditional control. The complexity of the fragments will be limited on the one hand by the limitation of the resources in the subsystem and on the other hand by the requirement of sufficiently frequent use of this fragment in user problems (it is probably unfeasible to create a too complex fragment for infrequent use; it is better to realize it by means of simpler typical fragments).

Several fragments can be initiated in a subsystem. The capability of combining the work of several fragments in a subsystem is provided by the following concepts.

First, the capability of assigning several address and computing fragments in the instruction is an important aspect. Several structures can participate simultaneously in processing. The elements of these structures can be read and written by different, but simultaneously executed address fragments. The instruction for several related computing fragments permits a more complex processing function to be assigned, which is a composite of typical functions.

Second, we regard the combination of fragments as a method used to increase the productivity of the conveyor subsystem when processing scalar fragments. During operation an individual fragment that processes scalar independent variables, the subsystem is not completely loaded. A combination of fragments is essentially a method used to determine the advantages of continuous flow organization of the subsystem.

Since several fragments can be in the active state simultaneously in the subsystem, it is convenient to represent a subsystem consisting of several layers or sections by the number of combined fragments. Each fragment can function within only one section allocated to it and in this sense it is protected against the action of other fragments and itself does not affect them directly.

Differently processor subsystems have a unified structure regardless of functional orientation. This solution has a number of positive properties. Thus, the methodology and technique of fragment microprogramming, subsystem control, organization of the memory of fragments, the structure of communications between devices, verification and debugging are all solved in the unified manner in different subsystems.

A subsystem regarded as an individual functional module consists of submodules that perform the functions of processing, control, switching and memory. Processing functions are accomplished by means of functional devices (FU). The subsystem contains several functional devices, which can operate simultaneously, to parallel these functions. Functional systems are oriented toward performance of specific elementary operations. The composition of a functional system in the subsystem and structure of data that are processed by these functional devices determines the functional specialization of the subsystem. Functional devices that realize functions requiring several operating cycles for execution have conveyor organization.

Thus, regardless of the number of cycles required to perform operations, the input of each functional device is freed at the beginning of the next cycle to receive the following operands and instructions.

Analysis of typical computing problems such as those of linear algebra, spectral analysis, calculation of elementary and spectral functions, formula calculations, calculation of polynomials and so on showed that a high-speed matrix switchboard can be used to guarantee flexible communication of the functional devices with each other if their number is relatively small (10-20).

The synchronous principle of functional device interaction is adopted in the subsystem. First, the synchronous principle requires approximately 30 percent less equipment compared to the asynchronous principle. Second, the determinant behavior of all the functional devices simplifies the control of the functional devices and, which is important, simplifies the switchboard since in this case the status of the switchboard is replaced synchronously by a single switching instruction. Moreover, fragment programming is simplified. Third, analysis of synchronous systems is simpler than analysis of asynchronous systems.

Systems Organization

The design principles of a system are as follows:

the system is constructed from several functionally oriented subsystems--the address subsystem (APS), computing subsystem (VPS), control subsystem (UPS), memory subsystem (PPS) and peripheral subsystem (PFPS);

a set of interacting processes (fragments) functions at a given moment in each of the subsystems and in the system as a whole;

asynchronous channels are used to transfer operands from one process to another; if the interacting processes function in different subsystems, their interaction is organized through channels that link different subsystems to each other; if the interacting processes function within a single subsystem, then channels that combine input and output terminals of the subsystem are used;

input operands are accordingly entered in the subsystem through input terminals, while the result operands accordingly leave the subsystem through the output terminals; the terminals can connect the inputs or outputs of

asynchronous channels of different designation; there may be several input and output terminals in the subsystem;

different types of resources required to fulfill a process are designated dynamically and independently of each other; the types of resources subject to distribution are the sections of the subsystem, the subchannels of asynchronous channels, the zones of local parameters of the process and the data and program memory domains. The last type of resources is determined for the program as a whole rather than for an individual process. The dynamic distribution of resources creates prerequisites, first, for organization of asynchronous starting of processes as resources are freed, which leads to an increase of the degree of loading of subsystems and accordingly to an increase of productivity, and second, to create a configurationally independent processor input language. This must be understood in the sense that the input language should not be strongly dependent on a specific set of processor resources, which solves the problem of the transferability of programs within different processor configurations.

The hierarchical principle of control is realized in the system, which reflects the hierarchical structure of the programs. The following levels of control are distinguished (from top to bottom):

control of execution of an individual fragment in a subsystem;

control of execution of an operator consisting of a list of interacting fragments; it includes tracking the operation of individual fragments and the distribution of resources for them;

control of execution of the program module consisting of a list of operators; it includes organization of the sequence of fulfilling the operators and of following the work of individual operators;

control of execution of the program consisting of modules; it includes following the work of modules, calculating the conditions of response of the modules and organization of access to shared resources jointly with the different modules being used.

The first level of control is realized in subsystems. The second and third levels are realized by the control subsystem by means of the corresponding fragments whose programs are written in the fragment memory of the control subsystem, or in other words by means of microprogram realization of control functions. It is feasible that several control processes--fragments--are constantly in an active status in the control subsystem. This is true of such fragments as interpretation of the input language operator, control of fulfillment of the operator, initial response to interrupt signals coming from subsystems and so on.

The fourth level of control is realized mainly by programs, i.e., by the operators and program modules of the user program or of the operating system. Some functions such as synchronization of processes during use of common resources and others such as second- and third-level control functions, may have equipment support in the form of special functional devices within the control subsystem.

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STRUCTURE OF IMAGE PROCESSING SYSTEM

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[Text] Consideration of a rather wide range of image processing problems, realization of which does not assume different geomtric transformations of the rotation or tension type and in the general case is unrelated to deformation of the coordinate grid, permits one to determine at a specific level of detail the stable structure of algorithms that guarantee solution of these problems.

This is determination of some, relatively small subset of elements of the initial image or an aggregate of them.

This is the representation on this set of the computing proceduring that generates a number of values related in the general case to different features.

This is organization of the process that accomplishes continuous or block mapping of the data of the initial set onto the domain of definition of the computing procedure during the process or sequential application of it to the entire initial volume of data or during tracking of some functional by it.

The entire series of problems in the considered scheme will require a known number of "passes," related to calculation of the preliminary parameters of transformations, for example, of parameters that reflect the characteristics of classes, in problems related to classification [1, 2]. Moreover, sequential use of computing procedures permits one to realize iteration algorithms. The effectiveness of the latter will be determined by the flexibility of representation of parameters, by the variety of computing procedures corresponding to the iterations and by the capability of representing different structures and "forms" of subsets for them. Thus, this may be some local domain around each point in the plane of the photograph for a number of transformations as, for example, in realization of convolution or a series of mathematical operations related to calculation of gradients, Laplacians and to interpolation or to calculation of features that reflect the texture of images [4, 5, 6]. For

realization of orthogonal transformations, this may be a set formed of elements whose coordinates reflect doubly inverse order [3]. This will be sets of vectors in problems of synthesis of color images or problems related to presentation of input information contained in several photographs, according to the characteristics of human perception of the images [7, 8]. In some problems the domain of definition of the computing procedure may correspond to some "volume," related to multidimensional representation of data [6] or on the contrary may degenerate to a point [4]. It is the necessity of the joint guarantee of the variety of "forms" and structures of the domains of definition of computing procedures that affect to a considerable degree the practical realization of interactive modes of image processing if the latter are not restricted by some narrow class of problems. If one proceeds from the fact that complex thematic processing of images, interpreter to a significant degree by its form, first requires an interactive medium, assuming joint postulation and resolution of a rather wide range of problems, then guarantee of the capability considered above becomes one of the main aspects in realization of this system. The latter is considerably aggravated by the significant volume of data to be processed, which comprises tens of Mbytes with regard to intermediate results in many problems even in relatively small image formats, as for example, in problems of classification with regard to adjacent elements in the plane of the photograph. All this assumes the presence of internal storage corresponding to the system.

Although the prospects for designing an internal storage with this capacity with random access is unrealistic, this is still on the one hand an expensive gratification (and even in this case one must have it in practice) and on the other hand, one can consider a compromise version. Then there is a corresponding hierarchy of memory levels related to each other by exchange processors. The structure of the latter, depending on specific problems and types of data determined by the control computer, should guarantee dynamic pumping of data and passage of it thourhg a medium that accomplishes direct processing.

The sufficient effectiveness of this hierarchy of memory levels follows primarily from the structure of processing algorithms that considers the sequential nature of access at the level of certain volumes of data and that assumes random access within them. It must be noted that this situation can occur upon transition from level to level up to a medium that guarantees realization of computing operations and in this case, the levels, like the algorithms themselves, may permit considerable parallelling.

The corresponding assumed levels of the memory hierarchy are:

the level of the operating library that guarantees random access at the data file level and sequential access inside them;

a main internal storage that guarantees buffering, storage and random access to data;

fast internal storage to which data are transformed which are the domain of definition of the computing procedure and from which they are accessible to it.

The interaction of exchange processes of the corresponding memory levels is unrelated to the address spaces of the latter and is vector, block exchange in nature. The problem of realization of a conveyor in direct form is not posed here. Again the variety of problems obviously does not permit complete coordination of the indirect rate of processing, the speed will be determined by the longer term operation and is more reasonable to guarantee support of them, using both microprogram and equipment realization of the latter.

The general algorithm of interaction of the main parts of the system, consisting of a main computer and terminal station (Figure 1) that includes a control computer, a set of commutation address exchange processors, several levels of data storage and display system, a direct computing medium and also abbreviations of interaction with the operator, assumes mapping of the selected combination of user procedures by the control computer onto a set of intial states of the required modules and parts of the system and initiation and maintenance of exchanges between them.

The memory subsystem, related to the level of the operating library, is guaranteed by the interaction of a number of modules joined in a single crate by the corresponding mainlines--one for control from the controller (E-60 minicomputer) and two for exchange of data. The latter guarantee sequential bit and byte addressless asynchronous exchange of data. Apparatus support of the controller at the level of the corresponding modules permits connection through interface cards of different media that guarantee direct storage of data if their structure permits one to consider them as a memory having random access to sequential files. This can obviously be media realized on the basis of Ts. M.D. [expansion unknown], on P.Z.S [expansion unknown], on structures or, for example, on magnetic disk store. The difference will be essentially related to the exchange time, which in the latter case for an image with volume of 512 X 512 X 8 bits (YeS-5061 magnetic disk) will correspond to 1-2 seconds. The effect of this value on the rate of solving problems in dialogue, with regard to the corresponding capabilities of buffering up to several images in the internal storage, of guaranteeing dynamic pumping of data and finally, with regard to the time for representation of the corresponding user directives during operation, can obviously not be so significant. Guarantee of all functions for management and description of the library catalogue and also communication with other external devices is guaranteed directly by means of this level. This permits one to consider interaction with a control process at the level of images and tasks and is not rigidly tied to realization of other levels and subsystems.

The level of the main internal storage is guaranteed by the set of unconnected units (channels) of the internal storage, physically realized in individual crates. Each of these units is a semiconductor memory with direct access, which is accomplished through a unified exchange mainline and which permits connection of different functional modules to it. In this case the capacity of each unit is determined by the number of memory modules contained in it. The maximum number of these modules is limited to eight. Their organization corresponds to a two-dimensional structure with capacity of 256 X 127 16-bit words and permits double stratification at the module level. This permits, along with the capability of access to a byte and 16-digit word, a guarantee

of simultaneous access of two words (32 digits) and of realizing the maximum capacity with a cycle of 400 nanoseconds of the memory itself up to 10 Mbytes/s. This capability guarantees the effectiveness of data exchange during operations related to representation of operands that require large dynamic ranges.

The nature of interaction of all modules and the processes corresponding to them is related to execution of drive and driven (several driven) functions and to establishment of asynchronous communications at the level of the first part of the address (the number of the vector) and synchronous data exchange in the second part (number of the element). The latter is achieved by a 12-digit multiplexed line.

Resolution of conflicts for a simultaneous request of a mainline is entrusted to a module that performs the functions of arbitrator and in this case the process having lowest priority can be interrupted after notification.

The basic set of functional modules corresponding to a single channel includes N internal storage modules (1-8), mainline arbitrator module, corresponding exchange processor modules both with operating library and fast internal storage accessible for calculations, a television driver and interface module directly for the control computer. The control registers of each of the modules is allocated an address space in the total capacity of the memory. Thus, for example, the television driver is described with the following set of registers. These are:

an element number register from which the image can be fed to the monitor (1,024 X 512 elements);

register for placing the image on the monitor screen;

register of the size of the imaged zone of the memory;

vertical and horizontal scale register (1, 2, 4, 8);

general control register.

Control of these registers is accessible to any mainline modules and permits realization of a number of interesting modes in image interpolation on the screen and in "animation" of the images by using multiplication by addition of special modules or, finally, it guarantees the capability of achieving a stereo effect with subsequenting tinting.

The carrying capacity of each of the channels and its capacity permits the television driver to display one of two images measuring 512 X 512 elements on the monitor or two of eight images simultaneously with resolution of 256 X X 256 elements of 8 bits each. Television drivers permit joint synchronization to regenerate the images in color with resolution of 512 X 512 elements or, for example, to achieve the capability of printing the image in 1,024 X 1,024 elements. One to organize parallel printing of several images immediately, depending on the number of available channels, and guarantees the capability of subsequent joint processing of them in the video tempo, i.e., to realize

similar capabilities of known systems. The basic version of the system includes up to four channels whose television outputs are combined into a systems television unit that permits switching, superposition of data, "tinting" of them during using of a color monitor and conversion of digital values to analog values.

The provision of readout by means of address processors from each of the internal storage units, determined by an ordered set of data that are the domain of definition of the computing procedure, permits effective use of vector processors for direct calculations. In this case the functions of the domain of the fast internal storage are performed directly by the internal storage of the vector processor. This version is more than sufficient for a number of problems, but one must encounter rather significant overhead expenses in exchange and duplication of data when realizing algorithms related to the initial two-dimensional structure of data. Thus, for example, when realizing convolution of an image with some mask (window) measuring 32 X 32 elements for calculation of a single new value, transmission of up to 1,000 elements to a vector processor without modification and adjustment of its program is required, whereas it would be sufficient to get along with 32 elements. Without excluding the considered capability, the terminal station is provided with its own internal storage and the corresponding computing medium.

The structure of the memory, from the viewpoint of display of an initial aggregate of data on it, emulates to a known degree the memory on shift registers, retaining random access within it in this case. A specific structure of data controlled by previous processors essentially seems to move and slip through this memory.

The memory consists directly of modules that permit parallel access of a set of computing processors (automatons) to them through one of the channels ("vertical"). A guarantee of movement through them is accomplished by the "horizontal" channels. All the modules are combined by a unified address line connected to a control device. Parallel removal of similar operands from each module is realized in practice.

The set of computing processors (or one processor) is also under single control. Communication with modules of the internal storage is accomplished through a switching medium. The latter ensures the capability of a relative shift of the processor matrix with respect to the memory modules, thus expanding the domain of definition of the computing procedure and retaining parallel operation of all processors.

The control device and the corresponding exchange channels with upper level of internal storage are similar to the media considered earlier and are accessible to the control computer through the level interface.

The considered structure of the image processing system, which assumes a developed dialogue during operation, guarantees known flexibility and permits the development and increase of capacity both in speed and in the complexity of the algorithms. The independence of levels and their modular nature within guarantees effective practical realization and the capability of design and assembly of different configurations.

Whereas a considerable part of the cost of a system is now related to its software, then part of it cannot be applied to the hardware level.

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DATA TRANSMISSION SYSTEM BASED ON ELEKTRONIKA-60 MICROCOMPUTER AND CAMAC EQUIPMENT

Novosibirsk VYSOKOPROIZVODITEL'NYYE VYCHISLITEL'NYYE SREDSTVA DLYA OBRABOTKI DANNYKH in Russian 1981 (signed to press 15 Jul 81) pp 75-81

[Article by S. T. Vas'kov, Ye. N. Bobrov and B. V. Fesenko from the collection "Highly Productive Computer Equipment for Data Processing" edited by Vadim Yevgen'yevich Kotov, Vychislitel'nyy tsentr SO AN SSSR, 299 copies, 90 pages]

[Text] A set of CAMAC modules that match the crate mainline to different communications channels and lines over a wide range of data transmission speeds was developed according to the operating program to create hardware of the first unit of the VTsKP [multiple-use computer center], Siberian Department, USSR Academy of Sciences, which made it possible to link territorially dispersed information gathering and processing systems to each other [1, 2].

An example of this system may be the scientific research automation system based on the Elektronika-60 microcomputer.

A set of different input-output devices linked by a computer channel provides greater functional capabilities in organization of this system.

Development of data transmission equipment (APD) in the designs of the Elektronika-60 microcomputer was a further continuation of work within the project of the multiple-use computer center, Siberian Department, USSR Academy of Sciences, and made it possible to expand the capabilities of the serial computer.

On the one hand, development of data transmission equipment within the designs of microcomputers and on the other hand, compatible in exchange formats and protocols to similar CAMAC equipment, permits organization of different versions of equipment configuration during design of the network such as:

exchange of two remote computers,

exchange of two remote CAMAC systems,

and exchange of a remote microcomputer with a CAMAC system.

Data transmission equipment guarantees matching of the common bus of the Elektronika-60 microcomputer to a sequential communications channel. The connecting lines of a city telephone exchange or physical pairs, transmission through which can be accomplished at speeds of 12, 24, 48 and 96 kbaud, can be used in realization of the communications channel.

Data transmission to a distance up to 16 kilometers is possible in this case.

There is the capability of operating on a standard tone-frequency telephone channel using serial signal conversion devices (modems).

In this case the data transmission equipment, besides being matched to the physical line, guarantees matching with the modem by a standard S2 junction [4].

Organization of data transmission over a tone-frequency telephone channel using serial modems is presented in Figure 1.

A duplex information channel is realized in these systems, i.e., transmission can be accomplished independently both in the forward and reverse directions. At the same time the proposed circuit also permits operation in the semiduplex mode.

The data transmission system is by function:

a system with resolving feedback (information is verified at the receiving end and a signal is transmitted to the return channel on the results of reception);

a system with feedback signal expectation (the next information is transmitted after the signal is received from the return channel).

The feedback signal is transmitted over the information channel of the reverse direction.

The presence of an internal storage permits information to be stored until confirmation has been received from the return channel.

The developed data transmission equipment is oriented toward the use of HDLC line protocol (high-level bit-oriented communications channel control procedure), confirmed by the International Organization on Standards (ISO standard 3309).

According to the protocol, a code-independence mode, formation of the structure of information transmitted over the communications channel and verification of the status of the channel are provided.

A block diagram of the data transmission equipment is shown in Figure 2.

The transmitting and receiving part includes an internal storage with capacity of 256 eight-digit words intended to store information for the verification time.

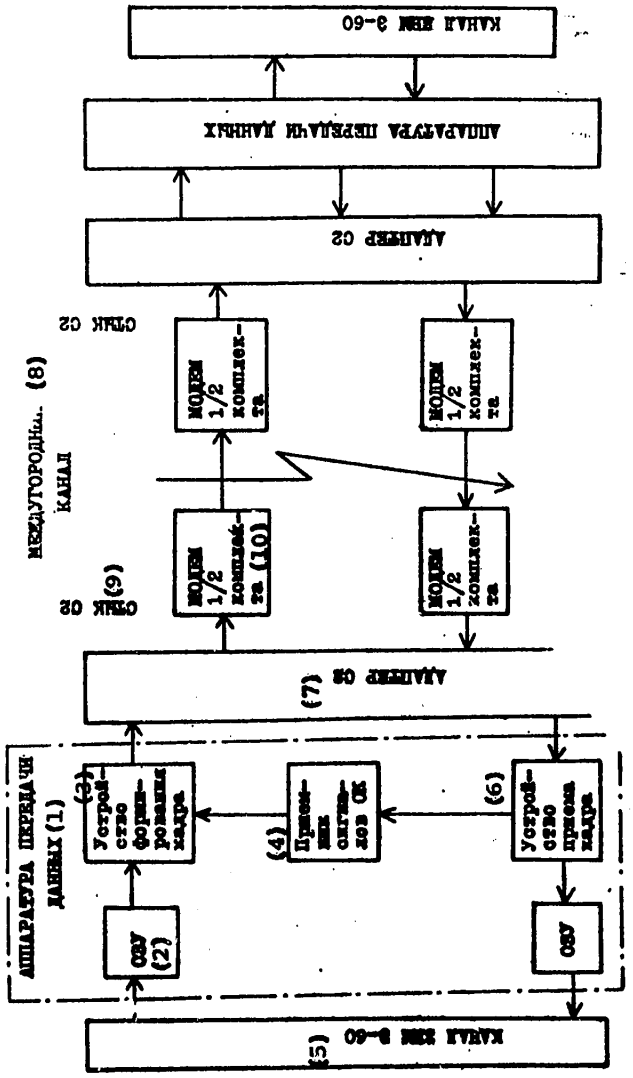


Figure 1. Block Diagram of Data Tranmission System Between Two Elektronika Microcomputers Using Standard Modems

Key:
1. Data transmission equipment
2. Internal storage
3. Frame shaping device
4. SK signal detector
5. Elektronika-60 computer channel
6. Frame receiving device
7. S2 adapter
8. Long-distance channel
9. S2 junction
10. One-half set modem

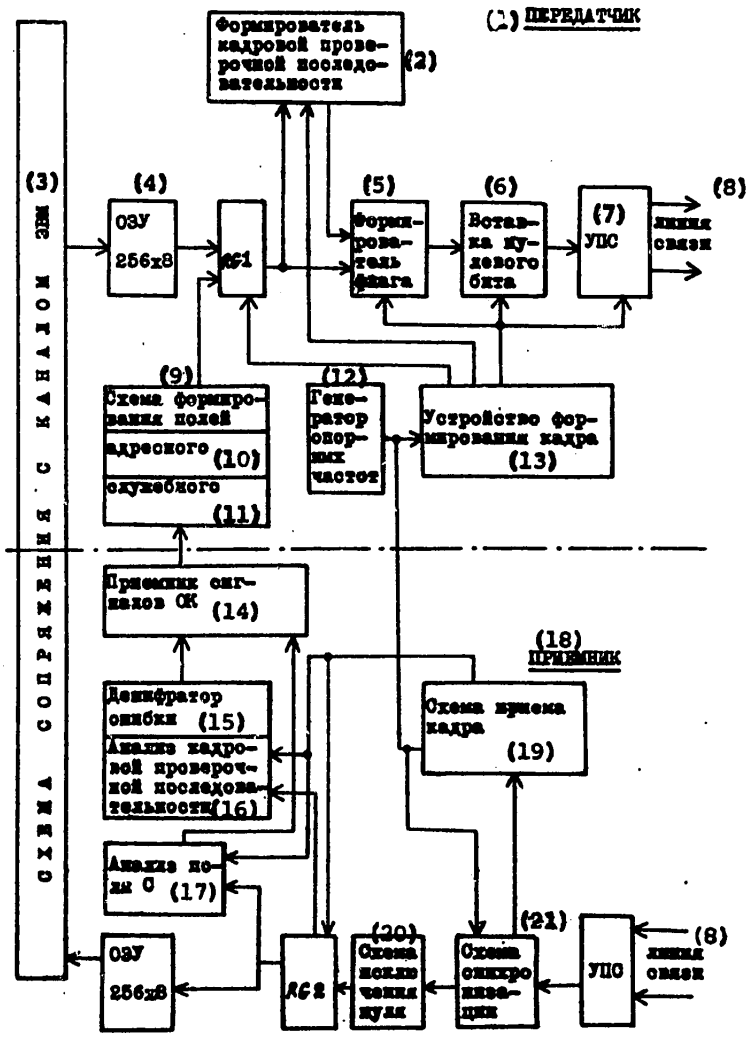


Figure 2. Block Diagram of Data Transmission Equipment

Key:

1. Transmitter
2. Frame verification sequence shaper
3. Computer channel integration circuit
4. Internal storage
5. Flag shaper
6. Zero bit insert
7. Signal conversion device
8. Communications line
9. Field shaping circuit
10. Address
11. Service
12. Reference frequency generator
13. Frame shaping device
14. OK signal detector
15. Error decoder

[Continued on following page]

[Key continued from preceding page]:

16. Frame verification sequence
17. Analysis of field S
18. Receiver
19. Frame receiving circuit
20. Zero exclusion circuit
21. Synchronization circuit

The use of two internal stores was determined by the need to organize a duplex operating mode in both directions.

RG1 and RG2 are registers that convert an eight-digit parallel/series code to series/parallel code.

The frame verification sequence shaper is a register with feedback that realizes the generator polynomial

$$x^{16} + x^{12} + x^5 + 1.$$

The designation of the remaining assemblies is clear from the block diagram.

Information is exchanged between the central processor and the data transmission equipment by means of standard access cycles to the channel.

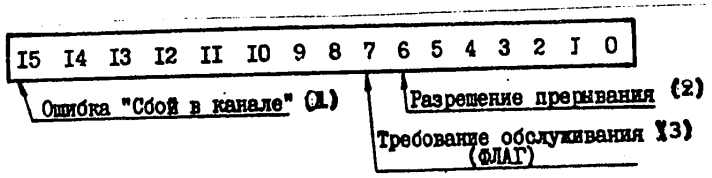
There is a number of internal registers to organize this exchange of the data transmission equipment.

The transmitter status register (address 177600) participates in operations with respect to the service requirement and presentation of interrupt.

The transmitter (address 177602) and receiver (address 177606) data registers are used during data exchange.

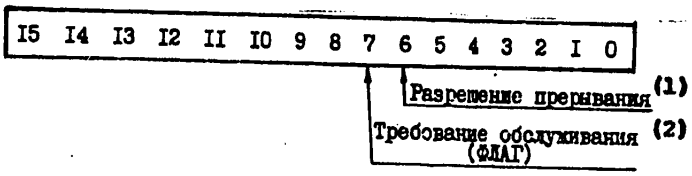
The transmitter word counting register (address 177610) is used to control the length of the transmitted data pack in the range from 0 to 256 bytes.

The receiver word counting register (address 177612) is designed to store information about the length of the data pack taken from the communications channel and stored in the internal storage. The register formats are presented below.



Format of Transmitter Status Register

Key:
1. "Breakdown in channel" error
2. Interrupt authorization
3. Servicing requirement (FLAG)



Format of Receiver Status Register

Key:
1. Interrupt authorization
2. Servicing requirement (FLAG)

Formats of Data Registers and Transmitter and Receiver Word Counting Register

Key:
1. Not used
2. Data

Using the capability of writing to the transmitting and receiving data registers (and the internal storage serves as them) for all 256 addresses and subsequent reading permits one tc organize testing of the internal storage in the auto-increment mode, while the use of the write-pause-read mode permits one to organize random access to the internal storage.

Organization of the interrupt requirement, presentation of interrupt and transmission of the interrupt vector address are accomplished in the standard manner for a computer.

Two independent interrupt requirements are used to call up the transmitter and receiver servicing subroutines. The interrupt vector addresses are 230 and 234, respectively.

Structurally, the data transmission equipment is fulfilled in two versions:

data transmission equipment for operating over the connecting lines of a city telephone exchange or over physical lines. In this case the data transmission equipment is made in the form of a single plate measuring 252 X 296 mm with disconnects for a lead to the computer channel and one disconnect on the plate for connecting the communications line.

If operation is over a standard tone-frequency telephone channel, then the same plate measuring 252 X 296 mm is used, but instead of an integration device with physical line, integration by a standard S2 junction is made on it [4] that guarantees matching to the serial modem.

The use of this equipment considerably expands the class of problems solved by means of microcomputers and making this equipment on a single ideological base from one developed previously permits solution of problems of compatibility and continuity of the equipment being developed.

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MODEM-2400 SIGNAL CONVERSION DEVICE

Novosibirsk VYSOKOPROIZVODITEL'NYYE VYCHISLITEL'NYYE SREDSTVA DLYA OBRABOTKI DANNYKH in Russian 1981 (signed to press 15 Jul 81) pp 82-89

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[Excerpt] The Modem-2400 signal conversion device is included in the hardware of the data transmission systems of the Collective-Use Computer Center, Siberian Department, USSR Academy of Sciences and is designed to convert binary signals to a signal suitable for transmission over standard tone-frequency (TCh) telephone channels with four-wire ending.

The modem guarantees synchronous operation in the duplex mode with data transmission speed of 2,400 bits/s over segregated (unswitched) channels with a length of six transceiving sections on a tone frequency (without correction of the characteristic of the group delay time (GVZ) of the channel).

The digital method of direct signal shaping in a temporary domain is used to transmit data in the modem transmitter [1].

Service information is transmitted in the return digital information channel organized in "data transmitter" and "data receiver" CAMAC modules [2, 3].

The Modem-2400 is designed for stable operation with frequency shift up to $\pm$7 Hz in the communications channel and length of the connecting line (SL) between the modem and tone-frequency channel up to 20 km and with variation of the received signal level from 0 to -30 dB. The signal level during transmission can be regulated in the range from 0 to 28 dB. The permissible communications interrupt time that does not lead to desynchronization of the modem receiver is 10 seconds. If fluctuating noise is fed to the receiver input with level 5 dB below the signal level, the bit error coefficient comprises not less than $1 \cdot 10^{-4}$. The frequency stability of the master oscillator is $1 \cdot 10^{-5}$. The output resistance of the modem in the direction of the tone-frequency channel is equal to 600 ohms.

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SOFTWARE

UDC 681.3.067

METHOD OF PROTECTION FROM UNAUTHORIZED USE OF INFORMATION IN ADAPTIVE CONTROL SYSTEM WITH IDENTIFIER

Moscow AVTOMATIKA I TELEMEKHANIKA in Russian No 4, Apr 82 (manuscript received 1 Dec 80) pp 127-132

[Article by V.N. Dyn'kin, S.S. Musayelyan and N.S. Raybman (deceased), Moscow]

[Text] The problem of protecting information from unauthorized use in an adaptive control system with an identifier having a hierarchical structure is discussed. Computer-proof transformations are presented which are used for protecting the password list of system users. A method of encryption of information and a method of authenticating messages in data transmission channels are suggested.

Modern systems for centralized supervision and control of territorially scattered enterprises, their individual subdivisions and entities have a hierarchical structure. For a hierarchical system it is possible to stipulate implementation of the ASI (adaptive control system with an identifier [1]) principle, not only for individual entities, but for the system as a whole. The block diagram of such a system for a 3-level hierarchical structure is presented in fig 1.

For many reasons, e.g., when it is necessary to maintain responsibility for functioning of an individual entity or group of entities, as well as to prevent the introduction of accidental or intentional changes in their operation, interference in the functioning process by outside individuals or individuals responsible for other entities can be undesirable. On the other hand the need arises of protecting the information circulating in the system from unauthorized actions--hooking up to communications channels for the purpose of intercepting transmitted information, including control instructions, or inserting spurious messages; and unauthorized reading or modification of data files. Various information on raw materials, materials, personnel resources and products produced can be subject to protection at various hierarchical levels. It is often necessary to protect individual subsystems. For example, of special interest is an ASI for controlling multirange supplies, when a storehouse for raw materials, semifinished products and finished products provides for the requests of several enterprises or entities, and ASI's for especially precise production processes, when the interference of outside personnel is impermissible. The most complete protection of modern automated systems requires

the involvement of hardware and software together with cryptographic methods and organizational measures for protection.

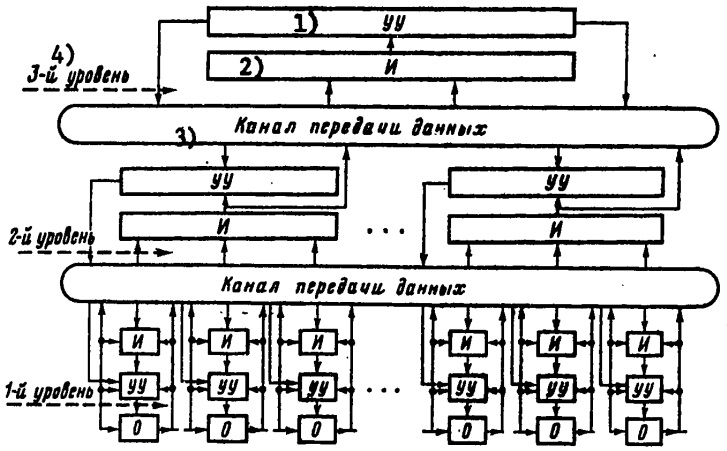

Figure 1. Block Diagram of Hierarchical ASI: UU--control unit, I--identifier, O--controlled entity

Key:
1. UU
2. I
3. Data transmission channel
4. Third level

One effective means of protecting information from unauthorized use is cryptography. It has found its obvious application in protection of communications, when information is transmitted through communications channels in encrypted form. Here the encryption can be performed both by the computer itself and by special cryptographic equipment installed at the transmitting and receiving ends of the communications line. Another important application of cryptography is the protection of external memories by means of encrypting stored information. As will be demonstrated below, cryptography can be used also for solving the problem of authenticating a user of the system--for determining the authenticity of a person requesting access to the system.

Content Formulation of Problems

Qualitative changes have been observed in the field of cryptography in recent years, which is associated with the rapid development of computer technology and an increase in the speed of computers. In particular, such concepts as computer-proofness and the one-way function [2] have appeared.

A code--the transformation of an unconcealed text into an encrypted text--is called computer-proof if in order to solve it (cracking the code's key or cracking the encrypted text without knowing the code's key is had in mind) the best of known algorithms requires the performance of a number of operations which not a single modern computer is in a position to perform in a certain time period.

We will say that function f is one-way if it easily (in a relatively small number of operations on a computer) converts unconcealed text x into encrypted text $y = f(x)$ for all values of x from the domain of definition, and the reverse operation (computation of the value of $x = f^{-1}(y)$ with a known encrypted text, y) is computationally unrealizable. The term "computationally unrealizable" means that transformation by means of the one-way function is computer-proof.

Two problems in protecting the hierarchical system referred to, which can be solved by means of cryptography, are discussed in this article:

1. Protection of the list of system user passwords stored in the computer's memory.

2. Protection from unauthorized reading of information and insertion of spurious messages in data transmission channels.

Our goal is solving the problems formulated above is to substantiate the computer-proof nature of the transformations presented and to construct appropriate encryption and decoding algorithms which can be implemented practically.

Solution of Problems

The traditional method of protecting a computing system from unauthorized access to it is the so-called password method. For the purpose of gaining access to the system each of its legitimate users presents his secret password, which is compared with a copy stored in the computer's memory in the password list under the name of the user in question. Access is permitted if the password presented agrees with the copy stored. Clearly, the list of stored passwords of system users requires reliable protection from encroachments of unauthorized people. For this it is possible to use a one-way function and to enter in the list not the passwords themselves, x, but their one-way transformation, $f(x)$ [3]. Each time a user, i, presents his secret password, x_i, the computer computes function $f(x_i)$ and compares it with the value of y_i stored in the list. Since f is a one-way function, then finding password x_i from its transformation, y_i, is impossible. Consequently, the need to protect (from unauthorized reading) the list in the computer's memory disappears.

The transformation of a binary vector--password x --into a binary vector--transformation y --by means of a certain binary matrix, H, can be used as the one-way function.

Statement 1. Transformation $x \cdot H = y$ is computer-proof.

In [4] the problem is discussed of the existence of a binary vector x with a Hamming weight of $\leq w$, so that $x \cdot H = y$, where y is the assigned binary vector, H is the assigned binary matrix and w is some negative number. It is demonstrated in [4] that this problem, as in problems of decoding in the general case of a linear code, as well as of finding the weight of the vector of a linear code, is NP-complete. NP-complete problems are NP-difficult ones for which easy solution algorithms have not been found. NP-complete problems belong to the class of NP problems which are solved by an indeterminate algorithm over a time period having a polynomial dependence on input parameters. The NP-completeness of these problems is proved by reducing to them the familiar NP-complete problem of "three-dimensional

sampling." Thus, finding password vector x of the assigned weight with known transformation vector y and matrix H is an NP-complete problem and, consequently, has a solution of exponential complexity. It remains to be added that vector x must be sufficiently long to avoid the possibility of direct search and H must be an orthogonal matrix with random distribution of zeroes and ones.

In [3] for the purpose of protecting a password list it is suggested that the following one-way function be used:

$$f(x)=q(x)=x^n+a_1x^{n-1}+\ldots+a_{n-1}x+a_n(\mathrm{mod}p), \qquad (1)$$

which self-maps set $(1,2,\ldots,p)$, where p is a large simple number, $1 \leq x$, $f(x) \leq p$ and $n, a_1, \ldots, a_n$ are whole non-negative numbers not greater than p.

Statement 2. Transformation $f(x) \equiv q(x) (\mathrm{mod}\ p)$ is computer-proof.

Actually, the computation of $f(x)$ requires $k \log n \log p$ operations, where k is a certain coefficient. This computation, even with high n and p (n on the order of 2^{50} and p about 2^{100}), is performed on a computer in fractions of a second, whereas the computation of x (finding the root of the polynomial over a Galois field, GF(p)) is a much more difficult problem. The best of the algorithms known [5] require at least $n^2(\log p)^2$ operations, which with the proper selection of n and p is an astronomically high number and is practically unrealizable. Therefore, if some outside person got possession of list y_i and tried to gain unauthorized access to the system, then he would encounter the insoluble problem of finding x from $f(x)$. It was also demonstrated in [3] that if n possible x correspond to each y_i (since the polynomial has a degree of n and p is prime) then the method of trial and error is also ineffective by far. (The required number of attempts for finding just a single password is $p/n \cdot m$, where m is the number of passwords.) Thus, function (1) is a good (in the sense of being computer-proof) one-way function.

It is tempting to use this one-way function for solving problem 2 (i.e., for encrypting information to be transmitted through communications channels). If, for example, digital values of messages, M, are substituted for x in function $f(x) \equiv \equiv q(x) (\mathrm{mod}\ p)$, and their mappings, $f(M)$, are transmitted through the channels, then in view of the one-way nature of function f the code will be sufficiently computer-proof. But the question remains unclear as to how a legitimate receiver will extract the transmitted messages from the encrypted messages received in order thereby not to perform extensive computations for finding the roots of polynomial $q(x)$ over GF(p). It is necessary also to take into account the fact that n potential messages can belong to each coded message in transmission (the degree of the polynomial equals n); therefore, ambiguity arises at the receiving end in cracking the coded messages received.

The encryption method suggested here has the following plan (fig 2).

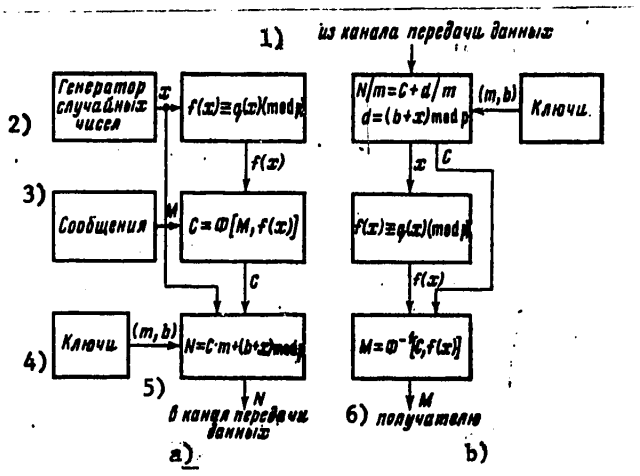

Figure 2. Flowchart of Encryption and Decoding Algorithms

Key:

1. From data transmission channel
2. Random number generator
3. Messages
4. Keys
5. To data transmission channel
6. To receiver

Encryption Algorithm

Let every kind of message, M , be replaced by its numerical equivalent over the range from 1 to p , where p is a high prime number, let us say, $p = 2^{64} - 59$. One-way function f(x) , determined by expression (1), is first computed for randomly selected x over the range from 1 to p . Then message M is converted into preliminary encrypted message C in the following manner:

$$C=\Phi[M,f(x)],$$

where $\Phi(\cdot\cdot)$ is an invertible function determining with each fixed value of f(x) the one-to-one correspondence between $M \in (1, \ldots, p)$ and $C \in (1, \ldots, p)$. Then preliminary encrypted message C is converted into encrypted message N by means of numbers m and b and the previously selected number x :

$$N=C\cdot m+(b+x)\bmod p,$$

where $m > p$ and $1 \leq b \leq p$. Numbers m and b are selected in advance by the sender and receiver as the key and are held in secrecy, and encrypted message N is transmitted into the channel, as illustrated in fig 2a.

Decoding Algorithm

Having received encrypted message N , the receiver divides it by number m and obtains preliminary encrypted message C as the quotient, and in the remainder a certain number, d = (b + x) mod p , from which, knowing b , randomly selected number x is easily found and one-way function f(x) is computed. Then the message is finally computed by means of inverse function Φ^{-1} ,

$$M=\Phi^{-1}[C, f(x)],$$

as illustrated in fig 2b.

The encryption and decoding algorithms include computation of polynomial q(x) over GF(p) and some additional operations, which makes it possible to implement them simply and to compute them rapidly on a computer.

Discussion

The Federal Data Encryption Standard (DES) developed in the USA for protecting commercial information transforms 64 bits of a binary block of unconcealed text into 64 bits of an encrypted text block. This transformation is performed under the control of 56 bits of a key block and by means of rearrangements and nonlinear substitutions scrambles the bits of data so that the slightest change in the unconcealed text completely changes the corresponding encrypted text. An analysis of the computer-proofness of the code (cryptanalysis) has shown that no simple method of disclosing the key exists for the DES, but has established the property of symmetry of the encrypted text and key in relation to their complements [2], which makes it possible to reduce by 50 percent the effort spent on cryptanalysis. The insufficient length of the key is the major area of criticism. It has been confirmed that with sufficient parallelization of the search process (on the order of 10^6) and when employing cryptanalysis with knowledge of the unconcealed text, when the corresponding unconcealed text is available in addition to the encrypted text, it is possible to make an exhaustive search of all 2^{56} possible keys.

For the method suggested, cryptanalysis reduces to finding the secret key--numbers m and b . Direct search for the key is impossible, since the exhaustive search of more than 2^{100} variants is unrealizable and the fact than number x is selected at random (for this purpose it is recommended that the GYeNAP physical random number generator [6] be used, which produces a sequence of random numbers with a specified distribution and which has a computer interface) makes it possible for identical messages to have different (random) encrypted messages and at the same time eliminates cryptanalysis by utilizing the statistical characteristics of the language employed. Furthermore, the cryptographic system described is protected from cryptanalysis with knowledge of the unconcealed text when the interceptor possesses the encrypted messages, N , and the messages, M , corresponding to them. Knowledge of these pairs of N and M does not provide the interceptor with any information on the key. Even the availability of the preliminary encrypted message, C , does not facilitate his situation.

The disadvantage of the encryption system described is extension of the amount of information to be transmitted at least twofold.

Authentication of Messages

This system also makes it possible to authenticate messages--to determine at the receiving end the authenticity and timeliness of messages received. For this purpose, in forming the next encrypted message, N_i, the sender must take into account the preliminary encrypted message, $C_i - 1$, of the preceding message, as illustrated below:

$$\begin{aligned} N_1 &= C_1 \cdot m + (b + x_1) \bmod p, \\ N_2 &= C_2 \cdot m + (b + C_1 + x_2) \bmod p, \\ &\cdots\cdots\cdots\cdots \\ N_i &= C_i \cdot m + (b + C_1 + \ldots + C_{i-1} + x_i) \bmod p, \\ &\cdots\cdots\cdots\cdots \end{aligned} \tag{2}$$

It is obvious from (2) that each successive encrypted message is related to the preceding. This structure for the formation of encrypted messages makes it possible for the receiver to detect deliberate insertion into the communications channel of spurious and old (previously intercepted) messages.

Additional Encryption

It is possible to improve reliability of concealment of transmitted messages by additional transformation of the encrypted message, N . For this it is necessary to select two numbers, m' and b' , satisfying the condition

$$m' > m \cdot p, \quad 1 \leqslant b' \leqslant p. \tag{3}$$

Then the final encrypted message, N' , will be

$$N' = C' \cdot m' + b' + N, \tag{4}$$

where $C' = \Phi[M, f(C)]$, or if to condition (3) is added the condition that m' and b' be relatively prime, $(m', b') = 1$, then instead Of (4) it is possible to use the transformation

$$N' = b' \cdot N \bmod m' .$$

Here two pairs of numbers, (m, b) and (m', b') , serve as the secret key and encrypted message N' is transmitted through the channel. The receiver by means of numbers m' and b' easily finds N and then message M from the algorithm described above. Transformations like (4) can be performed repeatedly by selecting new pairs of numbers as the key. Computer-proofness is thereby increased. The encryption and decoding algorithms are complicated unsubatantially. But the main disadvantage is retained. This is the greater increase in the amount of

information transmitted. In particular, in the case of repeated transformations, when encrypted message N' is transmitted through the channel, the amount of information transmitted increases at least threefold.

The encryption and decoding algorithms can be implemented both through software on the computer and through hardware. The latter turns out to be more desirable in the majority of instances, since it frees the data processing processor from the additional load of encrypting and decoding information and makes it possible to increase speed considerably by means of special-purpose large-scale integrated circuits.

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CSO: 1863/155

COMPUTER NETWORKS

UDC 621.395 : 621.391.15

COMPUTER NETWORK ADAPTIVITY, STABILITY, RELIABILITY

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[Annotation, table of contents, preface, conclusions and bibliographies from book "Computer Network Adaptivity, Stability and Reliability", by Stanislav Ivanovich Samoylenko, Aleksandr Abramovich Davydov, Valeriy Vladimirovich Zolotarev and Yevgeniya Iosifovna Tret'yakova; editor-in-chief: Professor Yu. G. Dadayev, doctor of engineering sciences; USSR Academy of Sciences, Scientific Council on the Complex Problem "Cybernetics", Izdatel'stvo "Nauka", 3100 copies, 278 pages]

[Excerpts] Structure of complex information processing systems is discussed in this book. Support is given to the method of adaptive switching, in which both circuit and packet switching can be used in a network as a function of the information. Considered are the sources of errors in information processing systems and methods of enhancing system noise immunity and reliability. Software methods are cited for enhancing noise immunity by using correcting codes in systems for information input, storage and transmission. Methods of synthesizing network structures are discussed.

The book is for scientists, engineers and technicians engaged in designing data transmission systems immune to noise.

Figs. 46, tables 18 and a bibliography of 214 titles.

CONTENTS

Preface

A basic problem in developing computer networks is achieving high noise immunity, reliability and viability of the system as a whole, i.e. achieving the capability of system operation when individual elements in it fail and when there are malfunctions in the systems for information transmission, storage and processing.

Analysis of error sources in complex man-machine systems indicates that of basic importance in the process is the protection of information input systems, information transmission channels and storage units. Information processing systems, based on computers, usually have higher noise immunity and reliability and make a lesser number of errors.

In connection with this, the main focus in this work is on the problems of guarding against errors in the facilities for information acquisition, storage and transmission, and on the problems of designing viable structures capable of operating when individual elements fail.

The question naturally arises: Are packet switching networks the most efficient facilities for designing integrated digital information transmission systems? Obviously, the answer has to be: No. Although packet switching networks have many advantages, they also have certain limitations and shortcomings. We should mention first of all that the presence of queues in the network centers, the length of which depends on the current load on the network, prohibits real-time transmission in this class of networks. The delay of individual messages or parts of them when sent through the network is not stable and varies with the network load. Also, the efficiency of path capacity utilization in packet switching networks depends on the type of messages sent. An analysis was made in a number of works on capacity utilization efficiency that showed that packet switching has the highest efficiency when short messages typical of interactive communication are sent. But when messages are long, circuit switching networks have higher efficiency because there is no need to divide the messages into short blocks and put in them the additional redundancy associated with addressing and other service information. Another shortcoming of packet switching is the need for processing at each network center of all information passing through it to pick out the address part of each packet and select subsequent routing, which increases the requirement for computer resources at network centers.

The network design problems is also not solved by the methods of message or circuit switching adopted separately. Message switching does not meet the requirements on delays even for interactive communication, to say nothing of real-time transmission. And with circuit switching, network path capacity utilization efficiency is considerably limited when short messages are sent, and when a low failure probability in the connection is required, loading a considerable share of the circuits in a trunk is not possible.

From what has been said, the general conclusion is that no one switching method is sufficiently universal to be used as the base for designing an efficient digital communication network to handle all types of information. Where is the way out of this situation?

The sole possibility is offered by developing networks with hybrid switching methods in which the capabilities of several methods, say circuit and packet switching, are combined. In recent years, much attention has been paid to this problem. Several levels of integration of networks with various switching methods can be isolated.

On the lower integration level are the separate networks offering data communication services in the mode of packet, circuit or message switching. The next level provides for combining switching centers while keeping separate transmission paths for the different switching modes. A higher level of integration is provided by hybrid switching in which common centers and common transmission paths are used in the network for two switching methods, say for packet and circuit switching. In the process, channel capacity can be shared between both modes. The boundary between them can be either fixed or floating; then its position is adaptively varied as a

function of the traffic. The latter method, adaptive switching, is the most promising in the sense of achieving efficiency in transmitting different types of messages when the relation between their amounts varies.

In the first chapter of this monograph, we present the principles of designing computer networks that make use of the adaptive switching method, we discuss possible network structures and we develop procedures for accessing an adaptive switching network based on extending the standard protocols used in packet switching networks.

In the second chapter, we cover the problems of enhancing noise immunity in computer networks. Here, we analyze error statistics and discuss methods of modeling them; we define the main error sources that most affect network noise immunity and methods for guarding against errors. In the sampling of protection methods included in the book, the main focus is on methods of noise-immune coding that are easy to implement by software. This is because under modern conditions with wide use of programmable units, including microprocessors, in networks, the most rational approach to enhancing noise immunity is to use software methods of protection.

In the third chapter, we discuss the problems of reliability of computer networks that include unreliable elements. Here the main focus is on principles of designing viable structures in which thanks to backup alternative routes for information transmission, there is the capability of operating the system when individual elements in it fail. As noted before, the most vulnerable spots in computer networks that affect their reliability are the communication channels; because of this, the main focus is on problems of designing reliable data communication networks that combine the network computer resources.

Chapter 3 was written jointly by A. A. Korobov and Yu. B. Shufchuk by using material made vailable by S. I. Samoylenko (section 3.13).

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Chapter 1. Adaptive Switching in Computer Networks

All that has been presented indicates that communication channel capacity utilization efficiency, and consequently communication costs, with the different switching types depends substantially on the nature of meesages sent.

However, the precise value of the parameters of the messages, on which the switching method efficiency depends, is unknown not only when the network is being designed, but even when it is being operated; as a result, a clear choice of an optimal switching method for a network being designed is essentially an unsolvable problem.

The sole possibility of achieving high network efficiency is to use adaptive switching principles, in which different switching methods can be used in the network, and the distribution of capacity between them occurs adaptively as a function of the state of the network at a given time.

1.6. Conclusion

The adaptive switching method affords the capability of raising the efficiency of using channel capacity in those cases when there is no precise information on the expected characteristics of messages to be sent, particularly on the distribution of message lengths and priorities, when the network is designed.

Adaptive switching will also allow raising the efficiency of communication channel utilization when the traffic varies in time.

Raising channel utilization efficiency with adaptive switching is achieved by using two reconfiguration mechanisms:

1) changing the allocation of network path capacity for sending in the packet and circuit switching modes as a function of requirements that arise, and

2) filling the pauses in the component messages.

Adaptive switching expands the range of services offered the network users, since, based on it, one can send with different priority levels in two modes, packet and circuit switching. Also, in the case of adaptive switching, there is the fundamentally new capability of organizing permanent switched channels with a high efficiency of path utilization, since the lack of communication on the permanent channel will automatically be filled by packets.

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Chapter 2. Noise Immunity in Computer Networks

2.9. Conclusion

The evolution of complex data processing systems is producing the need for a thorough study of the methods for raising data transmission efficiency and quality at all stages of the passage of digital data through the system. A most important criterion for selecting a particular method is the simplicity of the algorithms used to achieve high validity in information exchange and processing.

Another important problem occurring in computer network design is the development of methods that speed up and facilitate modeling of the operation of systems or parts of them under real conditions.

In connection with the obvious nonstationarity of many of the channels used and in view of the need for a set of rather large statistics, the models and error generators used must be especially simple and at the same time reflect the most essential properties of the channels they correspond to. Examples of the solution to the problem of designing efficient models meeting these requirements were presented above.

In selecting noise-immune coding methods, one should be guided by the fact that the least currently possible complexity of implementation with at the same time maximum speed and high uniformity of the apparatus is achieved when multithreshold decoders of convolutional codes are used in memoryless DSK [symmetric binary channels]. When there are severe restrictions on the delay for decision making in the system, a more complete comparison of all decoding algorithms has to be made.

For channels with a complex structure of errors, modeling the operation of decoders is evidently a mandatory stage in the design of all systems that use noise-immune codes. In doing so, all methods discussed in this chapter and cascade codes can be used.

The simple block codes, discussed above, that combine the advantages of ease of implementation and rather high degree of protection against errors when the noise level is small, are now fully acceptable during data input and storage.

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Chapter 3. Data Transmission Network Reliability

3.14. Conclusion

The results given in this chapter permit analyzing the characteristic of reliability (structural and functional) of communication networks used as the basis for data transmission networks. The analytic methods given here provide for precise or approximate computer computations of network reliability performance. These methods include:
the method of computing the probability that at any given time, communication is possible between any two nodes of an arbitrary subset of the communication network nodes (capacity of subset varies from 2 to n, where n is the number of network nodes);
the method of computing that at any given time, the condition is met for reliable network operation specified by an arbitrary Boolean function;
the method of computing the mathematical expectations of the time of faultless operation and the time of recovery of network communication; and
the simulation model for determining the laws of distribution of the time the communication network stays in the communication and noncommunication states.

Also given in this chapter are the methods for solving the problem of synthesizing the communication network configuration with a specified reliability under the condition of various limits on redundancy introduced into some initial configuration to enhance its reliability. These methods provide for precise or approximate solution to the synthesis problem on computers. These methods include:
the method of synthesizing the optimal configuration, i.e. configuration of a communication network with a specified reliability at minimum cost for network redundancy;
the method of the weakest section, which is a heuristic procedure for finding the configuration with the required reliability using the least possible number of redundant communication lines or at the least cost for them;
the method of synthesis of the extremal configuration of the communication network, from which the elimination of even one reserve communication line would lead to a decline in its reliability performance to a level below that specified; and
the method of synthesizing a configuration for a reliable communication network,

built on a base of broad heuristics that provides for an approximate solution to the problem of synthesizing the optimal network configuration.

The results given in this chapter can be applied and have already been applied in practice in the design of data transmission networks.

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DESIGN PRINCIPLES FOR COMPUTER NETWORK UPPER LEVELS

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[Excerpts] Discussed is a scheme for designing the upper levels of computer network software that in contrast to traditional schemes is based not on the sending (receiving of messages), but on calling of procedures in abstract objects. Levels 7-4 of the standard ISO model are reduced to one level. Advantages of this scheme compared to traditional schemes are shown: reduced cost for software development and operation, expanded functional capabilities with reduced resource cost and two-way network transparency.

ISO Model

A major problem apart from those discussed in the preceding sections concerns the ISO model, or more precisely, levels 7-4 of it. From a scientific and technical viewpoint, it seems to us the problem is rather clear. The ISO model as far as levels 7-4 are concerned is unsatisfactory at its very basis. This is evidenced in particular by the fact that the very authors of the model [2] were unable to decompose the protocols of the virtual terminal and sending of jobs and files by model levels.

In the proposed four-level model, the problems are solved much more simply; however, one can easily image the "political" difficulties of introducing it.

Conclusion

Discussed in the article is a scheme for designing network software as an alternative to that suggested in levels 7-4 of the ISO model. The main difference is that the suggested scheme is based on interaction of abstract objects (subsystems) effected by a call of procedures in these objects. The ISO model is based on

process interaction effected by sending and receiving messages. Placed above level 3 in the suggested model is the UDV [remote call] level which is the last in the system network software. It is found that the applications level does not actually have the specific nature of a network and in the majority of cases is reduced to local application software.

Implementation of the upper layers of the SEKOP [Multiuser Computer Network] [3] has confirmed a number of advantages of the approach in question:

1. Two-way network transparency is provided for. On the one hand, a user of the subsystems available on the network calls operations in them without concern as to whether these subsystems are local or remote relative to him. On the other, the subsystems (procedures in a subsystem) are independent of how they are called, locally or remotely. Thereby a simple interface can be provided between the users and preparers of subsystems in the form of agreements on communications when procedures are called. In the process, a local case is implemented efficiently.

2. Costs are reduced for developing applications subsystems since development of specific protocols is eliminated. With that, distributed programming is actually reduced to local.

In particular, during the development of the SEKOP network, implementation, for example, of sending jobs was reduced actually to writing interface procedures for the local system to start jobs and took several weeks in contrast to the several years usually needed to develop and implement traditional protocols.

3. Network software logic becomes more unified and transparent.

4. Data representation conversions can be naturally reduced to conversion of built-in types.

5. The universal protocol does not cause "superfluous" messages and deterioration of response times.

6. Coordination and standardization are required for one universal functional protocol (standards at layers 1-3 have largely been established). For comparison, let us point out that the ISO model requires standardization of protocols for layers 4 and 5 and a potentially infinite number of protocols at layers 6 and 7.

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IMPLEMENTATION OF NETWORK ACCESS TO SOFTWARE PACKAGES ON EXPERIMENTAL COMPUTER NETWORK

Moscow PROBLEMY MSNTI: INFORMATSIYA, UPRAVLENIYE, SISTEMY in Russian No 2, 1981 (signed to press 28 Sep 81) pp 18-24

[Article by Eduard Aleksandrovich Yakubaytis, academician, Latvian SSR Academy of Sciences, and director of the Institute of Electronics and Computing Technology, Latvian SSR Academy of Sciences]

[Text] Two alternatives are discussed for organizing network access to software packages on the Unified System of Computers which have been implemented on a Latvian SSR Academy of Sciences' experimental computer network.

Keywords: computer networks, network access, software packages, network protocols

Computer networks are the highly efficient base for the modern information processing industry. The first stage of their development was the creation of tree-like centralized networks in which n subscriber stations were connected to one computer through communication channels. In the second stage, the capability of combining a small number of "trees" together emerged. And, finally, in the third, currrent stage, distributed computer networks are being created; their topology is determined by the efficiency of execution of all processes of information processing.

Solving the varied network problems is enabled by specialization of systems shown in the table.

No	System	Tasks executed by system
1.	Working	Making network resources available: storage of data files; information retrieval; execution of computing operations; simulation of processes, phenomena and objects; software development
2.	Terminal	Use of network resources: terminal operation control, job preparation, interface with industrial processes for measurement and control of them
3.	Communication	Routing of flows of files of information sent between working or terminal systems

4. Administrative — Administrative control of computer network (collection of statistics, operation accounting, reports, malfunction diagnostics, reference information on network operation, etc.)

The working, terminal and administrative systems are called subscriber systems. Subscriber systems meeting the standards for interface to the data transmission network are connected directly to the communication systems. If a subscriber system does not meet these standards, it is connected to a communication system through a network logic element called an interface module. Each system is implemented in a complex consisting of one or more computers.

Working complexes enable making the most varied information and computing resources available to a broad group of users. Most efficiently used in them are computers especially developed for networks. The machines already produced under the Unified and Small Systems are not designed for networks. However, after taking special measures, successful implementation of working systems can be achieved with these computers.

There are three methods for connecting a working complex built with one or more Unified or Small computers.

The first of them: the subscriber complex is connected to an interface converter of the communication complex through a standard data transmission multiplexer (MPD) or data teleprocessing processor (PTD). This converter, which implements the interface module, looks like a standard subscriber station to the MPD (PTD), and a standard (for the network) subscriber complex to the communication complex.

The second method is logically equivalent to the first. However, here the interface module is implemented not in the equipment linked to the communication complex, but in the PTD, a mini or micro computer, linked directly to the subscriber complex.

The third method for connecting a working complex: special programs enabling creation of the network access method are written for Unified or Small computers. Then, after adding a network adapter to the working complex, it can be connected directly to the communication complex [1].

Let us consider two alternatives for organizing access to software packages (PPP) on the Unified System of Computers (KAMA, OKA, DUVZ, POISK-1, etc.) by using the network access method and the IRPR [radial parallel interface] network adapter (parallel transmission).

The first alternative consists in adding the network access method (SMD) to the software package. In doing so, the access method becomes, as it were, an integral part of the package and is used to implement the required programs. Note that application programs that operate in the package environment remain unchanged.

The second alternative consists in developing special software that implements the interface between the package and network. This alternative does not require making changes to the package. With that, the network access method is subdivided into logical and physical parts. The logical part emulates a standard device or group of devices and is implemented in the form of a logical interface converter (LOGIP).

The physical part is associated with support of the transport network protocols and is implemented in the form of a transport station (TS).

Let us dwell in more detail on each alternative.

The first alternative, the software package/network access method system, along with standard system terminals supports operation of remote terminal machines (TM) in the mode of multiaccess to software packages functioning on a working machine (RM) in the YeS OS operating system environment by using the network access method [NAM] [2].

The version of software (PO) of the software package/NAM consists in an extension of the package control program functions, development of additional program modules and modification of package control tables to support the mode of multiaccess of terminal machines through the communication complex to the software packages by network protocols.

The NAM is the basic access method and consists of a set of macro instructions and macro definitions that are stored in a system library, the input/output module loaded to user main storage and the real-time supervisor (SRV) as the basic complexing facility.

A request for use of the NAM which advises of the presence of a task that requires its services and loading of the input/output module to main storage are effected by the macro instruction AOPEN, which also opens the ADCB block previously built by the corresponding ADCB macro instruction. The block contains references to NAM modules and control blocks used by real-time supervisor during input/output and dispatching operations.

Input/output [IO] functions are performed by the macro instructions AREAD, AWRITE and ACNTRL, which initiate, respectively, read and write operations and transfer of control instructions. Access to the IO module occurs through these macro instructions; the module builds the channel program and IO control blocks and transfers control to real-time supervisor, which starts the IO operation and returns control to the program through the IO module.

The NAM supports sending "attention" signals to user programs for attention processing. An "attention" program for a given device is assigned by the macro instruction ASPAR, which opens the attention control block built earlier by using the macro instruction ASAEC. To synchronize IO operations with other program sections, the macro instructions AWAIT and APOST have been developed.

The macro instruction ADAR is used to disable a user's attention handling routine and discontinue communication between the "attention" control routine and real-time superviser. At the same time, the "attention" control routine is deleted from main storage.

The software package/NAM software, making use of NAM services, organizes:
--initiation of IO operations upon external or application program requests
--completion of handling of network protocols
--diagnostics of error situations during reception/sending of messages through the adapter

--multiaccess from terminal machines to indpendent system and application programs functioning in the operating environment of the software package/NAM
--conversion of network protocols to software package terminal protocols
--accumulation of statistical data during input/output of data, and
--multiplexing and demultiplexing of input and output data queues.

Thus, this alternative provides the capability of using software packages on a network.

The advantages of this alternative are:
--savings of main storage
--no need for development of additional support save for the access method modules
--and network software affects only the functional layer of a software package and not application programs.

The shortcoming of this alternative is that the software package operates directly with the network adapter and is independent of protocols used in the network.

The second alternative is to interface the software package with the network outside the package by developing special program facilities, the logical interface converter (LOGIP) and TS (transport station) which perform NAM functions [3].

LOGIP and TS software is based on the modular principle.

The general structure of the LOGIP is shown in fig. 1.

After receiving control from the operating system, the loader:
--starts the task of emulation of the data transmission multiplexer and subscriber stations (REM),
--starts the transport station (TSTATION) task, and
connects the nucleus.

The loader also handles REM and TSTATION abnormal ends of tasks and completion of the REM and TSTATION tasks.

Loader program modules are:
--module for starting REM and TSTATION tasks and connecting the LOGIP nucleus,
--module for handling REM and TSTATION ABEND's, and
--module for completion of LOGIP operation.

The LOGIP nucleus performs analysis of all SVC instructions issued in the system to identify the EXCP (CVC ∅) instructions. The EXCP instruction is generated when it is necessary to request

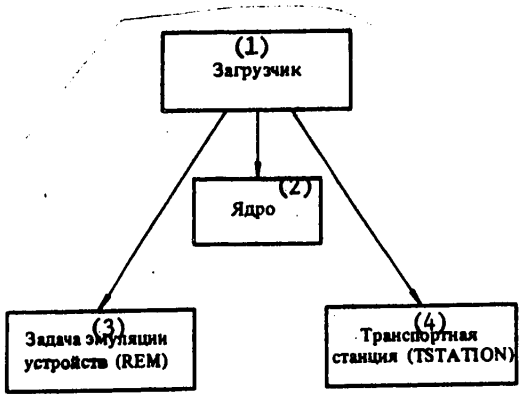

Fig. 1. General structure of LOGIP [logical interface converter]

Key:
1. loader
2. nucleus
3. device emulation task (REM)
4. transport station (TSTATION)

the operating system to execute an IO operation. While analyzing all EXCP instructions, the nucleus selects those instructions issued to devices emulated in the LOGIP and uses the POST/WAIT apparatus to send the instruction to the REM task for processing of the EXCP.

The task of emulating a standard device or group of devices (REM), with which a software package operates in a data teleprocessing system, effects simulation of the data transmission multiplexer and user subscriber stations. Required in the process are:
--data recoding
--reformatting of messages to be sent, and
--translation, processing and execution of instructions of the emulated device or group of devices.

Interaction of the modules is effected on the basis of the control tables.

The AVT (Address Vector Table) is the main LOGIP control table. Interaction between the REM and TSTATION tasks is based on this table.

The TSU (Table Status Unit) is used to describe each unit emulated in the LOGIP. Each entry in the table contains the address of the emulated unit and designates the logical channel corresponding to it.

The TCMT (Task Control Master Table) contains the symbolic names and addresses of points of entry to the modules that process the macro instructions of the basic telecommunications access method (BTMD) [BTAM]. The size of this table depends on the number of BTAM macros emulated in the LOGIP.

The REM task program modules are (fig. 2):
--starter
--dispatcher
--input/output supervisor
--BTAM macro processor
--task supervisor, and
--module for completion of REM device emulation program.

Starter prepares the REM program for functioning.

Dispatcher generates the list of addresses for the Event Control Blocks (ECB) for which the special flag is set for including the ECB in the queue. In the LOGIP system, there are: an ECB for each of the emulated units, an ECB for expectation of the arrival of data or an instruction from the transport station, an ECB for expectation of the arrival of the receipt for transfer of data by the transport station, and an ECB for expectation of the event of emulation program completion. Expectation of the events described by these ECB's is effected in the dispatcher.

The IO supervisor effects transfer of data and instructions upon requests from the processors of BTAM macro instructions and TS. When a request from TSTATION for receiving data is received, the dispatcher performs transfer of control to the IO supervisor. The IO supervisor is built from several independent program modules. After receiving the data, the IO supervisor sends a receipt to TS and transfers control to either the task supervisor or the dispatcher.

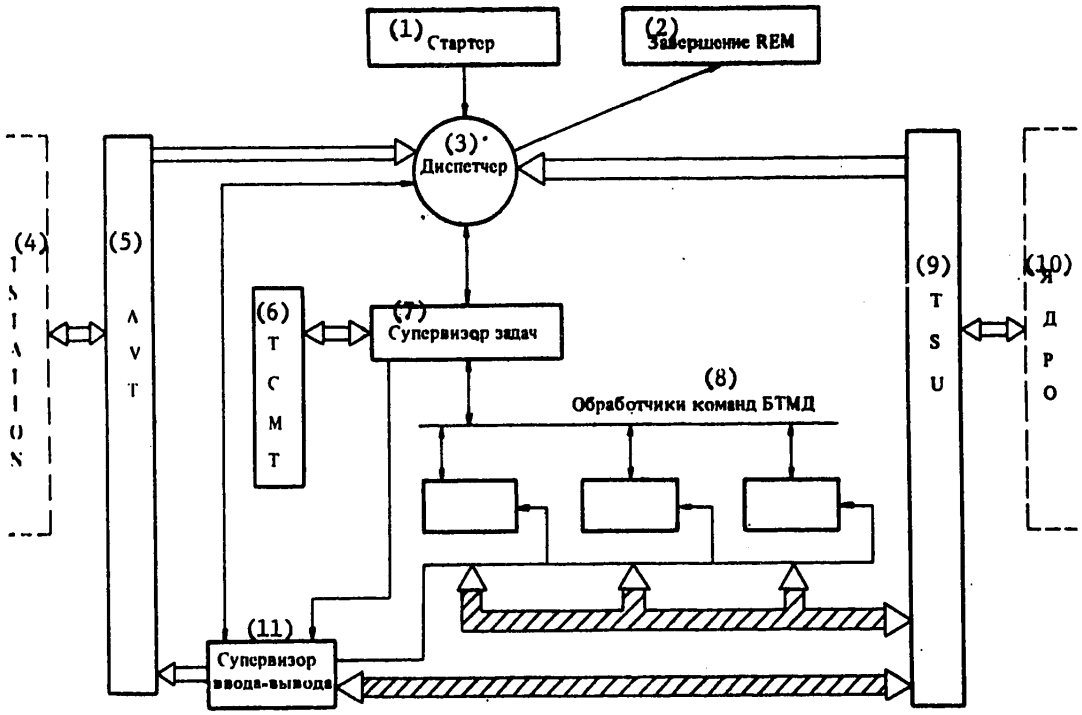

Fig. 2. REM task program modules

Key:

1. starter
2. completion of REM
3. dispatcher
4. transport station
5. address vector table
6. task control master table
7. task supervisor
8. BTAM instruction handlers
9. table status unit
10. nucleus

The BTAM macro instruction handlers process the corresponding BTAM macro instructions and forward IO requests to the task supervisor. They are loaded to main storage by the starter and receive control from the task supervisor when the appropriate BTAM macro instruction is issued by the user.

The task supervisor controls the BTAM macro instruction handlers and transfers control to the appropriate IO supervisor entry points when IO requests are forwarded by the handlers.

Completion of the device emulation program begins when the dispatcher receives an instruction for termination from the loader. Upon termination, storage requested for the buffer for the messages and the list of addresses for the ECB's is cleared, the BTAM macroinstruction handlers are cleared, and control is returned to the operating system.

The transport station is a system of program modules intended to perform two basic functions:
--set up and maintenance of operation of logical channels, and
--support of data transmission by physical communication channels.

Responsible for implementation of these functions are the appropriate subsystems for control of the logical (SULK) and physical (SUFK) channels.

SULK performs the functions of the transport layer of the experimental computer network, implementing organization of the logical channels and maintenance of communication sessions, assembly and disassembly of messages and control of their flows, and the functions of interface between the LOGIP and the TS.

SULK has the following structure:
--TS initializer
--TS scheduler
--TS terminator
--TS request handler
--interpreter and protocol instruction preprocessor.

The TS initializer issues the NAM instructions AOPEN and ASPAR, opening data sets for operation with the adapter and monopolizing IO processing from this unit.

The TS scheduler plans TS operations. When there are no requests for TS services, TS is in a wait state, after issuing the macro instruction AWAIT for the list of ECB's of expected events.

The TS terminator receives control when there is a request for TS termination. Forwarding the NAM macro instruction ADAR, it disables TS access to burst use of the adapter. The macro instruction ACLOSE terminates use of NAM by the transport station.

The interpreter interprets LOGIP-TS interface instructions. It discerns logical instructions and requests for data transmission to the network. Logical instructions are requests for opening/closing of logical channels. When these requests are made, control is passed to the protocol instruction preprocessor.

If the length of the message to be transmitted exceeds the maximum packet length established by the administration for the experimental computer network, the interpreter breaks up the message into packets and sends them to the SUFK.

The protocol instruction preprocessor performs operations to open/close logical channels and advise LOGIP of completion of these operations. The module analyzes protocol instructions, noting the logical channel state.

The SUFK is the program implementation of the network and channel levels of the experimental computer network. In accordance with this, the SUFK performs the functions of generating the packet, routing packets, making up the frame, transmitting data over the physical communication channel, handling malfunctions during data transmission over the physical channel and interacting with the SULK.

The physical channel control subsystem (SUFK) has the following structure:
--packet control module
--channel dispatcher
--transmission module
--instruction analyzer
--frame transmission completion module
--frame retransmission module
--data reading module
--TS data processing module, and
--data receiving module for the LOGIP.

The packet control module, after receiving control from the SULK, copies the data into its own area and generates packet headers, noting the numbers of the logical channel and group logical channel. This ensures delivery of the data to the necessary user through a virtual chain.

The channel dispatcher performs the functions of allocating the physical channel between the LOGIP and the TS. Using the exchange log, the dispatcher informs SUFK of the information source and number of malfunctions during data transmission. The module also makes up and packs data packets into a frame and makes up frame headers.

The transmission module effects direct transmission of data over a physical channel. It initiates transmission by using the NAM macro instruction AWRITE and analyzes the completion of an IO operation.

The instruction analyzer receives the instructions that have arrived from the adapter, forwarding the NAM instruction ACNTRL.

The analyzer also checks for adherence to the channel protocol. When the protocol is violated, an error meesage is sent to the console and the instruction received is ignored.

The frame transmission completion module clears the exchange log for further use.

The frame retransmission module receives control when there is a negative receipt for frame transmission. It notes the number of repeat tranmissions. When this number does not exceed the maximum specified by the protocol, the module calls the channel dispatcher with a request for frame retransmission. When this number is exceeded, the communication channel is considered out of order.

The data reading module receives control when the adapter sends a "read" instruction. Making use of the NAM macroinstruction AREAD, it reads the arriving data into its own buffer and checks for completion of the IO operation.

When the IO operation is completed normally, the module sends the originator an explanatory receipt, using the NAM macroinstruction ACNTRL, and transfers control to the operating system.

The TS data processing module receives control upon completion of transmission of a packet belonging to the TS, and also if data has been received through a logical

channel that had not been opened. The module controls the queue of messages, the source of which is the TS itself.

If the TS has received a message through a logical channel that had not been opened by the LOGIP, this module prepares a message to the user through the corresponding logical channel on the lack of facilities, the services of which were requested, and puts this message in the TS message queue.

Upon completion of TS message transmission, the module orders the message queue and informs the TS scheduler of the presence of messages for transmission.

The data receiving module for the LOGIP receives control when a logical channel has been opened by LOGIP for data transmission. The module informs the LOGIP of the presence of a message and sends it the data buffer address. After receiving a positive receipt, the buffer is considered free.

The module analyzes the sequence bit of the message packets and when necessary, performs assembly of the message.

This software design principle for the LOGIP and the TS permits affording simplicity of further expansion of system capabilities by incorporating new modules.

The advantage of the second alternative is that there is no need to make changes to the software package to enable its interface with a network. In the process, the software package is independent of the complexing units and the TS protocols. The shortcoming of this alternative is the high cost for software development.

Thus, as the more optimal by amount of additional software to be developed and system response time, the first alternative can be successfully used in specialized network software packages.

The second alternative is universal in the sense of adding to the nomenclature of software packages used and can be recommended as standard for networks built on the base of Unified System computers.

By using these methods, the following Unified System software packages have been connected to a network: DUVZ [conversational remote job entry], KAMA, OKA and POISK-1.

Now being implemented are the network access method and network adapter that follow the X.25 standard for connecting a working complex directly to a communication complex with the serial method of transmitting information.

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ROLE OF TERMINAL STATIONS IN COMPUTER NETWORKS

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[Article by Viktor Mikhaylovich Bryabrin, candidate of engineering sciences, sector manager, Computer Center, USSR Academy of Sciences]

[Excerpts] The generally accepted view of architecture of computer networks assumes that the basic functions for user information and computing service are performed by base (host) centers, while terminal stations together with channels and communication centers provide only transparency for the information to be sent. In this work, an analysis is made of an approach under which terminal stations implemented as personal computer systems provide users with far more service functions than under the traditional approach. Two nontraditional functions of terminal stations are discussed: 1) preparation of object or load modules for their execution on base center computers, including input of source programs, their editing, debugging and cross translation; 2) creation of an "intelligent interface" to a computer network, including an information reference system on its components, formation of a user's view on types of service and others.

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COMPUTER NETWORKS: PATH TO DEVELOPMENT OF INTERNATIONAL INFORMATION SERVICES

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[Article by Khinko Mikovich Khinov, professor and deputy director, and Vladimir Nikolayevich Kalachev, candidate of engineering sciences and senior scientific associate, both from the International Scientific Research Institute of Control Problems]

[Excerpts] State of the art of international information services based on computer networks is analyzed. Trends in development are identified. Various rates for use of information services are systematized. Efforts performed in socialist countries on organizing systems for communication with foreign computer networks and data bases are described.

Organization in Socialist Countries of Systems for Communication with Foreign Computer Networks

Several socialist countries now have efforts underway to establish systems for communication with computer networks in the United States, Canada and Western Europe. Interest in setting up these communication systems was evoked primarily by the capability of an outlet to the major foreign data banks and computer networks and of studying making the information and computing resources of their own countries commercially available to foreign users.

A number of socialist countries, members of the International Institute for Applied Systems Analysis (IIASA) in Laxenberg, Austria, use its communication center for an outlet to foreign computer networks. Establishing communications through the IIASA allows use of the experience, gained in IIASA, on setting up computer networks [8, 9] and resolution of a number of organizational problems.

Communication with the IIASA was set up centrally by establishing in each country a Center for Automated Access (TsAD) [CAA] to the IIASA. Within the country, access to foreign computer networks and data bases must be effected through the CAA.

The CAA's technical equipment must provide for:
--convenient access in the interactive and batch modes to IIASA information and computing resources, and through the IIASA, to the foreign computer networks
--continual reporting on all connections

--prevention of unauthorized access to external resources, and
--establishment of an additional level of information protection with a record of data and messages received and sent.

The CAA also has to make access available to national users remote to it. In connection with this, it has to be noted that a centralized access system will be profitable when it has a large number of users.

The main administrative functions of the CAA include:
--providing the legal and financial bases for access to foreign resources
--administrative monitoring and access control
--maintenance of the archive containing the communication protocols, and
--establishment of necessary working contacts with national organizations responsible for setting up computer networks in their own countries to introduce expertise in using foreign information and computing resources.

Systems for automated access to foreign computer networks and data banks are being set up in the VNR [Hungarian People's Republic], the PNR [Polish People's Republic], the USSR and the CSSR [8-11]. Experience in setting up these systems and the little operating experience gained so far have shown that the main difficulties occur in solving organizational, financial and legal problems, but not technical, since there is now sufficient experience in organizing national computer networks in these countries. Organizing access to foreign computer networks through the IIASA has contributed considerably to simplifying technical problems.

For communications, Hungary uses Hungarian TRA-70 computers, a leased communication line and the X.25 protocol [10]. The solution to the financial and legal problems is of interest. During the experimental operating period, costs are being paid centrally. This is because at this stage in view of the still in sufficient number of users, it is inexpedient to introduce a regulating system of payment by the users themselves for access to the foreign information and computing resources. Therefore, in Hungary, the main costs are paid by the State Committee for Development of Technology. These include funds for purchase of equipment needed and payment to foreign firms for information and computing services granted. Costs for use of the communication line are borne by the Hungarian Post Office. System operating costs are borne by the organization that set up this system, the Research Institute of Computer Technology and Automation of the Hungarian Academy of Sciences. In the experimental stage, computer users can access foreign computer networks and data banks during 60 hours per week. An hour of operation costs 60 to 80 dollars and depends on the type of operation and data base. Contracts with the foreign firms that make the information and computing services available were concluded through the foreign trade firm, the VNR METROIMPEKS. In 1980, contracts were made with Lockheed and the European Space Agency (ESRIN).

Used for communication with the IIASA in the USSR is the NORD-10 communication computer and a dedicated communication channel routed Moscow-Prague- Laxenberg. The channel is time-multiplexed into eight asynchronous channels with a throughput of 300 baud and one synchronous channel with 2400 baud. The synchronous channel is allocated for development of packet switching, which will be implemented on the base of the SM-4. Financial problems are resolved the same as in Hungary, centrally, in the experimental stage of operation of the automated access system. The basic costs are borne by the USSR State Committee on Science and Technology. Costs

for maintaining the system are borne by the organization that set it up, the All-Union Scientific Research Institute of Systems Research. Connected to the CAA in Moscow are users from Kiev, Leningrad, Novosibirsk and Riga as well as numerous users in Moscow itself.

At the start of 1981 in the CSSR, a communication system was connected to the Moscow-Prague-Laxenberg communication channel and uses four asynchronous 300-baud channels. Experimental operation of the system started in mid 1981.

Efforts are underway in Poland within the framework of the "Computer Network" research program to set up an inter-VUZ computer network. Putting a network of three centers into operation was planned in the first stage in 1981. One center will be connected to the IIASA communication line and will provide access for national users to foreign computer networks and data banks. As the network expands, the number of CAA users will also increase.

Communication systems between the socialist countries and West European computer networks, interexchange of information in national data banks and connection of national users to CAA's can be effected on the basis of Unified Computer System hardware. An example of the capability of implementing computer networks based on Unified Computer System hardware is the experimental communication line between Moscow and Kiev computer centers [12]. Used to link the YeS-1040 and YeS-1030 computers in it were YeS-8403 data transmission multiplexers, 8010 modems, a four-wire connecting line to link the computer centers to an international telephone station, and an international telephone channel.

Conclusion

With the emergence of computer networks, information services have expanded considerably, the number of users is continually increasing, and international information servicing is developing rapidly. This has caused a need for further development of data bases to meet the continually growing user demand for information from the various fields of human knowledge. The income of firms from providing information services is continually increasing: average annual income growth rates are 15 percent. Let us note that the export of information services is a very unique form of international trade, in which the sale of the commodity does not reduce its supply in the exporting country and requires no nonrenewable national resources.

The lack of legislation on setting up and operating international computer networks in the majority of West European conutries at the start of the period of development of international information servicing based on computer networks facilitated the rapid monopolization of information services by U.S. firms. Laws are now being passed or prepared in the West European countries to restrict the entry of American firms into this area and promote development of national information computer networks.

Since the time of emergence and development of information services based on computer networks, the pricing system has undergone several changes on the information market. Since the mid seventies, transfer of data bases by creating firms to operating firms has changed from a rental to a license basis. The cost of

author's rights (royalties) for data base creating firms has increased, but this has not affected the growth rate of demand on the information market. Among the system of payment by the user for operation with a data base to an operating firm, used most often are systems of payment by the hour, dependent or not dependent on the data base, and a payment system depending on the type of operations on the computers.

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COMPLEX OF MODELS FOR DESIGN OF TOPOLOGY OF COMMUNICATIONS OF TERRITORIAL INFORMATION AND COMPUTING CENTERS WITH REGARD TO RELIABILITY

Moscow PROBLEMY MSNTI: INFORMATSIYA, UPRAVLENIYE, SISTEMY in Russian No 2, 1981 (signed to press 28 Sep 81) pp 43-48

[Article by Pavel Ivanovich Bratukhin, doctor of engineering sciences and department chief, and Vadim Arnol'dovich Gadasin, candidate of physical and mathematical sciences and sector chief, both from the All-Union Scientific Research Institute for Organization and Control Problems of the USSR State Committee on Science and Technology]

[Excerpts] Discussed is a complex of models for design of topology of information communication networks with regard to reliability. Topology is optimized based on successive improvement of initial structure. Economic algorithms have been developed to computer cost characteristics and network reliability parameters. The complex has been implemented in the form of a PL/1 software package.

PLOTTER. These are programs that organize output of graphic information on an ATsPU [alpha-numeric printer]. This section combines general-purpose and specialized programs. A printer has to be used because of the shortage of plotters in existing computer centers equipped with the Unified System of Computers. The general-purpose programs in the section allow output of an arbitrary plot on a working field with the dimension h X v, where h and v are the number of characters horizontally and vertically. Values of h and v are defined by the user. When h exceeds 128, the size of the printer carriage, the plot is output in several pages.

The interactive complex developed allows improving a communication network configuration that includes up to 500 objects and up to 1000 communication channels. The complex has been implemented in the PL/1 algorithmic language and is intended for operation on Unified System computers using the OS 4.0 or OS 4.1 operating system. The catalog, organized on disk after translation, which includes on the order of 35 programs, requires about 150K bytes of storage. In the case of optimizing a network of 100 objects on the YeS-1040 computer, on the order of 100K bytes of main storage are required; the time for inclusion or exclusion of an optimal branch ranges from 0.5 to 1 minute for determinate criteria and to 7-10 minutes for stochastic criteria. In the NET version of the package, all programs are stored in a common library on magnetic disk and program interaction is controlled automatically by YeS OS facilities.

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DESIGN PRINCIPLES FOR STRUCTURE OF SHARED-USE COMPUTER SYSTEMS IN STATE COMPUTER CENTER NETWORK

Moscow PROBLEMY MSNTI: INFORMATSIYA, UPRAVLENIYE, SISTEMY in Russian No 2, 1981 (signed to press 28 Sep 81) pp 49-59

[Article by Aleksandr Petrovich Aleshin, candidate of engineering sciences and sector chief, Oleg Sergeyevich Konstandenko, candidate of engineering sciences and senior scientific associate, Gennadiy Viktorovich Ross, candidate of engineering sciences and senior scientific associate, and Leonid Grigor'yevich Rykov, department chief, all from the All-Union Scientific Research Institute of Organization and Control Problems of the USSR State Committee on Science and Technology]

[Excerpts] Discussed is the problem of designing shared-use computer system (VSKP) based on selected system of efficiency criteria. Design principles for VSKP structure are suggested. Basic algorithms are given to solve the problem of designing VSKP for the State Computer Center Network.

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LANGUAGE FOR DEVELOPMENT OF PROGRAMS WITH DISTRIBUTED STRUCTURE IN COMPUTER NETWORKS

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[Article by Anatoliy Fedorovich Dedkov, candidate of engineering sciences and sector chief, and Artur L'vovich Shchers, candidate of engineering sciences and department chief, both from the All-Union Scientific Research Institute of Organization and Control Problems of the USSR State Committee on Science and Technology]

[Excerpts] An experimental expansion of PL/1, oriented to operation in computer networks, is described. It includes facilities for list processing, subtask interaction, data exchange through a communication network and exchange with local terminals. The implementation, made on the Unified System of Computers, permits the user to define new types of data and include new statements in the language.

Conclusion

The RPL/S language has now been implemented on the Unified System of Computers by using a general-purpose RPL converter. It is undergoing experimental operation within the framework of the efforts on development of an experimental network of computer centers. Early results indicate the language is convenient and easy to learn. This is an experimental language and it may be recommended for broad application only after comprehensive tests and discussion. But there is no doubt of the need for programming languages oriented to operation in computer networks which will increase as this area of computer technology develops.

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EVALUATION OF TIME OF MESSAGE TRANSMISSION BY DATAGRAM METHOD IN COMPUTER NETWORK

Moscow PROBLEMY MSNTI: INFORMATSIYA, UPRAVLENIYE, SISTEMY in Russian No 2, 1981 (signed to press 28 Sep 81) pp 68-70

[Article by Rashit Biktimirovich Baybulatov, candidate of physical and mathematical sciences, Lyudmila Yur'yevna Bedova, senior scientific associate, and Lidiya Ivanovna Ivanushkina, senior scientific associate, all from the All-Union Scientific Research Institute of Organization and Control Problems of the USSR State Committee on Science and Technology]

[Excerpts] Evaluation is made of mean delay time for nonpriority message when data is transmitted by datagram method.

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8545
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APPROXIMATE METHOD FOR COMPARATIVE EVALUATION OF COST OF DISTRIBUTED SYSTEMS OF DATA BASES

Moscow PROBLEMY MSNTI: INFORMATSIYA, UPRAVLENIYE, SISTEMY in Russian No 2, 1981 (signed to press 28 Sep 81) pp 71-75

[Article by Inel' Alekseyevna Zotova, candidate of engineering sciences and sector chief, Lyubov' Mikhaylovna Feofanova, senior scientific associate, and Artur L'vovich Shchers, candidate of engineering sciences and department chief, all from the All-Union Scientific Research Institute of Organization and Control Problems of the USSR State Committee on Science and Technology]

[Excerpts] A centralized data base and two types of distributed data bases are comparatively analyzed by using cost criterion. Formulas are derived for approximate evaluation of cost of different data base systems. Some results are derived and discussed.

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EFFICIENCY OF INFORMATION EXCHANGE IN COMPUTER NETWORKS

Moscow PROBLEMY MSNTI: INFORMATSIYA, UPRAVLENIYE, SISTEMY in Russian No 2, 1981 (signed to press 28 Sep 81) pp 76-84

[Article by Stanislav Ivanovich Samoylenko, doctor of engineering sciences, professor, and deputy chairman of the Scientific Council on the Complex Problem "Cybernetics" of the USSR Academy of Sciences]

[Text] Basic principles of functioning and procedures for access to an adaptive switching network are considered. The adaptive switching method is comparatively analyzed with other known methods: packet switching, channel switching, and hybrid switching with fixed and floating threshold. Comparison is made by criterion of useful utilization of network path throughput. It is shown that adaptive switching provides a gain in throughput utilization, offering a universal set of transmission capabilities in the mode of packet and channel switching or by dedicated (permanently switched) channels.

Keywords: computer networks, adaptive switching method, packet and channel switching, hybrid switching, network path throughput, comparative analysis

1. Introduction

To achieve high efficiency in a general-purpose data transmission network, the following main requirements have to be met:

1. Capability of interaction through network of existing teleprocessing facilities without changing software.

2. Capability of interaction through the network of future teleprocessing systems based on international standards.

3. Achievement of efficient use of expensive throughput of network paths.

4. Achievement of capability of data transmission in various modes, including real-time transmission and direct interaction between computers.

These requirements are not met in a network based on one switching method taken individually. Thus, in particular, a channel switching (KK) [CS] network does not meet requirement 3; a packet switching (KP) [PS] network does not meet requirements 1 and 4; and using permanent (dedicated) channels (PK) [DC] does not meet requirement 3.

In connection with this, for general-purpose networks, it is advisable to apply hybrid switching methods that achieve an efficient path load when the CS, PS and DC modes are combined.

These capabilities are possessed by the adaptive switching (AK) [AS] method, which combines PS, PS and DC with achievement of efficient use of network path throughput [1-5].

Discussed in this article are the general principles for designing an adaptive switching network and procedures for access to a network based on the standard X.25 and X.28 protocols, and adaptive switching is compared to the other methods.

The main switching methods used or under development for use in digital communication networks are: CS, PS, hybrid switching (GK) [HS] with fixed (GKFP) or floating (GKPP) threshold [6].

In comparing AS with the other transmission methods, we will use the following technique.

For a specified type of traffic and path capacity, the maximum flow achievable in the mode of CS, PS, GKFP and GKPP will be evaluated when the specified requirements for service are met. Then AS will be evaluated by capability of achieving transmission of the same flows under the same requirements as that for the methods being compared, and additional capabilities (if any) offered in the AS mode will be determined.

In selecting parameters determining service quality, we will assume that in the CS mode, the transmission system is described by the model M/M/1 without a queue with failures and the basic criterion of service quality is the failure probability P_f.

In the PS mode, transmission will be described by the model M/M/N with queues without limitations, and the main criterion for evaluating transmission quality will be the mean packet delay time during transmission through network path τ.

The evaluation will be made under conditions of transmitting the following type of traffic. Transmission will be made by communication sessions of mean duration T_m. In each session, messages with pauses between them, the share of which equals h, will be transmitted.

2. Design Principles for Adaptive Switching Network

The adaptive switching network consists of nodes connected to each other by paths. Through each path, fixed-length frames, consisting of a specified number of octets, are transmitted. In each frame in the time-division multiplexing mode, tranmission in mode of CS, PS and DC is combined.

To transmit in the CS mode when connections are organized on all paths through which the connection passes, the frame positions assigned to the given connection are fixed. The request for organization of a connection is sent to the network in the form of a service packet or prescribed dialog with an asynchronous subscriber station.

In the DC mode, a connection is secured just as in the CS mode, but for a rather long period and by previous agreement with network administration.

The connection may be set up by the operator of a network input node by previous agreement with a subscriber.

In the PS mode, all frame positions are used that are not occupied at a given time by transmission in the CS or DC modes, including those temporarily free in organized connections because of pauses in messages being transmitted.

The adaptive network functioning principles are discussed in more detail in [1-5].

3. Procedures for Access to Adaptive Switching Network

In considering access procedures, let us give the procedures for existing and future teleprocessing systems.

3.1. Teleprocessing System with Permanent Channels

A teleprocessing system using dedicated channels can be implemented by connecting subscribers by trunk lines to the closest network node and organizing permanent channels in the network. In the DC mode with synchronous transmission, the network provides for transmission of blocks formatted in accordance with the protocol used in the given teleprocessing system. When interacting with an asynchronous subscriber, the network transmits characters one at a time or in a group between the computer and subscriber. Implemented on the trunck lines is the procedure for transmission of levels 1 and 2, adopted in the givtn teleprocessing system. In the simplest case, permanent connections can be organized through network operators. When software is used, service packets to set up and dismantle connections can be generated. Using DC does not cause reduction in efficiency of network path use thanks to the capability of filling the pauses in messages being transmitted.

3.2. Extension of the Standard X.25 Protocol

The standard X.25 protocol is intended for interaction with a network of synchronous subscribers in the PS mode with transmission through virtual channels or in the datagram mode. In the adaptive switching network, similar procedures can also be used for transmission in the CS mode. To achieve compatibility with the X.25 procedure in the AS mode, the CS mode can be earmarked by assigning appropriate groups of logical channel numbers to the PS and CS modes.

Thus, in particular, one can use the following distribution of logical channel groups:
group 0, for transmission in the datagram mode
group 1, for permanent virtual channels
groups 2-13, for switched virtual channels
group 14, for permanent channels
group 15, for switched channels.

In the process, to simplify dividing the data and service packets in the DC and CS modes, for each channel one can allocate two adjacent logical channel numbers, using one to send data and the other, service packets pertaining to this channel.

Since the distribution of logical channels is a local node function and the service packets used in the PS mode do not change, this access mode is fully compatible with the standard PS mode provided for by the X.25 recommendation.

3.3. Extension of the Standard X.28 Protocol

For asynchronous character-oriented terminals, an extension of the X.28 procedure, provided for the PS mode, can be implemented when describing the special services requested when the connection is organized, i.e. when the parameters are specified to implement interaction. In doing so, an additional parameter defining the switching method can be introduced.

The absence of this parameter indicates transmission will occur in the PS mode; presence of the parameter determines the CS mode. In the process, compatibility with the standard X.28 procedure is achieved, since no procedures provided for by X.28 are modified.

4. Comparison of Adaptive and Channel Switching

In using channel switching, one of N channels is made available for each communication session. If requests for communication sessions come in accordance with a Poisson distribution and the distribution of their duration is described by an exponential distribution, then the maximum input stream that can be served in the CS mode is determined by the condition [7]

$$P_f^{max} = \frac{(N\rho_{CS})^N}{N!\sum_{n=0}^{N}\frac{(N\cdot\rho_{CS})^n}{n!}}, \quad (1)$$

where P_f^{max} is the maximum permitted probability of failure to respond to a request to set up a communication session,

ρ_{CS} is the load factor for one channel of the path by the communication sessions in the CS mode, and

N is the number of channels in the path.

If P_f^{max} and N are given, then from expression (1) we determine ρ_{CS}, on which in turn the degree of use of network path capacity depends.

If ρ_{CS} is known, then the network path usage factor for transmission of data and service information for $P_f^{max} << 1$ is

$$H_{CS} \cong \rho_{CS}(1-h) \quad (2)$$

where h is the share of pauses in the transmitted messages.

When adaptive switching is used, we shall assume that the same traffic as in the preceding case is sent through the path in the CS mode. In the process, there will emerge the capability of sending in the PS mode additional traffic through part of

the path with capacity

$$C_{PS}^{CS} = C\ (1-H_{CS}), \tag{3}$$

where C is the network path capacity.

In the PS mode, with a Poisson stream of packets with an exponential distribution of their length, for a system with an unlimited queue, the maximum stream is determined by the condition [7]:

$$\tau_{max} = \frac{T}{1-\rho_{PS}}, \tag{4}$$

where τ_{max} is the maximum mean delay of packets permitted in the PS mode transmission,
T is the mean time for tranmission of one packet through the path (or part of it) with a specified capacity, and
ρ_{PS} is the capacity usage factor with PS.

Expression (4) determines the maximum value of the capacity usage factor with PS:

$$\rho_{PS} = 1 - \frac{T}{\tau_{max}}. \tag{5}$$

Based on what has been presented, one can formulate

Statement 4.1.

With identical traffic and equal qualitative conditions for CS mode transmission, adaptive switching affords the capability of additional data transmission in the PS mode with the maximum amount of transmission:

$$C[1 - \rho_{CS}(1-h)]\rho_{PS}.$$

Corollary 1. Maximum relative gain in path capacity usage with AS is

$$\eta_{AS/CS} = \frac{H_{AS}-H_{CS}}{H_{CS}} = \rho_{PS}\left(\frac{1}{\rho_{CS}(1-h)}-1\right). \tag{6}$$

Shown in fig. 1 is the relationship between $\eta_{AS/CS}$ and the share of pauses h when ρ_{PS}=0.6 and ρ_{CS}=0.3 and 0.6. Analysis of expression (6) shows that the gain with AS compared to CS increases as ρ_{PS} and h increase and declines as ρ_{CS} increases.

Key:
1. $\eta_{AS/CS}$
2. ρ_{CS} = 0.3
3. ρ_{PS} = 0.6
4. ρ_{CS} = 0.6
5. ρ_{PS} = 0.6

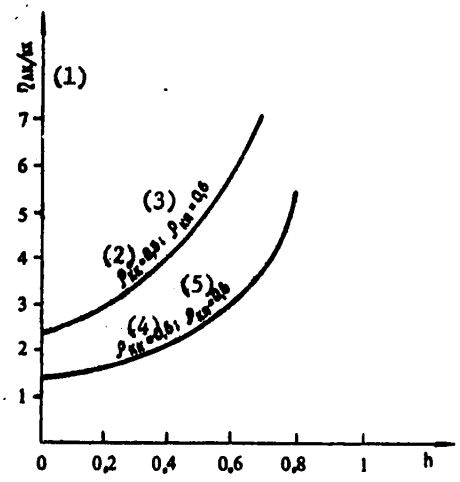

Fig. 1. Comparative evaluation of adaptive and channel switching

5. Comparison of Adaptive and Packet Switching

In comparing adaptive and packet switching, let us consider transmission of interactive traffic containing relatively short messages with long pauses between them. Comparing adaptive and packet switching in transmission of files is equivalent to the comparison of channel and packet switching which has been widely discussed in the literature [8].

Adaptive switching during transmission of interactive traffic may make use of the entire path capacity in the PS mode. However, transmission through the path in the AS mode differs from the transmission mode used in PS networks.

The difference is that in PS networks, each packet is formatted into a separate block transmitted over the path. Transmitted over the path in AS are fixed-length frames, each containing part of a packet, an entire packet or several packets as a function of the relationship between the length of the part of the frame used for packet transmission and the lengths of the packets to be sent.

In subsequent discussion, we will assume that the frames in the PS and AS modes, during transmission of them over the path, have an amount of service information equal to S^0_{PS} and S^0_{AS} respectively.

The mean number of packets sent in one frame when there are no switched channels is

$$N_p^m = L_f/L_p,$$

where L_f is the length of the information part of the frame, and

L_p is the mean packet length.

however, in a frame that may contain several packets, for example N_p, there is additional service information required to define the bounds between the jointly transmitted packets.

The size of this additional service information S_f can be determined from the following considerations. The service information entered must define the:
--number of full packets in the frame
--number of positions in the frame at which packets end, and
--flag of completeness or incompleteness of the last packet in the frame.
Consequently,

$$S_f = S_1 + S_2 + S_3,$$

where S_1 is the size of information needed to describe the number of packets in the frame:

$$S_1 = [\log_2 N_p^{max}] \text{ bits},$$

where N_p^{max} is the maximum number of packets that can be sent in a frame,

$[x]$ is the smallest integer equal to or greater than x, and

S_2 is the mean size of information needed to describe the separations between packets:

$$S_2 = [\log_2 L_f]\, N_p^m ,$$

where L_f is the number of positions in the information part of the frame,

N_p^m is the mean number of packets sent in a frame, and

S_3 is the size of information needed to describe the completeness or incompleteness of the last packet in the frame:

$$S_3 = 1 \text{ (bit)}.$$

In sending N_p^m packets in the packet switching mode, needed to frame the blocks in the network path are

$$S_{PS}=S_{PS}^0 N_p^m \text{(bits)},$$

where S_{PS} is the size of service information used to frame N_p^m packets in the PS mode.

In adaptive switching, needed to send N_p^m packets over the network path are

$$S_{AS}=S_{AS}^0 + S_f \text{(bits)}.$$

Based on what has been presented, the following conclusion can be drawn:

Statement 5.1.

In sending interactive traffic under the conditions when an average N_p^m packets are sent in a frame, AS affords better utilization of network path capacity, if this condition is met:

$$N_p^m > \frac{S_{AS}^0 + [\log_2 N_p^{max}] + 1}{S_{PS}^0 - [\log_2 L_f]}. \quad (7)$$

Example. Comparison of adaptive and packet switching with interactive traffic.

To illustrate the range in which AS affords more economic utilization of capacity than PS, let us consider expression (7) under the following conditions:

a) maximum number of packets in a frame $N_p^{max} = 16$, i.e.

$$[\log_2 N_p^{max}] = 4,$$

b) HDLC or BSC [binary synchronous communication] procedures are used to send the frames over the path. In the case of HDLC procedures [9], 6 octets are used for a frame, and we will assume that

$$S_{AS}^0 = S_{PS}^0 = 48 \text{ (bits)}.$$

In the BSC procedure with the transparent mode of transmission, framing consists of 10 octets, and we will assume that

$$S_{AS}^0 = S_{PS}^0 = 80 \text{ (bits)}.$$

Under these conditions, let us derive from expression (7) for the HDLC procedure

$$N_p^m \text{ (HDLC)} > \frac{53}{48 - [\log_2 L_f]}. \quad (8)$$

Similarly, for the BSC procedure, let us derive

$$N_p^m \text{ (BSC)} > \frac{85}{80 - [\log_2 L_f]}. \quad (9)$$

Fig. 2 shows the relationship between $\tilde{N}_p^m$ (HDLC) and $\tilde{N}_p^m$ (BSC) and the number of positions in the information part of the frame, L_f, where $\tilde{N}_p^m$ is the mean number of packets in a frame, above which AS is more efficient in capacity utilization than PS.

It can be seen from this graph that AS affords better utilization of capacity than PS when the frame length exceeds mean packet length by 20-40 percent when the HDLC procedure is used, or by 15-20 percent when the BSC procedure is used.

These conditions are easily met in practice. Consequently, always under real conditions, even when interactive traffic is sent which is most suited to PS, adaptive switching can afford better path capacity utilization. This gain becomes even more tangible when one considers that less redundancy is needed for forming the frame under the conditions of AS with a fixed-length frame than is the case for PS with a variable-length frame.

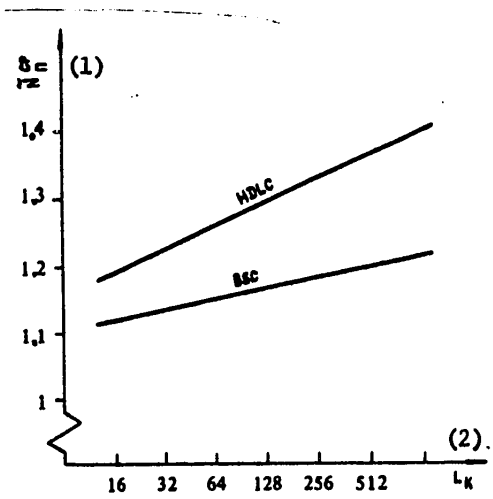

Fig. 2. Mean number of packets in a frame, above which adaptive is more efficient than packet switching

Key:
1. $\tilde{N}_p^m$
2. L_f

6. Comparison of Adaptive and Hybrid Switching

In comparing adaptive and hybrid switching, we will consider hybrid switching with fixed (GKFP) and floating (GKPP) threshold.

In evaluating AS, we will consider the use of it in which all HS functions are performed and certain additional capabilities are implemented, which also determine the advantages of AS.

6.1. Comparison of Adaptive and Fixed-Threshold Hybrid Switching

In using fixed-threshold hybrid switching [FxTHS], the network path is permanently divided into two parts, using one in the CS mode and the other in PS.

If of the total number, N, of channels in the path, N_{CS} are used in the CS mode and $N_{PS}=N-N_{CS}$, in the PS mode, then the path load factor can be determined by the relation

$$H_{FxTHS} = \frac{N_{CS}}{N}\rho_{CS}(1-h)+\frac{N_{PS}}{N}\rho_{PS}, \quad (10)$$

where ρ_{CS}, ρ_{PS} and h are determined in accordance with (1), (2) and (4).

With adaptive switching that enables transmitting in the CS mode the same stream of messages and with the same qualitative characteristics as that for HS, the volume of messages sent in the PS mode can be increased by using the temporarily free channels intended for the CS mode.

In this case

$$H_{AS}=\frac{N_{CS}}{N}[\rho_{CS}(1-h)+\rho_{PS}(1-\rho_{CS}+h\rho_{CS})]+\frac{N_{PS}}{N}\rho_{PS}. \quad (11)$$

We shall determine the efficiency of AS compared to FxTHS in utilization of path capacity as before

$$\eta_{AS/FxTHS}=\frac{H_{AS}-H_{FxTHS}}{H_{FxTHS}}. \quad (12)$$

One can now write the following:

Statement 6.1.

With identical traffic and equal qualitative characteristics of sending in the CS mode, adaptive switching affords the capability of increasing path load by the value

$$\eta_{AS/FxTHS}=\frac{N_{CS}\rho_{PS}(1-\rho_{CS}+h\rho_{CS})}{N_{CS}\rho_{CS}(1-h)+N_{PS}\rho_{PS}}. \quad (13)$$

Example. Comparison of adaptive and fixed-threshold hybrid switching.

Let us assume that in the FxTHS mode, the path has been divided in two, so that $N_{CS}=N_{PS}=N/2$.

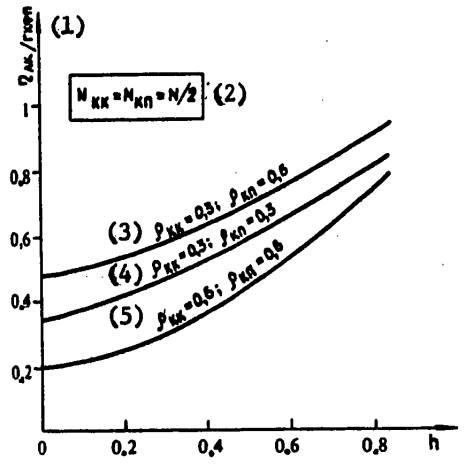

Fig. 3. Comparative evaluation of adaptive and fixed-threshold hybrid switching

Key:

1. $\eta_{AS/FxTHS}$
2. $N_{CS}=N_{PS}=N/2$
3. $\rho_{CS}=0.3$; $\rho_{PS}=0.6$
4. $\rho_{CS}=0.3$; $\rho_{PS}=0.3$
5. $\rho_{CS}=0.6$; $\rho_{PS}=0.6$

Then $$\eta_{AS/FxTHS} = \frac{\rho_{PS}(1-\rho_{CS}+h\rho_{CS})}{\rho_{CS}(1-h)+\rho_{PS}}. \quad (14)$$

The relation between $\eta_{AS/FxTHS}$ and h for certain values of ρ_{CS} and ρ_{PS} is shown in fig. 3. It can be seen from the drawing in particular that the efficiency of AS in path capacity utilization when h=0.5 in a wide range of values of ρ_{CS} and ρ_{PS} lies within the bounds of 30-60 percent compared to FxTHS. It should be noted that this gain is achieved under conditions more favorable for FxTHS, since the volume of traffic in the CS and PS modes matches the capacity allocated for these transmission modes.

6.2. Comparison of Adaptive and Floating-Threshold Hybrid Switching

When AS is used, a gain compared to floating-threshold hybrid switching [FtTHS] is achieved only by filling the pauses in the component messages. When h=0, AS and FtTHS have identical efficiency.

The path load factor with FtTHS is evaluated as follows:

$$\eta_{AS/FtTHS} \approx \frac{N_{CS}\rho_{CS}\rho_{PS}\cdot h}{N_{CS}\rho_{CS}(1-h)+N_{PS}\rho_{PS}+N_{CS}(1-\rho_{CS})\rho_{PS}} \quad (15)$$

Example. Comparing AS and FtTHS, as in the previous example, we shall assume that $N_{CS}=N_{PS}=N/2$.

Then from (15), let us derive

$$\eta_{AS/FtTHS} = \frac{\rho_{CS}h\rho_{PS}}{\rho_{CS}(1-h)+\rho_{PS}(2-\rho_{CS})}. \quad (16)$$

The value of the gain for certain values of ρ_{CS} and ρ_{PS} is shown in fig. 4. It can be seen from the graph that the gain by AS in the path capacity utilization when h=0.5 for the values of ρ_{CS} and ρ_{PS} under investigation, compared to FtTHS, ranges from about 5 to 25 percent.

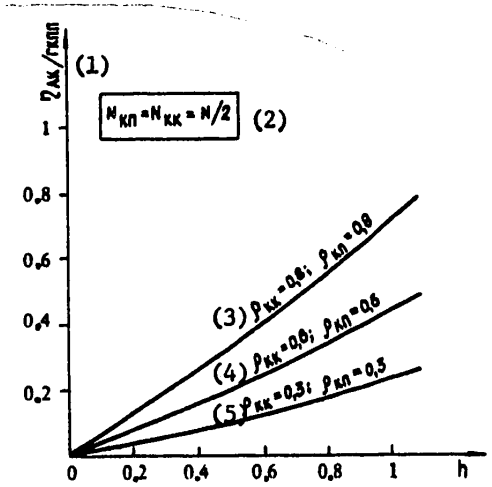

Fig. 4. Comparative evaluation of adaptive and floating-threshold hybrid switching

Key:
1. $\eta_{AS/FtTHS}$
2. $N_{PS}=N_{CS}=N/2$
3. $\rho_{CS}=0.8$; $\rho_{PS}=0.8$
4. $\rho_{CS}=0.6$; $\rho_{PS}=0.6$
5. $\rho_{CS}=0.3$; $\rho_{PS}=0.3$

Conclusion

This analysis allowed drawing the following conclusions.

1. Adaptive switching, offering universal capabilities for data transmission in the various modes (channel and packet switching, dedicated channels), can provide under real conditions better network path capacity utilization than all the switching methods discussed: channel, packet, fixed-threshold hybrid and floating-threshold hybrid switching.

2. A comparison of adaptive and channel switching shows that adaptive, providing for transmission in the CS mode of the same traffic and with the same qualitative characteristics of communication as a CS system, at the same time allows very substantial improvement in capacity utilization compared to the CS mode.

3. A comparison of adaptive and packet switching shows that with the easily met requirements with regard to AS frame length and mean packet length under otherwise equal conditions, AS affords better capacity utilization than PS.

4. A comparison of adaptive and fixed-threshold hybrid switching indicates that in sending real messages with the share of pauses on the order of 0.5, AS affords a gain of 50 percent or more in capacity utilization.

5. A comparison of adaptive and floating-threshold hybrid switching shows that under actual conditions with the share of pauses on the order of 0.5, AS affords a gain of 25 percent or more.

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DATA TELEPROCESSING STANDARDIZATION ACTIVITY BY INTERNATIONAL ORGANIZATIONS

Moscow PROBLEMY MSNTI: INFORMATSIYA, UPRAVLENIYE, SISTEMY in Russian No 2, 1981 (signed to press 28 Sep 81) pp 85-98

[Article by Stanislav Kushik, senior scientific associate, Aleksandr Sergeyevich Sorokin, candidate of engineering science and department chief, and Stanislav Nikolayevich Florentsev, candidate of engineering science, docent, chief of department of information technology and application programs, all from the International Center of Scientific and Technical Information]

[Excerpts] Described is the activity of a number of international organizations on standardization in data teleprocessing, the standards and recommendations of which have been widely propagated in the world. Brief information is given on series V, X, F, R, S and U CCITT recommendations, ISO and ECMA standards. Activity of technical committee TC97/SC16 of the ISO and other organizations on development of standards and recommendations for the seven-level model of a computer network is discussed.

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PROBLEMS IN EXPERIMENTAL RESEARCH ON INTERACTIVE INFORMATION RETRIEVAL SYSTEMS

Moscow PROBLEMY MSNTI: INFORMATSIYA, UPRAVLENIYE, SISTEMY in Russian No 2, 1981 (signed to press 28 Sep 81) pp 99-112

[Article by Vladimir Petrovich Sinyakov, senior scientific associate, International Center of Scientific and Technical Information]

[Excerpts] General characteristics are given for the problem of experimental research on interactive information retrieval systems. Discussed is the content of the main problems, for the solution of which experimental methods should be applied. Given is a classification of the main stages of the procedure of experimental research on characteristics of serving users of interactive information retrieval systems and the content of the problems occurring in each of these stages is defined. A brief description is given of the work performed by the International Center of Scientific and Technical Information within the framework of the program on experimental research in interactive information retrieval systems.

The KAMA software package is used in the USSR as a remote control system in automated systems for scientific and technical information operating in the mode of remote retrieval. Standard KAMA system facilities allow performing analysis of user activity from the viewpoint of using computer resources in an interactive system. At the end of a communication session, the system outputs data on the number of transactions performed, number of accesses to files and statistics on the execution of application and control modules. However, the standard KAMA system printout does not allow deriving data such as system response time to execution of individual instructions in the interactive system, statistics on instruction execution, volume of input and output messages, etc. [4].

Brief Description of Work Performed at the International Center of Scientific and Technical Information (MTsNTI)

A remote processing system for data bases of scientific and technical information has been developed at the MTsNTI based on the KAMA remote control system. Listed in table 2 is the composition of hardware used.

Table 2. Hardware used in remote data processing system at the Internation Center of Scientific and Technical Information

Model/Unit	Number of units in installation	Producer
YeS-1040 computer (1M byte main storage)	1	GDR
YeS-5061 magnetic disk storage unit	15	NRB
YeS-8403 MPD-3 data communication multiplexer; TAI telephone adapters	2	USSR
YeS-8002 low-speed modem (200 baud)	4	CSSR
YeS-8006 medium-speed modem (600/1200 baud)	4	VNR
YeS-8670 AP-70 subscriber station	2	USSR
YeS-8564 AP-64 cluster subscriber station (8 video terminals and a typewriter)	3	VNR
YeS-7906 local display station (4 video terminals and a typewriter)	1	USSR

[NRB = People's Republic of Bulgaria; VNR = Hungarian People's republic]

The configuration of the remote data processing system at the MTsNTI is shown in fig. 2. The software includes the OS 6.1 operating system with the basic telecommunications access method (BTMD), the KAMA remote control system and the DIALOG software package (PPP). Functional capabilities of the KAMA and DIALOG are described in [4].

The program of experimental research on interactive information retrieval systems, performed under the general scientific direction of Professor L. N. Sumarkov, doctor of engineering sciences, was begun in 1979 [30]. All experimental research is performed on the base of communication sessions with users at the Moscow Institute of Engineering Physics and the Institute of Atomic Energy imeni I. V. Kurchatov within the framework of conversations on scientific and technical cooperation. The aim of the effort is to study the typical behavior of users or the typical user during sessions of cummunication with the system, and to define for these users the characteristics required of a system when a selected number of problems are being solved.

Under this program, the following main results have been derived.

1. Probability distributions and averaged characteristics for an interactive information retrieval system were determined:

Mean system response time T_m is 7-8 seconds

Mean size of information output from system is 24,000-26,000 characters

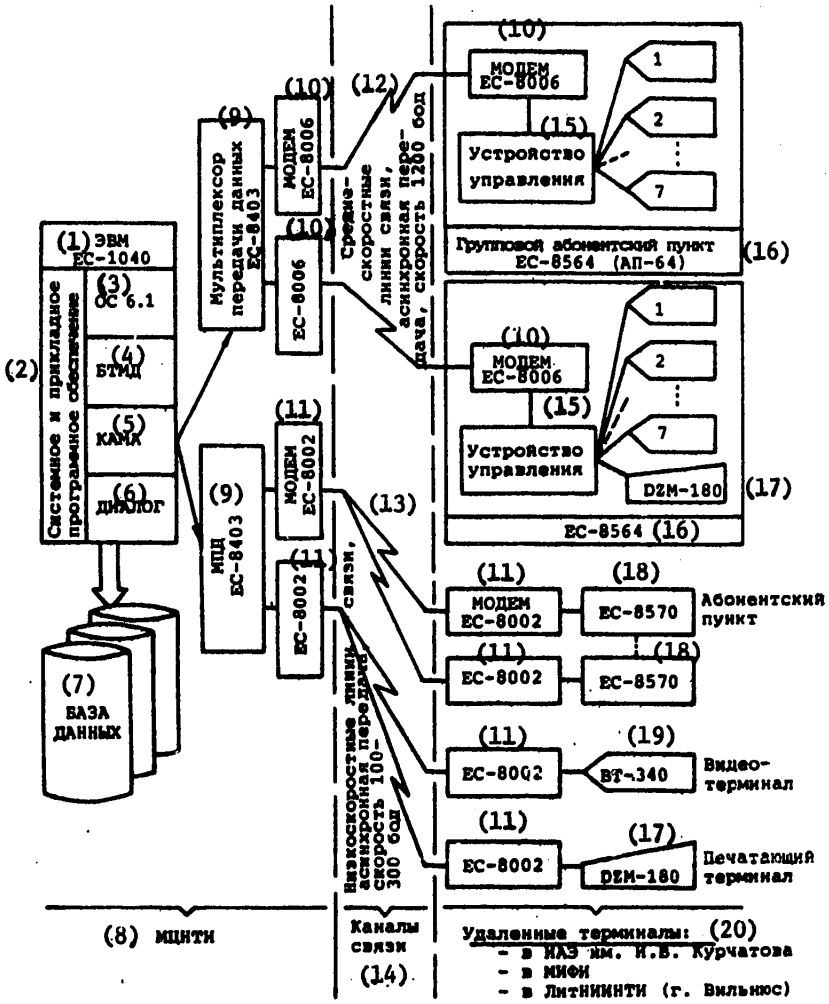

Fig. 2. Configuration of Remote Data Processing System at the International Center of Scientific and Technical Information

Key:

1. YeS-1040 computer
2. system and application software
3. OS 6.1
4. BTAM
5. KAMA
6. DIALOG
7. data base
8. MTsNTI
9. YeS-8403 data communication multiplexer
10. YeS-8006 modem
11. YeS-8002 modem
12. medium-speed communication lines, asynchronous transmission, 1200 baud
13. low-speed communication lines, asynchronous transmission, 100-300 baud
14. communication channels
15. control unit
16. YeS-8564 (AP-64) cluster subscriber station
17. DZM-180 printer terminal

[Key continued on following page]

18. YeS-8570 subscriber station
19. VT-340 video terminal
20. remote terminals at: Institute of Atomic Energy imeni I. V. Kurchatov, Moscow Institute of Engineering Physics and the Lithuanian Scientific Research Institute of Scientific and Technical Information (Vilnius)

2. Probability distributions and averaged parameters of dynamic properties of the user were determined:

Mean user response time T_m is 22-28 seconds

Average number of instructions per retrieval session is 35-40.

Average size of information input into system is 170-200 characters

3. Transition probability matrices for the set of functional user states were determined (example of matrix is shown in fig. 3).

Now being studied are correlations of the indicated parameters, basic systems engineering parameters (size of data bases, total number of active terminals, and others) and integral characteristics of interactive information retrieval sessions. The main characteristics being measured, constant and computed, are given in table 1 [not reproduced].

The system for experimental research on procedures of user interaction with an interactive information retrieval system, implemented on the base of the KAMA telemonitor and DIALOG software package, has been included in the software for the subsystem, "Remote Retrieval of Information from Data Bases of Scientific and Technical Information," of the MTsNTI and introduced in a number of other organizations.

Conclusion

For the first time in the USSR, experimental research has been performed on a practically functioning system of remote access to large data bases of scientific and technical information that is part of the information network of the USSR Academy of Sciences ("Akademset'") on the complex program "Power Engineering." Results of experiments can be used in developing standard documentation on organizing efficient interaction between users and the USSR Academy of Sciences' information network.

	A	B	C	D	E	F	G	H
A	0,3	0,4	0,1	0,06	0,04	0	0,05	0,05
B	0,2	0,6	0,1	0,1	0	0	0	0
C	0,6	0,1	0,1	0	0	0	0,1	0,1
D	0,7	0	0	0	0,1	0,2	0	0
E	0,9	0	0	0	0	0	0,1	0
F	0,2	0	0	0,3	0,1	0,3	0,1	0
G	0,3	0,2	0,1	0,05	0,03	0,02	0,15	0,15
H	0	0	0	0	0	0	0	1

Fig. 3. Transition probability matrix for functional states:

A - retrieval
B - document scan
C - document printout
D - data base selection
E - query scan
F - training mode
G - auxiliary operations
H - disconnection from system

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COMPUTER NETWORK ECONOMICS

Moscow PROBLEMY MSNTI: INFORMATSIYA, UPRAVLENIYE, SISTEMY in Russian No 2, 1981 (signed to press 28 Sep 81) pp 113-120

[Article by Yuriy Aleksandrovich Mikheyev, candidate of engineering sciences and deputy director, Pavel Ivanovich Bratukhin, doctor of engineering sciences and department chief, and Artur L'vovich Shchers, candidate of engineering sciences and department chief, all from the All-Union Scientific Research Institute of Organization and Control Problems of the USSR State Committee on Science and Technology]

[Excerpts] Discussed are the three main components of the economic effect from introducing computers into the national economy: 1) selection of an efficient organizational form for introducing computers--establishment of the State Computer Center Network (GSVTs). The main design principles for the GSVTs are given; 2) optimal selection of the structure of technical characteristics and territorial location of the GSVTs. Discussed is the structure of the complex of mathematical models for determining these characteristics of the GSVTs; 3) optimal management of GSVTs resources in solving subscriber problems. Given are the structure and main design principles for the network dispatcher service and the network distributed operating system.

Development of the ROSS [network distributed operating system] and the DSS [network dispatcher service], which perform the functions mentioned above, will allow providing for the solution to complex national economic problems and information services to network subscribers with the minimum outlays for data processing within prescribed periods and with the required quality.

Evaluating the economic effect from setting up the State Computer Center Network at present is a very complicated process. However, the experience available from setting up early computer networks (fragments of the State Computer Center Network) indicates that performing a given amount of work on a shared-use computer network required half the capital investment and one-half to two-fifths the operating cost of performing it at individual (departmental) computer centers. The payoff period for setting up a computer network in the USSR is about 3 years.

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EXHIBITS AND CONFERENCES

SYSTEMS ENGINEERING EXHIBIT TO BE HELD IN LENINGRAD

Riga AVTOMATIKA I VYCHISLITEL'NAYA TEKHNIKA in Russian No 2, Mar-Apr 82 p 94

[Article]

[Text] The next exhibition Systems Engineering-83 is planned to be held in Leningrad in April 1983 at the suggestion of the scientific and technical society. The topic is computers and systems, subsystems, mini- and microcomputers, organizational techniques, SAPR [automated design system] systems, multiplication equipment, business games, communications systems and so on. Leading foreign companies, the collective organizer of which will be the Novea Company (West Germany), will be represented at the exhibition.

To supply the exhibition with equipment meeting the interests of developing Soviet science and technology and the needs of industry, the scientific and technical center requests organizations, institutes, enterprises and specialists to present their suggestions on the composition (topic) of the exhibition, specific equipment and the manufacturing companies and also problems in this field which they would like to have discussed at the symposium. The address is: 191014 Leningrad, Kovenskiy pereulok, 12, Plant Orgtekhnika NTTs, Sistemotekhnika. The telephone number for inquiries is 272-16-01.

6521
CSO: 1863/161

QUESTIONS OF COMPUTATION OPTIMIZATION: 14TH REPUBLIC SEMINAR-SCHOOL IN KATSIVELI

Kiev KIBERNETIKA in Russian No 2, Mar-Apr 82 pp 129-130

[Report by V.S. Mikhalevich, I.V. Sergiyenko, V.V. Ivanov, M.D. Babich and V.K. Zadiraka]

[Text] One of the main avenues in the development of computer mathematics is improvements in the theory of computation errors, research on questions of comparative analysis of computing algorithms and the building of optimal (in a given sense) algorithms for problem-solving in computer and applied mathematics.

Because with each passing year there is an increase in the number of organizations using computers for complex calculations, optimization of computations by all rational methods and means is an urgent and important problem.

Taking into account the urgency of this subject, the Ukrainian SSR Academy of Sciences Institute of Cybernetics organized the 14th Republic Seminar-School "Questions of Computation Optimization" for the purpose of familiarizing a broad range of specialists with the latest achievements in the field of the optimization of computations, mathematical methods and program facilities for dialogue optimization and the more rapid introduction of research results in the national economy, and also for the purpose of coordinating research. The institute conducted the seminar-school 13 through 22 October 1981 in the settlement of Katsiveli (Krymskaya Oblast) on the base of the Ukrainian SSR Academy of Sciences House of Creativity for Scientists.

The seminar-school was oriented on the scientific staffs of computer centers, scientific research establishments and teaching VUZ's.

The main work on determining the subject matter of the seminar-school and the direction of its work was done by Academician V.M. Glushkov (deceased), Academician of the Ukrainian SSR Academy of Sciences V.S. Mikhalevich, corresponding member of the Ukrainian SSR Academy of Sciences I.V. Sergiyenko and professor V.V. Ivanov.

Representatives from 40 of the country's scientific research and training establishments participated in its work. They included Ukrainian SSR Academy of Sciences institutes of cybernetics, mathematics, applied problems in mechanics and mathematics, material science and physics, the USSR Academy of Sciences Ural Scientific Center for mathematics and mechanics, computer centers of the USSR,

Belorussian and Georgian academies of sciences, the Ukrainian SSR Gosplan, the universities of Moscow, Leningrad, Kiev, Uzhgorod, Odessa, Novosibirsk and Gorkiy, polytechnical institutes in L'vov, Kiev and Penza, teaching institutes in Irkutsk and Sumy, and others.

The number of participants totaled 130, including 1 academician of the Ukrainian SSR Academy of Sciences, 1 corresponding member of the Ukrainian SSR Academy of Sciences, 10 doctors of science and 60 candidates of science.

At the plenary session the participants of the seminar-school were welcomed by professor V.V. Ivanov, who talked about the development of the subjects of the seminar-school and its topicality having a direct relationship to improvements in quality and efficiency in solving important national economic tasks. In their speeches, senior staff member of the Ukrainian SSR Academy of Sciences Institute of Cybernetics M.D. Babich and director of the Ukrainian SSR Academy of Sciences House of Creativity, A.V. Yermoshin, spoke of the history of the seminar-schools and matters concerned with organizing and holding them, and also of the procedure for work at this seminar-school.

On the scientific plane, of the subjects presented at the seminar-school, mention should be made of those avenues concerning the theoretical and practical bases for systems optimization and methods for doing it, and computation optimization by modeling systems under development with parallel computations on a large computer complex. These avenues, formulated by academician V.M. Glushkov, are being developed at the Ukrainian SSR Academy of Sciences Institute of Cybernetics by Ukrainian SSR Academy of Sciences academician V.S. Mikhalevich, corresponding member of the Ukrainian SSR Academy of Sciences I.V. Sergiyenko, doctors of physical and mathematical sciences V.V. Ivanov, A.A. Letichevskiy, Yu.V. Kapitonova and N.Z. Shor and doctor of technical sciences V.L. Volkovich and their colleagues; and they were presented in lectures delivered by doctors of physical and mathematical sciences V.V. Ivanov, A.A. Letichevskiy and N.Z. Shor, doctor of technical sciences V.L. Volkovich, and candidates of physical and mathematical sciences P.N. Besarab, V.A. Roshchin and V.A. Trubin.

There was lively interest in the lecture titled "Main Directions in the Work of the International Institute of Systems Analysis (IIAS, Vienna)" delivered by Ukrainian SSR Academy of Sciences academician V.S. Mikhalevich who had just returned from a scientific trip to Austria. In his lecture he characterized the main scientific problems being worked on by the staff of this institute, and he also talked about the role of the Soviet Union in fulfilling its basic programs and about the participation of Soviet mathematicians in its scientific research.

Under the general title "The Variety of Optimization Problems," devoted to theoretical bases and practical recommendations in mathematical programming problems, interesting and substantial lectures were presented by professor V.A. Yemelichev, and also by his students candidates of physical and mathematical sciences V.N. Shevchenko and V.A. Pavlechko, and by scientific colleagues A.D. Korzinkov, V.P. Ovchinikov and V.V. Matveyev.

Questions concerned with the theory of chain and branch fractions and its application for solving problems in computer mathematics were dealt with in lectures and addresses

by professor V.Ya. Skorobogat'ko, readers P.I. Bodnarchuk and R.V. Slonevskiy and their students Ya.N. Glinskiy, Z.I. Krupka and Ya.N. Pelekh.

Note should be made of the lecture by doctor of physical and mathematical sciences Yu.I. Petunin "A Modified Least Square Method for Regression Models With Random Pertubations of Arguments," and of candidates of physical and mathematical sciences I.V. Beyko ("Extreme Models for Controlled Systems"), M.K. Samarin ("Direct Design Methods for Aggregates of a Simple Structure"), A.I. Grebennikov ("Optimization Problems in Approximation Theory"), A.V. Buledza ("T-Functions as Generalizations of Chebyshev Polynomials and Their Application in Iteration Process Theory"), S.N. Kiro ("Polynomials Deviating Least from Zero"),Yu.K. Dem'yanovich ("Approximation of Local Functions on an Irregular Grid"), A.Yu. Luchka ("Fast Convergence in Projection of the Noniterative Method for Hammerstein Equations"), and D.V. Gusak ("Boundary Functionals for One Class of Random Processes").

Great attention was given to lectures dealing with the development of applied program packages for solving problems in mathematical programming, function approximation and numeric integration. These were delivered by doctor of physical and mathematical sciences N.Z. Shor ("Use of the Methods of Nondifferentiated Optimization as Nuclei for Functional Models of the 'Planer' Package") and candidates of physical and mathematical sciences V.A. Roshchin ("Mathematical Models and Methods Realized in the DISPRO [expansion unknown] Applied Programs"), V.A. Pavlechko ("Realization of an Applied Program Package for Optimal Planning in an Automated Enterprise Management System"), V.I. Berdyshev ("Numeric Function Approximation") and M.V. Anolik ("A Program Package for Calculating Continual Integrals").

In addition, the subjects of the seminar-school included 17 addresses by its participants. These included reports by candidates of physical and mathematical sciences Yu.Yu. Chervak, S.S. Volokitin, I.V. Boykov, V.G. Ustyuzhaninov, A.A. Alekseyev, R.V. Polyakov, B.A. Galanov and N.Ya. Mar'yashkin, junior scientific personnel A.Yu. Yeremin and S.V. Poborchiy, and assistant lecturer R.N. Sharipov.

There was discussion of original work and results. Particularly lively discussion resulted from the lectures by doctor of physical and mathematical sciences A.A. Letichevskiy "Parallel Computations on a Macroconveyer Computer Complex" and by candidate of physical and mathematical sciences P.N. Besarab "Numeric Solutions to Regular Differential Equations in Multiple Processor Computer Systems."

The particpants of the seminar-school were given an opportunity to familiarize themselves with the latest achievements in the field of computation optimization and to get to know about a number of new theoretical problems and possible directions in their research.

Summing up the results of the seminar-school, it can be noted that it was interesting and was conducted at the necessary scientific level. The lectures presented were substantial and profound in the scientific sense. They will undoubtedly promote a widening of the front of work to develop optimal methods and the corresponding software to provide solutions for standard classes of problems in computer and applied mathematics on the computer, and an improvement in the quality and efficiency of computations in general.

Professor V.Ya. Skorobogat'ko and candidates of physical and mathematical sciences S.N. Kiro, M.D. Babich, V.K. Zadiraka, S.S. Lebedev, V.V. Lukovich and A.Yu. Luchka spoke at the final session. They noted the topicality of the subjects of the seminar-school, the high quality of most lectures and the undoubted usefulness of such measures, and they expressed a number of wishes regarding future seminar-schools and their subject matter, organization and venue.

A decision was adopted in which the following, in particular, were proposed:

to request the Ukrainian SSR Academy of Sciences to take the initiative in organizing and holding the 15th Republic Seminar-School on Questions of Computation Optimization;

to recommend that when selecting participants for the 15th and subsequent republic seminar-schools the organizing committee give preference to computer mathematicians and programmers from Vuz's, computer centers and scientific research institutes and industrial enterprises working within the framework of the given subject matter;

to attract specialists from the country's major scientific centers to lecture at the seminar-school;

to express thanks to the Ukrainian SSR Academy of Sciences Order of Lenin Institute of Cybernetics, the Ukrainian SSR Academy of Sciences House of Creativity for Scientists and the organizing committee of the seminar-school for organizing and holding it.

9642
CSO: 1863/178

PUBLICATIONS

ABSTRACTS OF ITEMS IN JOURNAL 'AUTOMATION AND COMPUTER EQUIPMENT', MARCH-APRIL 1982

Riga AVTOMATIKA I VYCHISLITEL'NAYA TEKHNIKA in Russian No 2, Mar-Apr 82 pp 95, 97, 99

UDC 681.324

FIBER-OPTIC CHANNELS OF LOCAL COMPUTER NETWORKS

[Abstract of article by Yakubaytis, E. A. and Finkel'shteyn, Ye. Ya.]

[Text] Fiber-optic data transmission channels are considered as communication devices of local computer networks. The different methods of designing the optical monochannel on the basis of optical cable segments with optical connecting elements and on the basis of long optrons are compared. The advantages and disadvantages of different versions of monochannel configuration--linear and star--are considered.

UDC 681.324

ANALYSIS OF INFORMATION TRANSMISSION IN MULTIMACHINE SYSTEMS WITH DIRECT COMMUNICATIONS

[Abstract of article by Red'ko, V. A. and Puzov, V. G.]

[Text] The process of information transmission in a four-machine computer system is analyzed by means of simulation modelling. The load of the transmission channel components, the nature of the resulting queues and the effect of the flow intensity of requirements on transmission speed are investigated. The variable parameters are the structure of the buffer memory, the number of its units and sections and the policy of designating the buffer units. The presented method permits selection of the optimum version of the structure for a specific situation.

UDC 681.322-181.48.001.2

FORMALIZED APPROACH TO OPTIMIZATION OF INTERNAL CONFIGURATION OF MICROCOMPUTERS

[Abstract of article by Lapkin, L. Ya. and Nosov, V. G.]

[Text] A formalized method is suggested for optimization of the internal configuration of a microcomputer designed on the basis of microprocessor sections.

Definitions of the internal configuration and its features are given. The problem of optimizing the internal configuration reduces to one of linear programming with boolean variables. Several postulations of the problems of optimizing the internal configuration of a microcomputer are considered. An example of the structure of a microcomputer and estimates of the features of internal configuration are presented.

UDC 681.324

FUNCTIONAL MODELS OF PROCESSES WITH REGARD TO DETECTION, BANNING AND ELIMINATION OF DEAD-END SITUATIONS

[Abstract of article by Zinov'yev, E. V. and Strekalev, A. A.]

[Text] Functional models of processes are considered under conditions of the occurrence of dead-end situations for methods of detection, banning and elimination of dead ends. The number of steps necessary to the process for completion is estimated.

UDC 519.7

SELECTION OF DIVISION IN DECOMPOSITION OF GRAPH-FLOW SHEETS OF ALGORITHMS

[Abstract of article by Baranov, S. I., Zhuravina, L. N. and Peschanskiy, V. A.]

[Text] The method of finding the division in decomposition of graph-flow sheets of algorithms (GSA) is considered that guarantees the division will be found with minimum number of units with restrictions on the parameters of each of the component GSA. The method permits one to find the component GSA of approximately identical complexity. The lower and upper bounds are introduced to estimate the number of units of division. A sequential algorithm is described for finding this division. The result of GSA decomposition by this division is close to the optimum.

UDC 519.713

LOGIC-DYNAMIC SYNTHESIS OF DIGITAL DEVICES

[Abstract of article by Levin, V. I.]

[Text] An approach is suggested for design of the block diagrams of digital automatons that guarantee two directions of the theory of automatons independently developed earlier: a) logic synthesis of the automaton circuit and b) dynamic analysis of the given automaton circuit. The design includes five steps: 1) coding of the internal states of the automaton by the version of the distinguishing code (y_1, ..., y_r) that uncouples as great a number of transition pairs as possible, 2) separation of transition pairs (if necessary) that are "impassing" uncoupled in stage 1, 3) design of the block diagram of the automaton, 4) dynamic analysis of the transitions included in the remaining uncoupled transition pairs to determine the conditions for the time parameters of the circuit that guarantee the correctness of transition and selection

of the corresponding parameters (end of procedure), if selection is impossible 5) introduction of an additional y_{r+1} digit of the internal status code and transition to step 1 with respect to the code (y_1, ..., y_r, y_{r+1}). The algorithmic structure of each step is described in detail. An example that illustrates the advantage in the complexity of realization of the automaton is given.

UDC 681.518.54

LANGUAGE FOR FORMAL DESCRIPTION OF BINARY VECTORS AND PROGRAM FOR CALCULATING THEIR SIGNATURES

[Abstract of article by Novik, G. Kh., Kramfus, I. R. and Shenderovich, S. D.]

[Text] Signature analysis is used extensively as a means of recording output binary vectors when testing logic circuits and devices. The length of the output binary vector corresponds to the dimension of the measuring window inside which specific, usually periodic distribution of components (ones and zeros) of the vector occurs. This permits one to realize sufficiently compact notation of the vector in the form of sequentially arranged groups of ones and zeros and this notation in turn permits one to introduce vectors into a digital computer by means of which the signatures are calculated theoretically. The calculating program is based on simulation of the operation of the polynomial divisor $x^{16} + x^{12} + x^9 + x^7 + 1$. The program model utilizes a block of programs written in PL/M-80 and microassembler 8080/8085 languages and the corresponding systems programs. The proposed formal entry grammar is sufficiently simple and ensures the flow of entry with arbitrary depth of embedding. The operating time of the program is on the order of a fraction of a second. The calculated signatures of binary vectors when testing logic microcircuits of different series corresponded fully to experimental signatures.

UDC 681.324:681.3.06

ONE INTERACTIVE APPROACH TO AUTOMATION OF DESIGN OF OPERATING SYSTEMS

[Abstract of article by Kalnin'sh, Ya. Ya. and Ekmanis, Ye. Ye.]

[Text] Synthesis of operating devices that realize a program given in high-level algorithmic language with time restriction of fulfilling it is described. The problem of minimizing the hardware expenditures in synthesis of these devices is considered. A method is outlined for automated design of operating devices in which the use of formal methods of parallelling the performance of program and minimization operations of hardware expenditures can be combined with the use of designer experience.

UDC 681.35

ESTIMATING THE DISTRIBUTION PARAMETERS OF THE CHARACTERISTICS OF COMPUTER SYSTEMS

[Abstract of article by Chuyko, M. M.]

[Text] A method is proposed for determining the estimates of the distribution parameters of the characteristics of computer systems found as a result of measurements. The experiments show that these distributions are multimodal with regard to which it is suggested that they be regarded as mixtures of single-modal distributions of the given type. The problem of determining the distribution parameters reduces to one of dividing the distribution mixtures by the components. It is suggested that random search for the global maximum of the similarity function in the presence of restrictions on the optimization parameters be used to solve it. A number of advantages of realizing this algorithm is noted compared to realization of the previously known algorithm of dividing the sample by subpopulations. It is recommended that the algorithm be used in the case of weakly separated mixtures of distributions.

UDC 681.324

MODELS OF CONFLICTS IN MEMORY OF MULTIPROCESSOR SYSTEMS

[Abstract of article by Kagan, B. M. and Kreynin, A. Ya.]

[Text] Analytical probability models are proposed for estimating the productivity of multiprocessor systems with general and local memory. The models are based on exponential stochastic mass queueing networks.

UDC 681.51:519.872

METHOD OF INVESTIGATING THE FUNCTIONING OF FRAGMENTS OF COMPUTER SYSTEMS WITH VARIABLE MODE

[Abstract of article by Sklyarevich, F. A.]

[Text] The fragment of a computer system with variable functional mode is considered. The process of changing the modes is an inhomogeneous marker process. A transient system of first-order linear differential equations that determines the laws of variation of the functional indicators corresponds to each mode. It is proved without using Focker-Planck-Kolmogorov equations that their unconditional mean values are determined by a system of linear differential equations easily found by transforming the equations of the behavior of the fragment with each of the modes separately under conditions of fitting the functional indicators when their modes change. The method is applicable for determining the mean value and second initial moment of the number of occupied processors in a multiprocessor system with variable mode.

UDC 519.718

DESIGN OF VERIFICATION TESTS FOR PROGRAMMABLE LOGIC MATRICES

[Abstract of article by Zakrevskiy, A. D.]

[Text] The problem of detection in programmable logic matrices of multiple malfunctions formed by arbitrary combinations of single malfunctions of the type of appearance or disappearance of transistors in the components of the matrix field of the circuit is considered. It is shown that the problem of designing effective verification tests for programmable logic matrices is closely related to that of optimum realization of a given system of boolean functions on a programmable logic matrix. An approach is suggested for solving it that is made more specific for the case of a single boolean function in the system. The problem reduces to finding a weakly determined boolean function having single realization among disjunctive normal form with given number of elementary conjunctions.

UDC 621.372.542

ANALYSIS OF VINOGRAD METHOD FOR CALCULATION OF DISCRETE FOURIER TRANSFORM OF 2^n-POINT SEQUENCES

[Abstract of article by Mayorov, S. A., Matveye, Yu. N. and Ochin, Ye. F.]

[Text] The possibility of direct use of the Vinograd algorithm to calculate a 2^n-point discrete Fourier transform and also the possibility of using small-point Vinograd algorithms in a 2^n-point fast Fourier transform are considered. The computer memory expenditures and number of operations in realization of Vinograd algorithms are estimated.

UDC 621.391.244

APPLICATION OF RECTANGULAR PERIODIC FUNCTIONS TO CALCULATION OF DISCRETE FOURIER TRANSFORM

[Abstract of article by Bilinskiy, I. Ya., Borovik, Yu. F. and Mikelson, A. K.]

[Text] A method is proposed for fulfilling a Fourier transform that utilizes an intermediate procedure of signal expansion in a system of rectangular periodic filter functions that assume only values of 0, 1 and -1, which can also be nonorthogonal. The requirements on the filter function system are determined. It is shown that the procedure of determining the Fourier coefficients according to the proposed method consists of two steps. The intermediate coefficients corresponding to the procedure of signal expansion in a system of rectangular periodic functions are determined in the first step. This step does not contain multiplication operations. The desired values of the Fourier coefficients as solutions of a system of linear equations are calculated in the second step. The number of multiplication operations in the second step depends on the type of filter functions. Examples of possible systems of filter functions are presented. The use of a given method in fulfilling a discrete

Fourier transform permits a considerable reduction of the number of multiplication operations compared to the algorithm of a fast Fourier transform. The method can be recommended for design of special processors of discrete Fourier transform operating in real time.

UDC 519.711.7

ROUTING ALGORITHMS FOR MESSAGE-SWITCHING NETWORKS

[Abstract of article by Apraksin, Yu. K., Zapevalin, A. A. and Kiryukhin, V. V.]

[Text] A procedure for selecting the direction of information transmission in message-switching networks is investigated. A number of routing algorithms that utilize information only about the status of channels incident to a given assembly is considered. A unified structure for describing the algorithms is proposed. The effectiveness of the algorithms is estimated on the basis of the adopted model of the network from the viewpoint of the main criterion--the average time of delivery of the message to the addressee.

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TABLE OF CONTENTS FROM JOURNAL 'CYBERNETICS', MARCH-APRIL 1982

Kiev KIBERNETIKA in Russian No 2, Mar-Apr 82 p 133

[Text] Contents

REPORTS IN BRIEF

9642
CSO: 1863/178

UDC 681.142.2

ANALYTICAL METHODS FOR MULTIPROGRAM SYSTEMS

Moscow METODY ANALIZA MUL'TIPROGRAMMNYKH SISTEM in Russian 1982 (signed to press 29 Dec 81) pp 2-3, 153

[Annotation, editor's foreword and table of contents from book "Analytical Methods for Multiprogram Systems", by Valeriy Alekseyevich Balyberdin, edited by S. D. Pashkeyev, Izdatel'stvo "Radio i svyaz'", 8,000 copies, 153 pages]

[Text] Methods are shown for quantitative analysis of data processing systems built on the basis of multiprogrammed computers. The main problems arising in the development and function of such systems are discussed and ways of solving them are indicated. The computation methods considered make it possible to take into account the complex processes involved in problem interaction at the level of exchange and computation overlap. Much attention is given to questions of the practical application of these methods.

The book is intended for engineers associated with the design and organization of function in data processing systems based on multiprogrammed program computers; it may be of use to students on advanced courses.

Editor's Foreword

Questions of improving the efficiency of computer equipment have always attracted the attention of data processing system developers and users. One promising way in this direction is the use of multiprogramming as a method for simultaneously solving several problems on the same computer.

It came about historically that the first period in research in the field of multiprogramming on a single computer coincided with the appearance of multiprocessor and multimachine computing systems. This stimulated development of work in the field of parallel algorithms and computing structures, on which the main scientific effort was focused. Later, however, developments in practical data processing showed that in many cases the most expedient and economically justified way of increasing a system's productivity is multiprogramming. This is especially true for specialized systems in which constraints on physical parameters partially exclude the possibility of substantial increases in system productivity through augmenting the computer resources.

In recent years there has been a marked increase in the interest in the problems of multiprogramming, especially with regard to methods for formal description and

quantitative analysis of multiprogram systems, not only in our country but also abroad. The concrete proof of this is the publication in foreign sources of a number of materials on this subject written by Soviet authors, including the author of this book. However, available work is largely disjointed and reflects isolated, partial aspects of multiprogramming. It would seem that there is a need for a generalized presentation of questions concerned with quantitative evaluation and optimization of the computing process in multiprogram systems, within the framework of a unified approach. V.A. Balybedrin's book "Analytical Methods for Multiprogram Systems" is the first of attempts of this kind. It has been written on the basis of many years in research and practical experience by the author in the field of developing data processing systems on the basis of multiprogrammed computers. In it, material is generalized from a great amount of work on this subject done in recent years. The book reflects the present status of and immediate prospects for the development of methods for quantitative analysis of multiprogram systems and will undoubtedly fill a gap in the literature on data processing systems based on multiprogrammed computers.

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CSO: 1863/175

JOURNAL 'INSTRUMENTS, MEANS OF AUTOMATION AND CONTROL SYSTEMS TS-2: COMPUTER HARDWARE AND OFFICE EQUIPMENT', JULY-AUGUST 1981

Moscow PRIBORY, SREDSTVA AVTOMATIZATSII I SISTEMY UPRAVLENIYA, TS-2: SREDSTVA VYCHISLITEL'NOY TEKHNIKI I ORGTEKHNIKI (BIBLIOGRAFICHESKAYA INFORMATSIYA) in Russian No 4, Jul-Aug 81 pp 1-16

[Text] A. COMPUTER TECHNOLOGY

A1. General Questions of Computer Technology

681.322

360. "Computer task execution analysis." Kostyuk, I. T. and Makarenko, V. N. In book: "Problemy razrabotki matematicheskogo obespecheniya mezhotraslevykh ASU" [Problems of the Development of Interbranch ASU Software]. Collection of Scientific Works. UkrSSR Gosplan. Main Scientific Research and Information-Computer Center, Kiev, pp 123-128. [Input from GPNTB].

681.3.003.13

361. "On the question of the effectiveness of computer use." Karapetyan, V. V. VOPROSY RADIOELEKTRONIKI. SERIYA EVT:NAUCHNO-TEKHNICHESKIY SBORNIK, 1980, No 15, pp 8-13.

681.323

362. "Criterion for estimating effectiveness of specialized computer hardware." Agzamov, Sh. Sh. In book: "Avtomatizatsiya proizvodstvennykh protsessov" [Automation of Production Processes]. Tashkent, 1980, pp 38-45. (Trudy/Tashkent Polytechnic Institute, No 308). [Input from GPNTB].

681.3.01

363. "On some distinctive features of the electromagnetic compatibility of computers." Karapatyan, V. V. VOPROSY RADIOELEKTRONIKI. SERIYA EVT:NAUCHNO-TEKHNICHESKIY SBORNIK, 1980, No 15, pp3-7.

See also No 407.

A2. Theoretical Questions

681.325.66

364. "Automation of construction of models of functioning of elements of digital circuits." Tatulyan, S. A. and Oganesyan, G. G. VOPROSY RADIOELEKTRONIKI. SERIYA EVT:NAUCHNO-TEKHNICHESKIY SBORNIK, 1980, No 15, pp 91-94.

681.3.01

365.. "Analysis of methods of organizing a computer synchronization system." Seropyan, S. S. VOPROSY RADIOELEKTRONIKI. SERIYA EVT:NAUCHNO-TEKHNICHESKIY SBORNIK, 1980, No 15, pp 33-41. Bibliography, p 41: 10 items.

681.3.01:621.398

366. "Analysis of buffering processes in remote processing systems." Broytman, M. D. and Ettinger, B. Ya. AVTOMATIKA I VYCHISLITEL'NAYA TEKHNIKA, 1981, No 2, pp 55-61. Institute of Electronics and Computer Technology, Latvian SSR Academy of Sciences. Bibliography, p 61: 10 items.

[681.326.3:[53.072:681.3]

367."Method of combining the modeling levels during investigation of the functioning and development of computer systems." Dudkin, A. M., Zinkin, S. A. and Kulagin, V. P. VOPROSY RADIOELEKTRONIKI. SERIYA EVT:NAUCHNO-TEKHNICHESKIY SBORNIK, 1980, No 10, pp 85-89, ill.

681.3.06

368. "Minimization of systems of canonical equations representing a digital automaton with consideration of the signal distribution." Vashkevich, N. P. VOPROSY RADIOELEKTRONIKI. SERIYA EVT:NAUCHNO-TEKHNICHESKIY SBORNIK, 1980, No 10, pp 90-96. Bibliography, p 96: 3 items.

621.391.833

369. "Determination of the probabilities of distortions of the positions of pulses of reproduction." Knyazev, G. I., Mikhaylov, V. I. and Rakov, B. M. VOPROSY RADIOELEKTRONIKI. SERIYA EVT:NAUCHNO-TEKHNICHESKIY SBORNIK, 1980, No 10, pp 9-14. Bibliography, p 14: 4 items. Calculations of the probabilities and distributions of positions of pulses and the amounts of distortions during reproduction of information from a magnetic carrier is determined from the graph of superpositions, which represents a mathematical model.

007.52

370. "Optimization of disjunctive decomposition during synthesis of an automaton on PLM [not further identified]." Plotnikov, A. V., Salomatin, V. A. and Barkalov, A. A. VOPROSY RADIOELEKTRONIKI. SERIYA EVT:NAUCHNO-TEKHNICHESKIY SBORNIK, 1980, No 10, pp 80-84, ill. Bibliography, pp 83-84: 5 items.

681.326:32

371. "System of documented representation and coding of a diagram of micro-program logic." Vashkevich, N. P., Dudkin, A. M., Zinkin, S. A. et al. VOPROSY RADIOELEKTRONIKI. SERIYA EVT:NAUCHNO-TEKHNICHESKIY SBORNIK, 1980, No 10, pp 75-79, ill.

See also 363, 435 and 437.

A3. Reliability of Computers

681.3-192

372. "Questions of increase of computer reliability in commutation working regimes. VIP [not further identified]." Muradkhanyan, E. A. VOPROSY RADIOELEKTRONIKI. SERIYA EVT:NAUCHNO-TEKHNICHESKIY SBORNIK, 1980, No 15, pp 55-61.

681.3-192

373. "Integrated device for diagnosis of YeS computer cards." Mkrtumyan, I. B. and Karokhanyan, M. O. VOPROSY RADIOELEKTRONIKI. SERIYA EVT:NAUCHNO-TEKHNICHESKIY SBORNIK, 1980, No 15, pp 50-54.

681.326.75:681.327.6

374. "Organization of monitoring information with the use of an error detection code." Tsapulin, V. K. and Goryachev, V. A. VOPROSY RADIOELEKTRONIKI, SERIYA EVT:NAUCHNO-TEKHNICHESKIY SBORNIK, 1980, No 10, pp 127-130, ill. The authors examine questions regarding realization on Series 155 micro-circuits of a device for monitoring information on magnetic carriers by means of an error detection code.

681.3-192

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620.1.05:681.3

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681.3.06-181.48

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681.3.015:681.326.74.06

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681.32.06

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621.316.729:681.327.13

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681.3.01:658.012.011.56

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681.325.5-181.4

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681.3.06:658.012.011.58

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681.3.06-181.48

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681.32.06-52:519.5

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621.316.729:681.327.13

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681.3.06-181.48

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621.327.28:681.3-181.48

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621.377:623.223.4:54.06

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681.3-192

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681.3.06

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681.327.28-529:621.3.049.77

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621.3.049.771.14

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681.327.67:621.3.049.77

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A.8. Computers

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681.3.02

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681.327.2

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681.3.01:621.316.56

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681.3.01:621.316.56

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681.327.2

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681.327.2:681.3-181.4

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681.326.3

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681.3-181.48

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681.326.34

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A.8.5. Stores

53.072:681.31

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681.327

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621.312.799

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621.327.632

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681.327.6.071.3

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681.327.68

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681.327.67

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681.3.067

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681.327.6.071.3:621.317.443

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681.327.67

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681.327.2-185.4

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681.326.3

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681.327.2-185.4

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681.327:634

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621.327.6.071.3:621.317.4

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681.327:.621.3.049.77

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681.3.04:681.327.11

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681.327,2-185.4:621.3.049.774.3

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681.327.68

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681.327.6.071.1/2

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681.327.67

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681.3.067

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681.327.2-185.4

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See also No 369, 374, 382, 390, 393, 400, 401

A.8.7. Other Computer Units and Elements

681.3.067

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68.332.35

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A. 9. Application of Computers

621.9.06-529

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621.9.06-529

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681.3.001.24

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002.53:681.518

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681.26:681.2/.3

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681.3.001.57

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681.3:621.372.54

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JOURNAL 'INSTRUMENTS, MEANS OF AUTOMATION AND CONTROL SYSTEMS TS-2: COMPUTER HARDWARE AND OFFICE EQUIPMENT', NOVEMBER-DECEMBER 1981

Moscow PRIBORY, SREDSTVA AVTOMATIZATSII I SISTEMY UPRAVLENIYA, TS-2: SREDSTVA VYCHISLITEL'NOY TEKHNIKI I ORGTEKHNIKI (BIBLIOGRAFICHESKAYA INFORMATSIYA) in Russian No 6, Nov-Dec 81 pp 1-24

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UDC 621.311.1.064

POWER SYSTEM AUTOMATIC EQUIPMENT SEMICONDUCTOR ELEMENTS

Moscow POLUPROVODNIKOVYYE ELEMENTY AVTOMATICHESKIKH USTROYSTV ENERGOSISTEM in Russian 1981 (signed to press 18 Apr 81) pp 2-4, 6-7, 405-407

[Annotation, excerpts from foreword and introduction, and table of contents from book "Power System Automatic Equipment Semiconductor Elements", by Nikolay Il'ich Ovcharenko, Energoizdat, 12,000 copies, 408 pages]

[Excerpts] In this book the operating principles are discussed, as well as methods of technical implementation of analog and some digital semiconductor functional elements of the measuring portion of relay protection, automatic emergency warning, automatic regulation and remote control equipment.

Elements are classified on the basis of operations on signals performed in automatic equipment in the process of obtaining, transferring, processing, using and representing data.

This book is intended for engineers involved in designing and servicing automatic equipment and automatic control systems and can be of interest to graduate students and students specializing in electric power.

Functional elements of the measuring portion of electric power system automatic control and protection equipment and their characteristics are discussed in this book. The results are presented of a number of studies relating to the development of functional elements and continuously operating and relay-controlled measuring elements carried out at MEI's [Moscow Power Engineering Institute] department of automation and relay protection by the author or together with V.G. Doroguntsev, V.V. Budkin, E.I. Bass, R.V. Temkina and graduate students Yu.A. Len'kov, A.M. Chukhin et al. The author is grateful to these comrades for their scientific cooperation and the possibility presented of publishing individual data.

The author wishes to express his gratitude also to the reviewer, Doctor of Technical Sciences Professor V.L. Benin, for his valuable comments on the manuscript, which have helped to improve it.

The author will be very grateful to readers who forward their comments on this book and requests that they be sent to the address of Energoizdat: 11314, Moscow, M-114, Shlyuzovaya nab., 10.

The measuring section has certain features occasioned by the specific nature of the process of producing and distributing electric power, in particular, by the danger of catastrophic consequences of tardy and faulty operation of automatic equipment. Therefore, the measuring section must be characterized by high technical perfection.

The measuring section should, as a rule, be practically inertialess. The time of its operation should not exceed the duration of a single mains frequency cycle. Therefore, opportunities for "storing" information in the formation of signals by statistical processing of many realizations of a random process requiring time are excluded. The measuring section of the automatic equipment for controlling the process of producing and distributing electric power must generate the proper signal in practically a single realization of the random process carrying the information, which requires use of the appropriate operating principles and makes the technical implementation of this section exceptionally difficult.

Requirements for the measuring section of automatic equipment have become ever stricter as electric power engineering has developed and the USSR Unified Energy System (YeES SSSR) has been created. Therefore, the measuring section of automatic equipment for controlling the process of producing and distributing electric power should be implemented on the basis of the latest scientific and engineering achievements of information technology.

Under conditions of modern scientific and technical progress hardware for the implementation of automatic control equipment is being developed and improved extremely rapidly. The development of semiconductor hardware is the principal trend. Integrated semiconductor functional elements represent today's level of the development of information hardware.

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