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USSR Report

CYBERNETICS, COMPUTERS AND AUTOMATION TECHNOLOGY

(FOUO 11/81)

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CONTENTS

SM COMPUTERS

SMALL COMPUTERS AND THEIR APPLICATION

Moscow MALIYE EVM I IKH PRIMENENIYE in Russian 1980 (signed to press 14 Aug 80) pp 2-49, 89-94, 147, 172-183, 190-195, 210, 212-213, 230 - 231

[Annotation, table of contents, introduction and excerpts from book "Small Computers and Their Application," edited by B. N. Naumov, Izdatel'stvo "Statistika", 34,000 copies, 232 pages]

[Text] The SM-3 and SM-4 control computer complexes (UVK) developed within the family of small computers (SM EVM) are considered. The configuration characteristics of UVK, the input-output systems interface, the hardware of SM EVM for development of complexes and the software are described. Examples of configuration of problem-oriented complexes are presented.

The book is intended for specialists in the field of computer technology and automated control systems.

Contents

Introduction

Development and serial output of a new family of productive and economical small computers (SM EVM) open wide opportunities for introduction of automatic information processing and control systems in new and traditional fields of application of computer equipment. Solution of problems of qualitative improvement of the structure of computer complexes, development of the component and design-production base ensured large-series production of SM EVM. Oriented toward a wide range of applications (complex automation of production processes, automation of monitoring and measurements, automation of scientific research, automation of teaching, message switching, automation of scientific and engineering calculations and processing economic and statistical information), SM EVM become accessible to a large number of users.

At the present time the SM EVM includes SM-1P, SM-2P, SM-3P and SM-4P basic processors with productivity from 200,000 (SM-1 and SM-3) to 400,000 (SM-2) and 800,000 operations per second (SM-4). SM-1P and SM-2P processors continue the line of domestic M-6000 and M-7000 computers. Therefore, the SM-1 and SM-2 computers are oriented primarily toward application in those systems where there is already sufficient completion of the software for the M-6000 and M-7000 computers.

The SM-3 and SM-4 computers, continuing the line of domestic M-400 computers, include a large number of essentially new structural solutions directed toward simplification of programming, design of various computer, control, information and measuring complexes and arranged in an optimum manner to work under specific conditions.

The main features of the SM-3 and SM-4 are a wide range of productivity under specific conditions of application, major structure of the interface with apparatus realization of most input-output information systems functions, simple realization of multiprocessor and multimachine systems, high speed of processing interrupt and capability with formats of different length.

The nomenclature of devices (input-output, communicating with objects, external magnetic carrier memory and so on), traditional for small control computer complexes, is supplemented by devices for expansion of the intermachine and interprocessor communications complexes. Because of this, realization of computer systems with common and separate field of peripherals and complexes with variable structure is provided. The software of the SM-3 and SM-4 is constructed on the basis of multiuser real-time systems, time sharing, remote processing, dialogue systems and so on, with a large number of procedure-oriented routines.

The book offered to the reader is the first in a series of books devoted to SM EVM. The main characteristics of SM EVM (SM-3 and SM-4) are considered in it. The book provides specialists in the field of computer technology and automated control systems the main reference data which permit one to select the appropriate computer and to evaluate the capabilities of the hardware and software of the SM-3 and SM-4 and also examples of configuration of SM-3 and SM-4 complexes.

The following books will be devoted to detailed consideration of programming problems on the SM-3 and SM-4 computers, description of hardware and analysis of the principles of configuration of complexes of different designation, problems of joint operation of SM EVM with other families of computers and design of automated control and information processing systems based on the SM-3 and SM-4 UVK.

The wishes and comments of the Institute of Cybernetics of the Ukrainian SSR Academy of Sciences, the Central Economic and Mathematics Institute of the USSR Academy of Sciences and a number of plant organizations were taken into account during preparation of the book.

The comments of the book reviewer, doctor of technical sciences, Professor A. G. Shigin were especially useful.

Chapter 1.

SYSTEMS ENGINEERING CHARACTERISTICS AND CONFIGURATION OF SM-3 AND SM-4 CONTROL COMPUTER COMPLEXES

1.1. Systems Engineering Characteristics of SM-3 and SM-4

[Text] Systems engineering characteristics are determined by parameters of both individual devices and modules of the SM-3 and SM-4 and by generalized indicators of productivity, efficiency and structural characteristics of the SM-3 and SM-4 complexes. These characteristics permit one to refine the field of effective application of the SM-3 and SM-4 and to provide a general idea of the capabilities of designing systems based on the SM-3 and SM-4. The nomenclature of the SM-3 and SM-4 hardware is constructed on the basis of 16-digit processors (SM-3P and SM-4P) and includes internal storage modules and a set of external devices and interprocessor and intermachine communications devices.

The systems characteristics (speed of information input-output, processing speed, functional capabilities, set of external devices, operating efficiency of multiprocessor complexes and so on) of the SM-3 are 2 to 10 times greater than the corresponding characteristics of microprocessor computers (for example, the Elektronika-60). The use of new structural and design-engineering solutions in the SM-4 computer made it possible to increase approximately fourfold the productivity of this processor compared to the SM-3 and to bring it up to a level close to the productivity of medium-sized computers (for example, the YeS-1033). The instruction set of the SM-3 computer is the instruction subset of the SM-4 computer and therefore all the routines written for the SM-3 can be processed on the SM-4 without any change. Most operating systems are common to the SM-3 and SM-4.

One of the most important problems of wide application of modern computers is reduction of expenditures for programming and primarily for the more laborious systems programming, which requires highly qualified programmers. The new structural solutions used in the SM-3 and SM-4 provide apparatus realization of a large number of systems functions in the following typical modes:

real time (system of priorities of requests for interrupt, processing of interrupts, register and cartridge (stack) memory, information storage system and problem restart system with brief cutoff of power and hardware-software monitoring);

time-sharing (means of security and dynamic redistribution of memory, hardware-software for dynamic change of priorities);

solution of information retrieval problems, construction and management of data bases: different format information processing (byte, bit, word and double

word) with floating and fixed decimal, processing and transmission of information files, an effective instruction set which provides simple realization of different data structures (lists, tables and files).

Apparatus execution of complex systems functions in a processor occurs on the average an order faster than execution of routine modules with similar systems characteristics. This in turn significantly expands the boundaries of application of the SM-3 and SM-4.

Structurally, these complexes can be made in the form of a set of several modules (processor, memory, object communications device--USO) built into the control object. Single-column versions of configuration may also include magnetic disc stores, punch tape input-output modules or internal storage expansion blocks. Two-column and multicolumn versions of configuration, depending on designation, may include USO expansion modules (from several hundreds to several thousand input and output signals, with given metrological and dynamic characteristics), magnetic carrier nonvolatile memory expansion modules, modules for design of two-processor systems (hierarchical, distributed, with variable structure, with separate and common field and so on). The capabilities of using the SM-3 and SM-4 are expanded due to the devices for communicating with other computer families. The capability of connecting microprocessor computers to the SM-3 and SM-4 provides design of distributed information, control and measuring systems in which the SM-3 and SM-4 perform the functions of a central computer.

During joint operation with the YeS EVM [Unified computer system], the SM-3 and SM-4 UVK are used as

a remote intellectual terminal;

an input-output processor which provides communications with the object in real time with high dynamic characteristics;

a message concentrator in network structures;

a peripheral processor.

An important design feature of the SM-3 and SM-4 is execution of individual modules in the form of self-contained structural blocks with their own power supply sources and so on. They are connected to the complex by the standard method using cables. This permits the user to configure SM-3 and SM-4 complexes with regard to specific conditions and to carry out simple pre-assmebly of systems during operation to provide new functional capabilities.

The external devices of the SM EVM can be connected both to the SM-3 and SM-4 by the same integration modules (controllers and interface blocks).

Let us consider the characteristics of the main devices which can operate in SM-3 and SM-4 complexes.

The external storage devices include:

cassette-type magnetic disc stores with capacity of 4.8 Mbytes (the interchangeable carrier is a single-disc cassette with capacity of 2.4 Mbytes). Up to four storage devices (with total capacity of 80-160 Mbytes) can be connected to the dispatcher. These storage devices are used to design expanded-volume information files;

floppy magnetic disc storage device with capacity of 1.5 Mbytes. It is used in systems if smaller dynamic characteristics of space are permissible (approximately an order lower than for cassette type storage devices). A decrease of the reqirements on storage conditions of the carrier expands the capabilities of using the SM-3 and SM-4 under more complex operating conditions of the complexes;

cassette-type magnetic tape store with capacity of 0.7 Mbytes. It is used if storage devices of minimum dimensions are required.

Combination punch tape input-output devices provide entry of information with maximum speed of 500-1,000 lines/second (maximum perforation speed of 50 lines/second).

Printers include sequential and parallel type alphanumeric printers with speed of 100-180 characters/second and 90-1,200 lines/second, respectively (which corresponds to 9,000 characters/second).

Alphanumeric displays with capacity of 2,000 characters per frame are systems console devices. They can be used as operator terminals in ASU [Automated control system] of various types.

Inclusion of a graphical display (EPG SM) in the nomenclature of SM EVM expands the capabilities of working with graphical information in dialogue modes.

An important feature of the SM-3 and SM-4 is the developed nomenclature of USO different in characteristics. SM-3 and SM-4 complexes can use five types of USO which provide different sets of input (output) signals with given characteristics corresponding to the reuqirements of various systems: ASU TP [Automated Control System for Production Processes], monitoring and measuring systems and scientific research automation systems:

USO with "Common bus" interface. This class includes a modular USO which provides input-output of analog (UVA) and digital (UVD) signals, including initiative signals. Self-contained complete blocks (64-256 signals) or USO racks (256-1,024 signals) can be configured as a function of the required signal composition. The maximum separation of the analog signal input sensors is up to 600 meters from the UVK.

Moreover, a complex multifunctional USO--a high-speed input-output device (48 digital signal input channels and 48 digital signal output channels and 24 analog signal input channels and 2 analog signal output channels in a single self-contained complete block) can be used;

USO with interface of 2K from the nomenclature of M-6000, M-7000, SM-1 and SM-2 computers (expanded set of modules, capability of separation by 1-2 km and so on). OSh/2K integration-matching devices (USS OSh/2K) which realize two direct access channels and two routine channels (using expanders to the SM-3 and SM-4 so

that up to 120 interface cards of 2K capacity can be connected) are used to connect these devices to the SM-3 and SM-4;

modules of the international Camac standards system (they are connected to the SM-3 and SM-4 by means of the Camac controller). The modular nature of this type of USO increases its effective use in the systems with frequently rearranged structure (automation of scientific research, monitoring and measuring, finishing experimental processes and so on).

modules from the nomenclature of unit means of electronic measuring equipment (ASET) which are connected through the ASET controller. Because of the increased metrological support, these devices are oriented toward use in monitoring and measuring complexes and in some systems for uatomation of scientific research;

single-card USO modules from the nomenclature of SM-1800 microcomputers. The SM-1800 microcomputer with USO modules (and with all its own peripherals) is connected to the SM-3 and SM-4 by means of the SM-1800 OSh/bus interface card. Because of this, the UVK can operate with USO of new classes by intellectual and distributed USO.* The integrated characteristic which determines the effectiveness of using computers under specific conditions is the computer productivity when processing specific requests in given functioning modes.

Indicators of productivity depend on a large number of factors: the rate that elementary operations are performed, the rate of information exchange, the structure of the central part, configuration of the computer complex, characteristics of peripherals, structure and adjustments of the operating system, systems of the priorities of characteristics of the algorithms being solved, selected service disciplines and so on.

The time required to complete standard instructions and operations which can serve as input data for calculation of the productivity of SM-4 (SM-3) complexes is as follows:

Type of Instruction or Operation	Time of Completion, μs	
	SM-4	SM-3
Switching	1.2	4
"Register-register" format	1.2	5
"Register-memory" format	3.3	7
"Memory-memory" format	4.7	10
Multiplication (with fixed decimal)	10.8	16*
Division (with fixed decimal)	12.7	19.5*
Addition (with floating decimal)	28.7	320
Multiplication (with floating decimal)	34.0	410
Cycle during word reading operations with regeneration, word recording and byte recording	1.2	1.2
*with arithmetic expander		

[Table continued on following page]

*The characteristics of the devices of SM EVM are considered in more detail in Chapter 5.

[Table continued from preceding page]

Type of Instruction or Operation	Time of Completion, μs	
	SM-4	SM-3
Cycle during word reading operations without regeneration	0.7	0.7
Access time	0.5	0.5
Response to external interrupt through direct access channel	6	6
Response to interrupt through routine channel (without regard to time of completing instruction)	10	10

The speed of SM-4P (SM-3P) processors achieved on examples of information processing by averaged sets of operations is 130,000 (60,000) for scientific and technical tasks, 130,000 (30,000) for economic information processing tasks and 320,000 (150,000) instructions per second for operational control tasks.

The degree of conformity of SM-3 and SM-4 structure to the complex and contradictory requirement of real-time information processing may be indicated by the fact that the speed of SM-3P and SM-4P processors in the operational control modes is essentially at the level of completing elementary instructions of the "register-memory" format. Some problems of estimating the productivity of SM-3 and SM-4 with regard to the operating characteristics in multitask modes are considered in [10].

The intrasystems interface of the SM-3 and SM-4 is realized in the form of a unified "Common bus" (OSh)* main channel.

In this case all devices, including the internal storage, are connected to the OSh. A large number of important systems functions (on realization of the priority system, multilevel interrupt system, high reactivity, information exchange and so on) is realized by apparatus in the OSh interface. Let us consider a number of the main systems engineering characteristics of the OSh interface.

Depending on the capabilities contained in the dispatchers (control devices), the OSh interface can provide the following information exchange modes:

direct access--extraprocessor exchange realized at a speed of 700 kwords/second (comparable to the memory cycle). High-speed devices (magnetic disk and magnetic tape stores, object communications devices, machine communications adapters and so on) operate in this mode. Information files can be recorded on magnetic carriers in SM-3 and SM-4 using this channel without loading the processor;

the routine channel of information file exchange realized with loading of the processor at speeds of 30 kwords/second (for the SM-3) and 300 kwords/second (for the SM-4). It is used for medium productivity devices with simpler control devices;

routine channel with interrupt of the background routine with entry of each word (or byte), which provides an exchange rate of 16 kwords/second (for the SM-3)

*The OSh interface is considered in more detail in Chapter 2.

and 33 kwords/second (for the SM-4). It is used for low-speed devices (for example, input devices with perforation carrier).

An important systems characteristic of the OSh interface is the asynchronous principle of communications which provides effective operation in a single complex of devices with different level of productivity and simple replacement of modules of the same type by more productive modules.

A significant increase of the affected speed of information processing in real-time modes can be achieved in the SM-3 and SM-4 due to the presence of internal storage cells in the registers of external devices and realization of active addressing of external devices (the devices report their own address upon interrupts).

All the systems characteristics of SM-3 and SM-4 complexes noted above provide effective joint operation of them with special processors of different classes, which expands the capabilities of using SM-3 and SM-4 in such fields as scientific and technical, engineering calculations, programming automation, complex signal processing and economic and statistical information processing.

The capability of using SM-3 and SM-4 to automate various functions in complex control systems simplifies to a significant degree combination of UVK into unified control systems, reduces programming expenditures and simplifies introduction and operation of the systems.

To provide delivery of SM-3 and SM-4 which correspond to the maximum degree to the diverse requirements of a wide range of customers, the following types of complexes are realized:

basic complexes. The minimum set of devices is the processor, two-three universal input-output devices, one or two external storage devices and software (including one or two general-purpose operating systems). These complexes are a serial product of the manufacturing plants;

specified complexes. They are produced by the manufacturing plant by orders (specifications) of users and include one or several basic SM-3 and SM-4 complexes and additional modules from the SM EVM nomenclature (expansion of the OZU [Internal storage] to 22K words for the SM-3 and to 124K words for the SM-4, sets of peripheral devices and interprocessor and intermachine communications devices). The software corresponds to the basic complex and is supplemented by drivers of connected devices;

problem-oriented complexes. They are developed for a specific set of applications combined by the unity of information processing technology. These complexes are constructed on the basis of specified complexes and may include additional nonstandard modules, devices from the nomenclature of other families of computers, modules of operating systems and applied problem packs which provide information processing in specific given modes for a specific set of objects.*

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* The principles of configuration of SM-3 and SM-4 complexes are considered in more detail in Chapter 5.

The systems engineering characteristics of complexes are determined to a significant degree by computer configuration.

1.2. General Data on the Configuration of the SM-3 and SM-4 UVK

Computer configuration is understood as everything that the machine offers to the program working at the level of machine instructions: the structure of the memory, addressing mechanisms, functional diagram of the processor, instruction formats, means of controlling peripheral devices, interrupt system and so on [3]. The efficiency of executing different tasks depends on the specific configuration properties of computers.

The configuration of the SM-3 and SM-4 UVK considered in this chapter provides the highest efficiency when solving problems of processing large information files structurally organized in the form of stacks, tables and queues, information gathering and processing and control in the real-time mode with high response of the system to interrupts from external devices, byte processing and information transmission. These problems are typical for many areas of application of computer equipment and primarily for systems where automation of scientific experiments and production processes and for automated production control systems and information-measuring systems.

The SM-3 and SM-4 UVK have unified configuration* and are compatible "from bottom to top." This compatibility means that an arbitrary routine in machine code executed on the SM-3 can also be executed on the SM-4 since all the configuration characteristics of the SM-3 are retained in the SM-4 UVK, which has more complete productivity achieved by use of additional configurational capabilities of the central processor of the SM-4 (compared to the SM-3) and also higher speed in the main instruction set (similar to the SM-3). Henceforth, when describing the configurational properties of the SM-3 UVK, it will mean that these properties are also related to the SM-4 UVK. The additional capabilities of the SM-4 complex will be especially stipulated.

The configuration of the SM-3 and SM-4 UVK differs significantly from that of most small computers. One of the typical features of any computer is the method of addressing the internal storage device (OZU). There is the problem of addressing a large volume of OZU for small computers, which usually have a 16-digit instruction format. This problem is solved in many small computers by means of indirect addressing through the "zero" memory page [1]. The capability of direct access to addresses of the "zero" page is provided in the instruction format since its capacity is usually small (256-2,048 words). The disadvantages of this method are obvious: two access cycles to the OZU are essentially required for each access to the operand; moreover, even with a small volume of the "zero" page in 16-digit instruction format, double-address instructions required to perform two-place operations of the addition, comparison and other types cannot be realized. Of course, these instructions are realized in computers which utilize the "zero" page principle. However, an internal register-storage device in which the result of the

*This family may also include the Elektronika-60 computer and the previously produced M-400 complex.

operation is stored is used as the second operand in this case. An additional instruction is used to refer to the contents of this register in the OZU.

Another method of addressing is used in the SM-3 UVK: addressing through one of the general purpose registers (RON) of the processor. The number of this register is indicated in the instruction format and essentially no time is expended on access to it when executing the instruction. The contents of the register are interpreted as a function of the addressing mode which is also given in the instruction format. There are eight of these registers and three digits are required for addressing any of them. This provides the capability of realizing single- and double-address instructions with 16-digit instruction format, which considerably facilitates programming at the machine instruction level.

Another characteristic feature of the SM-3 UVK is the use of a unified "Common bus" interface in which information exchange (addresses, data and control signals) between the processor and memory is accomplished by the same principle as between the processor and external device (VU).

Because of using this interface, special input-output instructions of the processor are no longer necessary; direct access to the OZU is simply realized, i.e., information exchange occurs without the participation of the processor between the VU and memory block or between two VU; the operating flexibility of the processor with the VU is enhanced since all the address instructions can be used to transmit and process information in the VU registers. A total of 4,096 old words of the addressed memory is allocated for addressing the VU registers, addressed the same as OZU cells. Thus, the configuration of the UVK (if the physical restrictions of the load capability of the "Common bus" lines are not taken into account) permits connection of a practically unlimited number of VU to the processor.

General-Purpose Registers of the Processor

The processor has eight 16-digit universal general-purpose registers (RON): R0-R7. These registers can be used both as storage devices, index registers, address displays, table displays, list displays and so on and also as memory range displays for temporary storage of data (stack). The specific use of the registers depends on the selected addressing mode.

Among these registers should especially be allocated R7 and R6 registers. The R7 register is used as an instruction counter, i.e., it contains the address of the next instruction to be executed, which permits several additional addressing modes to be achieved.

The processor utilizes the R6 register as a stack display during execution of some instructions which require temporary storage of data (for example, the return address during access to the subroutine). The programmer should determine the memory zone allocated for this stack (the address of the top of the stack is established). The programmer can use this stack for temporary storage of data.

The Word of Processor Status

Information about the current state of the processor (the word of processor status) is stored in a 16-digit register which is located in the processor (Figure 1.1).

The 0-3 digits of the SSP (word of processor status) are the conditional codes which contain information about the result of the last operation in the processor. The method of establishing the conditional codes depends on the instruction being executed and is given in the description of it. However, conditional codes are established in the following manner during execution of most instructions:

Z = 1, if the result is equal to zero;

N = 1, if the result is negative;

C = 1, if transfer from a high digit occurred as a result of the operation;

V = 1, if arithemtic overflow occurred as a result of the operation.

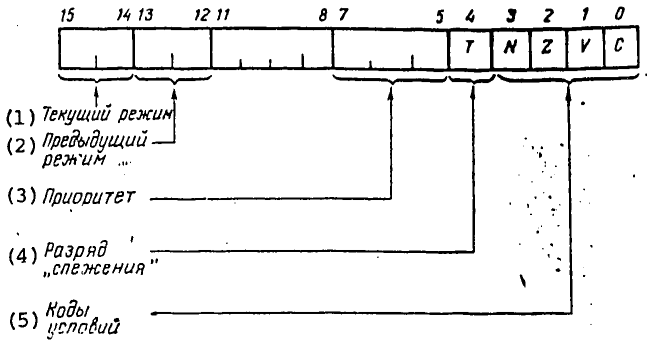


Figure 1.1. Word of Processor Status

Key:
1. Current mode
2. Previous mode
3. Priority
4. "Addition" digit
5. Conditional codes

The programmer may assign one of eight priority levels to the processor. To do this, he sets the corresponding code (0-7) in digits 5-7 of the SSP. If code 7 is set, not a single one of the external devices (VU) can interrupt the current routine.

Digit 4 of the SSP is the "addition" digit set or rejected by the programmer. If this digit is set before execution of any instruction, internal interrupt occurs. This property permits one to "track" the routine being executed and is used in different debugging routines (for example, in the "Debugger" routine in the DOS SM [Small computer disc operating system]).

The higher digits of the SSP are used only in the SM-4 processor. Digits 14 and 15 contain information about the current mode (user or systems) of the processor, while digits 12 and 13 contain information about the previous mode.

Organization of Memory

The minimum addressable unit of the OZU is the byte (eight binary digits) in the SM-3 UVK. Since the address network of the SM-3 is 16-digit, the address field of the OZU is equal to 0-64K bytes.* However, the instructions of the SM-3 UVK can perform operations both with bytes and with words consisting of two bytes. The OZU is a linear sequence of 8-digit cells (bytes) with addresses 0-157777 (older 8K bytes of the field being addressed with addresses of 160000-177777 are related to VU registers). Moreover, from the programmer's viewpoint the memory can be represented (Figure 1.2) in the form of a sequence of two-byte words with addresses 0-157776. An even address always corresponds to the lowest byte in the word and an odd address always corresponds to the highest byte. Word addressing is accomplished by even addresses.

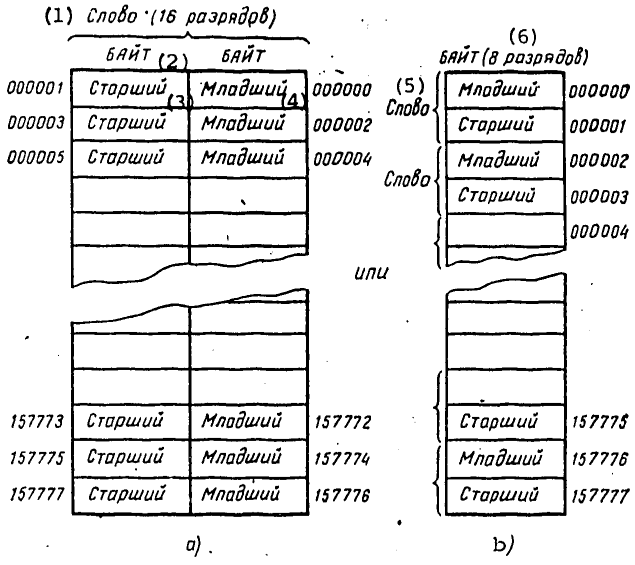


Figure 1.2. Organization of Memory

Key:
1. Word (16 digits)
2. Byte
3. Highest
4. Lowest
5. Word
6. Byte (8 digits)

As already pointed out, the highest 8K byte (or accordingly 4K words) of the addressed field is carried to the VU vectors. The lowest 256_8 words of the OZU are

*K is a symbol used in data processing systems as a measure of the capacity of storage devices or the speed of information transmission equal to 1,024 (2^{10}) units. For example, the capacity of an OZU equal to 16K means that it contains 16·1,024 = = 16,384 cells.

carried to the interrupt vectors (see Section 1.2).* This OZU zone is an ordinary memory and can be used by the programmer for any routine, but the systems routines are not guaranteed upon execution.

The SM-4 UVK processor contains hardware for addressing of 256K bytes or 128 K words. The 16-digit address formed by the instruction is convered by the memory dispatcher of the SM-4 to an 18-digit address displayed on the "Common bus" interface. If the memory dispatcher is switched off, this conversion is prohibited and the processor operates the same as the SM-3 processor. It should be noted that the "Common bus" interface contains 18 address lines. The SM-3 or SM-4 processor (if the memory controller is switched off) automatically prints out ones on the two highest "Common bus" address lines upon formation of addresses of the VU registers (160000-177777) by the instruction. Thus, the VU registers actually have addresses of 760000-777777.

The Stack

The stack is a method of organizing a file of memory elements in which the elements are recorded or sampled by the principle : the last recorded element is sampled first from the file. The address by which the element is sampled or recorded is called the top of the stack.

The configuration of the SM-3 and SM-4 UVK permits easy organization of stacks with sliding top. Any of the RON (except R7--the instruction counter) can be used as the indicator of the top of the stack and the automatic increase or automatic decrease modes permit regulation of the position of the top of the stack. Register R6 uses some instructions as the stack index to which data for temporary storage are carried. Therefore, R6 is called the index of the hardware stack and is denoted by US. The memory zone in which the hardware stack should be located is selected by the programmer. If there are instructions in the routine which utilize the hardware stack, the programmer should set the initial value of the address of the top of the stack in the US. The processor reduces the contents of the US by one-half upon recording to the hardware stack (when executing the corresponding instructions) and then records the new element by the address contained in the US. Upon sampling from the stack, the processor selects the element by the address contained in the US and then increases the contents of the US by two. The programmer can also use the region of the hardware stack for temporary storage of data. He should observe the following rule in this case: the contents of the US should be reduced by one-half prior to recording in the stack and it should be increased by two after sampling from the stack. The hardware stack is used only for word storage. The programmer can organize stacks consisting both of words and of bytes by using the remaining registers.

The System of Interrupts

Two types of interrupts from external storage devices (external interrupts) are possible in the SM-3 UVK:

*The interrupt vector is two OZU cells in which the programmer writes the routine address for interrupt processing and the SSP upon execution of the routine.

extraprocessor interrupt in which the external storage device exchanges data directly with the OZU without participation of the processor (this operating mode is frequently called direct-memory access);

routine interrupt in which control is transferred to a special interrupt processing routine.

There are four levels (by priority) of routine interrupts and one level of extraprocessor interrupt in the UVK.

Two lines each correspond to each level in the "Common bus" channel (Figure 1.3): the interrupt request ZPk (ZPD for extraprocessor interrupt) and interrupt authorization RPk (RPD--for nonprocessor interrupt). The letter "k" corresponds to the number of the level.

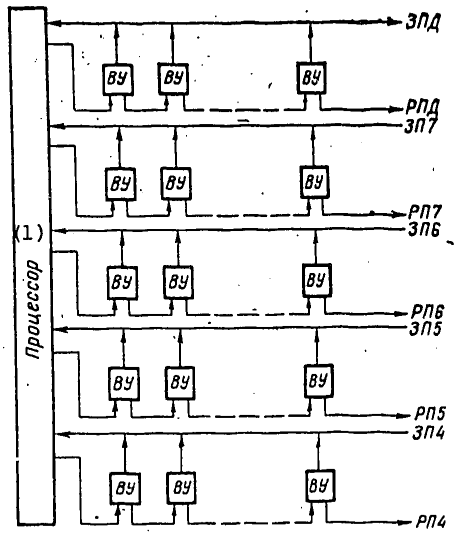


Figure 1.3. Diagram of Interrupt Request and Authorization

Key:
1. Processor

The devices which display the request to the ZPD line have the highest absolute priority. After one of these devices displays the request, a signal appears on the RPD line which authorizes the interrupt even if the processor has not completed execution of the current instruction. An exception are the cases:

if the processor transmits information over the "Common bus" at the moment of the request. The signal is displayed on the RPD line after completion of the transmission, i.e., at the end of the next "Common bus" cycle (there may be several cycles during execution of the instruction);

if less than 8 microseconds remain prior to completion of the execution of one of the long instructions with floating decimal in the SM-4. The signal on the RPD line appears after execution of this instruction.

The RPD line passes sequentially through all the devices located at this level. If several devices display a request simultaneously, the request of the device first connected to the RPD is satisfied since it should block further passage of the signal through the RPD (if it displayed the request). Thus, the device which is first connected physically to the RPD line has the highest relative priority among devices of this level.

Upon receiving a request through one of the ZP4-ZP7 lines, the processor compares the priority of the line (line ZP7 has the highest priority) with the priority of the processor indicated in the SSP. If the priority of the line is higher, the processor transmits a signal over the corresponding line of the RP after execution of the current instruction and begins to execute the interrupt procedure.

An interrupt does not occur if the priorities of the line of the ZP and the processor are equal.

If several devices display a request on the same line of the ZP, the request of the device which was first connected to the corresponding line of the RP is satisfied.

After receiving the RP signal, the device displays the address of its own interrupt vector over the lines of the "Common bus" data.

Upon receiving the address of the interrupt vector, the processor

stores the current SSP in the stack (i.e., in the memory cell whose address is in the US, first reducing this address by one-half);

stores the address of the next instruction of the interrupted program in the stack;

records the address of the subroutine of interrupt processing (the first word of the interrupt vector) in the instruction counter;

records the second word of the interrupt vector in the SSP register.

We shall call the described procedure interrupt by vector n (n is the address of the first word of the interrupt vector).

In some cases the described procedure of interrupt is fulfilled as a result of factors determined by the status of the processor (internal interrupts) rather than by request from the VU. The following types of interrupt are possible in this case:

interrupt with odd addressing--it occurs upon an attempt to execute an instruction in which an odd word address is indicated. The interrupt vector should be in cells 4 and 6;

interrupt upon loss of power supply--it occurs when the voltage of the AC network decreases below the normal level. The interrupt vector should be in cells 24-26. A total of 2 microseconds is allocated to execute the program whose address is recorded in cell 24.

Control is again transferred through vector 24 upon restoration of power supply to normal level;

interrupt during addressing of a nonexistent memory--it occurs upon an attempt to address a memory cell whose address is greater than the upper bound of the addressing of the OZU block. The interrupt vector should be in cells 4 and 6;

interrupt due to incorrect instruction--it occurs upon an attempt to execute an instruction with operation code not included in the instruction set. The interrupt vector should be in cells 10 and 12;

interrupt due to an addition digit--it occurs if an addition digit is set prior to execution of any SSP instruction. The interrupt vector should be in cells 14 and 16.

1.3. Addressing Modes

Addressing is accomplished in the SM-3 UVK by eight RON registers. This addressing is indirect from the programmer's viewpoint. However, this is not actually true since the registers are inside the processor and essentially no time is expended on access to them. The format of the address instructions, besides the operating code, includes the address field which determines the addressing of one or two operands (Figure 1.4). The address field of two-address instructions is the source field and the reception field. The address field of single-address instructions consists only of the reception field. The source field (the same as the reception field) contains the number of one of the RON (three digits) and the number of the addressing modes (three digits). The addressing mode determines the method of interpretation of the contents of the selected register. A description of the main addressing modes is presented in Table 1.1.

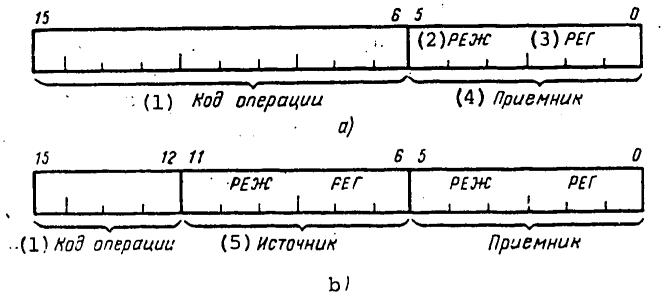


Figure 1.4. Formats of Single- (a) and Two-Address Instructions (b)

Key:
1. Operating code
2. Mode
3. Register
4. Receiver
5. Source

To use the contents of the register as an address (or the address of an address in indirect modes) of the operand, this address (or the address of the address) must

first be entered in the given register. Since additional time is required for this, the indicated method is used only when processing information files when the set register can once serve multiply to address sequential memory cells. In this case the work is carried out with automatic increase or decrease of the register contents by one or two after execution of each instruction with access to a given register. Thus, the address of the next byte (with an automatic increase or decrease by one) or of a word (with automatic increase or decrease by two) is prepared in the register. It should be noted that an automatic increase (or decrease) is always by two when using indirect modes 3 and 5 since the register contairs the address which is always a 16-digit (two byte) word rather than the operand in this case.

Table 1.1. Main Addressing Modes

Direct Modes (Operand Address Is Formed)		Indirect Modes (Address of the Operand Address Is Formed)		Description of Mode
Number of Mode	Mnemonic Code	Number of Mode	Mnemonic Code	
0	R_n	1	@ R_n	The contents of the register are the operand in mode 0 and the address of the operand in mode 1
2	$(R_n)+$	3	@$(R_n)+$	The contents of the register are used as the address (or the address of the address) of the operand and is then increased by one or two (in mode 2) and is always increased by two in mode 3
4	$-(R_n)$	5	@$-(R_n)$	The contents of the register are reduced by one or two (in mode 4) and are always reduced by two in mode 3; it is then used as the address (or the address of the address) of the operand
6	$X(R_n)$	7	@ $X(R_p)$	The contents of the register are added to those of cell X following the instruction; the sum is used as the address (or the address of the address) of the operand

Note. n is the number of the selected register.

Examples of using addressing modes in the instructions of the SM-3 and SM-4 EVK are presented in Table 1.2.

Register R7 (the instruction counter), which we will subsequently denote by SK, is used as the RON for working with individual cells of the OZU. This counter always contains the address of the cell following the executed instruction. Thus, if the SK is used as an RON in the addressing field, preliminary setting of the register (SK in the given case) is not required. Although the SK can be used in any of the main addressing modes, work with the SK is practically feasible in only four of these modes. From the programmer's viewpoint, four additional addressing modes

(direct, absolute, relative and indirect-relative) are possible, although these modes in no way differ with respect to apparatus from the corresponding modes with use of other registers. Addressing modes using the SK as a general-purpose register are presented in Table 1.3.

Table 1.2. Examples of Using Addressing Modes

(1) № п/п	(2) Мнемоника	(3) Код операции	(4) Описание	(5) Содержимое регистров и ячеек памяти: (6) до выполнения команды	(7) после выполнения команды
1	INC R3	005203	Увеличить на единицу содержимое регистра R3 (8)	(R3) = 000777	(R3) = 001000
2	INC @ R3	005213	Увеличить на единицу содержимое ячейки 1000 (9)	(R3) = 001000 (1000) = 002000	(R3) = 001000 (1000) = 002001
3	INC (R3)+	005223	Увеличить на единицу содержимое ячейки 1000 (10)	(R3) = 001000 (1000) = 002001	(R3) = 001002 (1000) = 002002
4	DEC @ (R3)+	005033	Уменьшить на единицу содержимое ячейки 3010 (11)	(R3) = 001002 (1002) = 003010 (3010) = 002365	(R3) = 001004 (1002) = 003010 (3010) = 002364
5	MOV—(R3), R4	014304	Переслать содержимое ячейки 1002 в регистр R4 (12)	(R3) = 001004 (1002) = 003010 (R4) = 005020	(R3) = 001002 (1002) = 003010 (R4) = 003010
6	CLR @—(R4)	005054	Очистить содержимое ячейки 5000 (13)	(R4) = 003010 (3006) = 005000 (5000) = 012475	(R4) = 003006 (3006) = 005000 (5000) = 000000
7	MOV 2(R4), R1 000002	016401	Переслать содержимое ячейки 3010 в регистр R1 (14)	(R4) = 003006 (3006) = 005000 (R1) = 000175 (3010) = 002364	(R4) = 003006 (3006) = 005000 (R1) = 002364 (3010) = 002364
8	CLR @ 2(R4) 000002	005074	Очистить содержимое ячейки 2364	(R4) = 003006 (3006) = 005000 (3010) = 002364 (2364) = 000005	(R4) = 003006 (3006) = 005000 (3010) = 002364 (2364) = 000000

Key:
1. Number of item
2. Mnemonic code
3. Operating code
4. Description
5. Contents of registers and memory cells
6. Prior to execution of instruction
7. After execution of instruction
8. Increase contents of register R3 by one
9. Increase contents of cell 1000 by one
10. Decrease contents of cell 3010 by one
11. Transmit contents of cell 1002 to register R4
12. Erase contents of Cell 5000
13. Transmit contents of cell 3010 to register R1
14. Erase contents of cell 2364

Let us consider the features of absolute and relative addressing. Relative addressing is used mainly when writing so-called position-independent routines (which are not dependent on position in the OZU). If the routine is designed for transfer in the memory, absolute addressing cannot be used in most cases since the direct address of the operand, which changes its value upon transfer of the routine, is contained in the second word of the instruction. The difference between the current position of the instruction (i.e., the contents of the SK) and the actual address of the operand is stored in the second word with relative addressing. If the entire routine is transferred to another position of the OZU, this difference is stored and consequently the operation will be executed correctly. However, there are special cells which have fixed addresses not dependent on the position of the routine (for example, addresses of interrupt vectors and registers of devices). Absolute addressing must be used upon access to these cells, otherwise access to these cells will be incorrectly executed when the routine is transferred.

Table 1.3. Addressing Modes Using SK as General-Purpose Register

Addressing Mode	Number of Addressing	Mnemonic Code	Description
Direct	2	#N	Contents of N cell following the first word of instruction is the operand
Absolute	3	@#A	Contents of A cell following the first word of instruction is address of operand
Relative	6	A	Contents of cell following the first word instruction is added to contents of SK; the sum A is address of the operand
Indirect-relative	7	A	Contents of cell following the first word of instruction is added to contents of SK; sum A is address of address of operand

Examples of using addressing modes with the instruction counter as the general-purpose register are presented in Table 1.4.

When executing the instruction presented in example 1 (the direct addressing mode), the following occurs. After the instruction is sampled, the SK in the processor is always automatically increased by two. Then, since mode 2 is being used, the contents of the SK are interpreted as the address (2002 in the given case) of the operand, i.e., the operand is the second word of the instruction. Thus, this mode permits one to be given constants in the routine by storage of this constant in the second word of the instruction and by using the register mode with automatic increase of register SK. An automatic increase is necessary since otherwise the constant is interpreted as the next instruction.

The operations are executed similar to the previous mode in the absolute addressing mode (example 2). However, the contents of the SK are interpreted as the address of the operand address, i.e., the address of the operand is the second word of the instruction.

The processor again turns to the memory for the index word by the address contained in the SK in the relative addressing mode (example 3) after selecting the instruction and increasing the contents of SK by two, after which it again increases the

Table 1.4. Examples of Using Addressing Modes With Instruction Counter

(1) Мнемоника	(2) Код команды	(3) Описание	(4) Содержимое регистров и ячеек памяти	
			(5) до исполнения команды	(6) после исполнения команды
MOV # 300, R0	012700 000300	(7) Переслать число 300 в регистр R0	(R0) = 001000 (2000) = 012700 (CK) = 002000 (2002) = 000300	(R0) = 000300 (2000) = 0127000 (CK) = 002004 (2002) = 000300
CLR @ # 300	005037 000300	(8) Очистить ячейку 300	(CK) = 00200 (300) = 000225 (200) = 005037 (202) = 000300	(CK) = 002004 (300) = 000000 (2000) = 005037 (2002) = 000300
INC 300	005267 000074	(9) Увеличить на единицу содержимое ячейки 300	(CK) = 000200 (200) = 005267 (202) = 000074 (300) = 000000	(CK) = 000204 (200) = 005267 (202) = 000074 (300) = 000001
CLR @ 300	005267 000074	(10) Очистить ячейку 500	(CK) = 000200 (200) = 005077 (202) = 000074 (300) = 000500 (500) = 001001	(CK) = 000204 (200) = 005077 (202) = 000074 (300) = 000500 (500) = 000000

Key:
1. Mnemonic code
2. Instruction code
3. Description
4. Contents of registers and memory cells
5. Prior to execution of instruction
6. After execution of instruction
7. Transmit number 300 to register R0
8. Erase cell 300
9. Increase by one the contents of cell 300
10. Erase cell 500

contents of SK by two. Since the addressing mode is index type, the processor adds the index word to the contents of the selected register, which the SK register is in the relative mode. The sum (74 + 204 = 300 in the given example) is the address of the operand.

The indirect-relative addressing mode (example 4) is similar to the previous one, only the sum of the index word and the contents of the SK are interpreted as the address of the operand address.

1.4. The Instruction Set

All the instructions contained in the instruction set of the SM-3 and SM-4 UVK are separated into groups (single-address, two-address, transfer instructions and so on) and into subgroups. This separation is purely arbitrary in some cases and is made for purposes of convenience of outline.

Formal description of the instructions is given in Tables 1.5-1.10. The name, mnemonic notation (used in writing routines in Assembler language), the formal algorithm and the verbal description are presented in these descriptions. The following notations are used in formal description of the instructions:

(XXX)	--contents of XXX	→	--"becomes"
ist	--source address	↑	--selection from stack
prm	--receiver address	↓	--recording to stack
&	--"AND" function (logic multiplication)	Z	--digit of zero character in word of state
!	--"OR" function (logic addition)	N	--digit of minus character in word of state
ⓘ	--"EXCLUDING OR" function (addition modulo 2)	C	--digit of transfer character in word of state
-	--feature from top--"NOT" function (inversion)	V	--digit of overflow character in word of state

This formal description is quite adequate to understand the word of some instructions. However, let us consider more instructions in more detail. Special attention should be turned toward methods of setting the conditional codes. In the general case conditional codes are set according to the definitions given in 1.1. However, when executing some instructions, the conditional codes are set in a special manner. In these cases the method of setting the conditional codes is stipulated especially in the description of the instruction.

Single-Address Instructions

Formal description of single-address instructions is presented in Table 1.5. Their format is shown in Figure 1.4, a. Six digits of the instruction code are allocated for the address field, which contains the number of the addressing mode and the number of one of the RON which determines the address of the operand according to the rules considered in 1.3. The remaining 10 digits in the instruction format are allocated for the operating code.

Special attention should be turned toward the rules for setting the transfer and overflow digits in the arithmetic instructions (understanding of this problem is also important when using two-address instructions and transfer instructions).

Let us consider methods of displaying numerical information in the SM-3 UVK. Numbers can be displayed in two forms in the SM-3: with and without a sign. Numbers with a sign are displayed in a supplementary code and have ranges of -2^7-2^7-1 (when operating with bytes) and $-2^{15}-2^{15}-1$ (in operations with words). If the result of the operation goes beyond this range when executing arithmetic instructions, the overflow digit V is set in the SSP. Display of numbers without a sign has ranges of $0-2^8-1$ (in operations with bytes) and $0-2^{16}-1$ (in operations with words). If the result of the operations goes beyond this range during execution of arithmetic instructions, the transfer digit C is set in the SSP. Thus, when executing arithmetic instructions, the transfer digit is actually the overflow index for representation of numbers without a sign. Single-address instructions can execute operations both with bytes and with words. An exception are SWAB and SXT instructions (the SXT instruction is realized only in the SM-4 UVK), for which operations with bytes are meaningless. The feature of byte operation is a one in digit 15 of the instruction code. The letter B is added in the mnemonic notation of the instruction in this case.

Arithmetic instructions. There are three single-address arithmetic instructions INCREMENT (INC), DECREMENT (DEC) and CLEAR (CLR) in the instruction set of the SM-3 UVK.

The operand always contains a zero after execution of the CLR instruction. Therefore, digit Z is set to one and digit N is dropped to zero. Digits V and C are also dropped to zero.

The INC instruction adds one to the contents of the operand. Let us consider the case when the operand contains the number 077777 (or 177 for operations with bytes), which is the maximum positive integer in character representation of numbers, prior to execution of this instruction. As a result of adding one to this number, the number 100000 is found, which is negative (i.e., overflow occurs). Therefore, digit V is set to one in this case.

The DEC instruction subtracts a one from the contents of the operand. The condition of reset when using this instruction occurs if the number 100000 (or 200 for byte operations) is contained in the operand, which is the maximum negative number. It is natural that subtraction of a one from this number leads to the sign representation of the numbers leaving the range and digit V is set to one.

The INC and DEC instructions do not change the status of digit C even if carry occurs (i.e., arithmetic overflow with display of numbers without a sign). This is determined by the fact that the lowest (or highest digit of the shifted word (byte) which should be used in the next shift cycle is recorded to digit C in the instructions of the cyclic shift. Thus, instructions (for organization of program cycles) which do not change the state of digit C are required when organizing a multiple cyclic shift.

Logic instructions. Only the corresponding setting of digits Z and N occurs as a result of executing the TEST (TST) instruction. Digits V and C are dropped to zero. the contents of the operand do not change in this case. This instruction is usually employed to determine the carry conditions at points of program branching.

Table 1.5. Single-Address Instructions

Number of Item	Instruction	Mnemonic Code	Operating Code	Algorithm	Description
1	CLEAR	CLR	0050	(prm)←0	All reception digits are dropped to zero
2	INCREMENT	INC	0052	(prm)←(prm) + 1	One is added to the contents of the receiver
3	DECREMENT	DEC	0053	(prm)←(prm) - 1	One is subtracted from the contents of the receiver
4	NEGATOR	COM	0051	(prm)←$\overline{(prm)}$	All reception digits are inverted
5	TEST	TST	0057	--	Digits of conditional codes are set. Contents of receiver do not change
6	NEGATOR	NEG	0054	(prm) ←- (prm)	Sign of receiver contents changes to opposite
7	ARITHMETIC SHIFT TO RIGHT	ASR	0062	--	All digits of receiver contents shift by one digit to the right. Value of zero digit of receiver is carried to digit C. Digit 15 (or 7)* does not change
8	ARITHMETIC SHIFT TO LEFT	ASL	0063	--	All digits of receiver contents shift by one digit to left. Value of digit 15 (or 7)* of receiver is carried to digit C. A zero is carried to digit 0 of receiver
9	CYCLIC SHIFT TO RIGHT	ROR	0060	--	All digits of receiver contents shift by one digit to right. Value of digit C is carried to digit 15 (or 7)* of

*In operations with bytes.

[Table continued on following page]

Table 1.5. [Continued from preceding page]

Number of Item	Instruction	Mnemonic Code	Operating Code	Algorithm	Description
					receiver. Value of digit 0 of receiver is carried to digit C
10	CYCLIC SHIFT TO LEFT	ROL	0061	--	All digits of receiver contents are shifted by one digit to left. Value of digit C is carried to digit 0 of receiver. Value of digit 15 (or 7)* is carried to digit C
11	ADDITION WITH CARRY	ADC	0055	(prm)←(prm) + (C)	Value of digit C is added to contents of receiver
12	SUBTRACTION OF CARRY	SBC	0056	(prm)←(prm) - (C)	Value of digit C is subtracted from receiver contents
13	BYTE PERMUTATION	SWAB	0003	--	Highest and lowest bytes of receiver contents change places
14	SIGN DISTRIBUTION	SXT	0067	(prm)←0, if N = 0 (prm)← -1 , if N = 1	All digits of receiver are filled with ones or zeros as a function of the value of digit N

*In operations with bytes.

The NEGATION (NEG) instruction changes the sign of the operand, i.e., the operation of conversion of the number to supplementary code is carried out. If the operand is equal to 100000, digit V is set to one upon execution of this instruction. This occurs because the number 100000 (-2^{15}) is the maximum negative number to which no positive number corresponds (modulo) in the supplementary code. This means that the result of the operation goes beyond the range of the sign representation of the numbers. Digit C is always set to one with the exception of the case when the operand contains zero. The negation operation carried out on any number (except zero) means an attempt to find a negative number which does not exist in representation without a sign.

The INVERSION (COM) instruction executes digit by digit inversion of the operand, i.e., the operation of transfer to reverse codes. In this case digit V is always dropped to zero and digit C is set to one.

Shift instructions. The arithmetic shift instructions ASR (ASL) accomplish the operation of shifting the operand by one digit to the right (or to the left). In this case the "expelled" lowest (highest) digit of the operand is written in digit C. Upon a shift to the right, the highest digit of the operand retains its value which it would have prior to execution after execution of the operation. Upon a shift to the left, a zero is written in the lowest digit of the operand. The operation of the arithmetic shift instructions is illustrated by Figure 1.5.

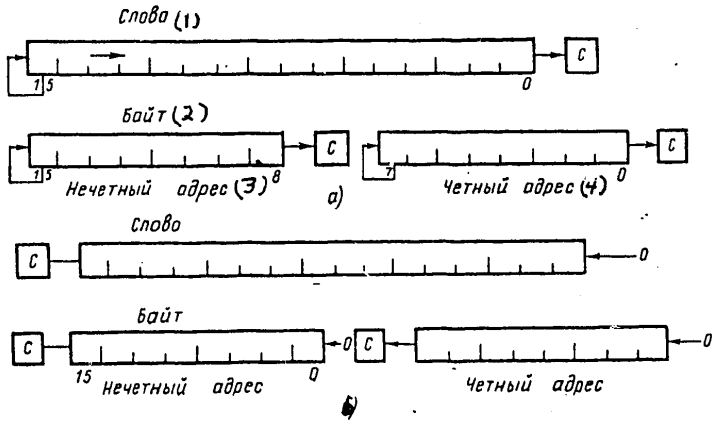


Figure 1.5. Execution of Format Shift to Right (a) and to Left (b)

Key:
1. Word
2. Byte
3. Odd address
4. Even address

The cyclic shift instructions ROR (ROL) also accomplish the operation of shift of the operand by one digit to the right (or left). In this case the contents of digit C are recorded in the highest (lowest) digit of the operand. The "expelled" lowest (highest) digit of the operand is written the same as in the arithmetic shift. Thus, the cyclic shift of a 17-digit (or nine-digit with byte operations) register consisting of an operand and digit C is accomplished. When organizing

a multiple cyclic shift of the operand, the programmer should not use instructions which change the state of digit C. The work of cyclic shift instructions is illustrated by Figure 1.6.

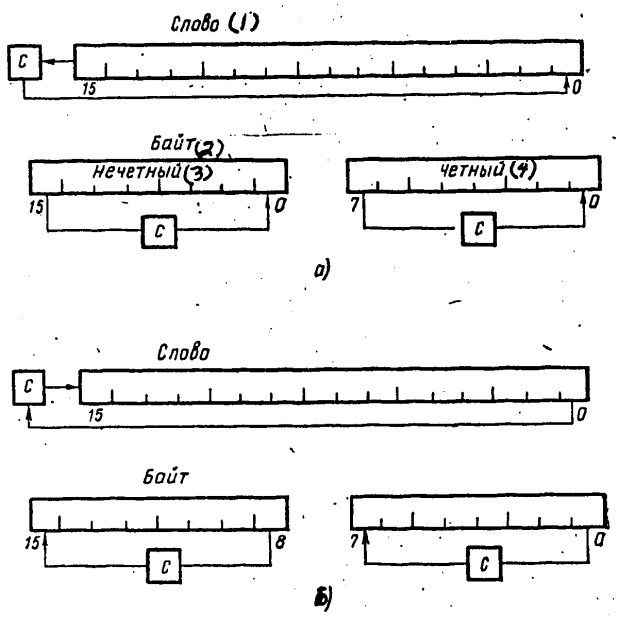


Figure 1.6. Execution of Cyclic Shift Instructions to the Left (a) and to the Right (b)

Key:

1. Word
2. Byte
3. Odd
4. Even

Instructions for working with increased accuracy. The 16-digit format of a machine word places restrictions on the range of represented numbers. If this range must be expanded, the operands are represented in the form of several words (or bytes). Arithmetic operations are executed separately on the highest and lowest parts of the operands. If a digit C is set above the lowest parts during the operation, this means that the result exceeds the range of the lowest part of the operand and this should not be taken into account during operation on the highest parts of the operand. The ADDITION WITH CARRY (ADC) and SUBTRACTION WITH CARRY (SBC) instructions are used for this purpose.

For example, if two numbers with double accuracy, one of which is recorded in registers R1 and R2 and the second of which is recorded in registers R3 and R4 must be added, the following sequence can be used:

```
ADD R1 AND R3; add the smallest parts;

ADC R4; add the value of carry to the highest part;
```

ADD R2 AND R4; add the highest parts.

The SIGN DISTRIBUTION (SXT) instruction is used to facilitate working with negative numbers. It permits transfer of the number contained in the word to an equivalent word with double accuracy (with regard to sign), consisting of two words. Digit Z is set to one if the initial word is positive (since the second word is filled with zeroes in this case). Digits N, V and C are dropped to zero. This instruction is realized only in the SM-4 UVK and does not execute operations with bytes.

The SWAB instruction. The highest and lowest bytes in the word change places as a result of executing the BYTE PERMUTATION (SWAB) instruction. For example, if the number 123456_8 was in register R0 prior to execution of the SWAB R0 instruction, the number 027247$_8$ will be contained in it after execution. Conditional codes Z and N are set according to the contents of the lowest byte of the result. Digits V and C are dropped to zero. This instruction is convenient in packing (or unpacking) of data which represent a byte file entered (or read) from the VU. It is obvious that this instruction does not perform operations on bytes.

Two-Address Instructions

Arithmetic-logic instructions. Formal description of these instructions is presented in Table 1.6. The format is shown in Figure 1.4, b. As can be seen from the figure, the instruction code consists of two address fields and an operating code field. Each address field is formed the same as the address field of single-address instructions. The address formed in digits 5-11 is called the source address and that formed in digits 0-5 is called the receiver address. The result of the operation is always transmitted through the receiver address. Digits 12-15 of the instruction code are allocated for the operating code field. Two-address arithmetic-logic instructions can perform operations both on words and on bytes. An exception are ADD (ADD) and SUBTRACT (SUB) instructions. The feature of byte operation is a one in digit 15 of the instruction code, the same as in single-address instructions. The letter B is added in the mnemonic notation of the instruction.

The TRANSMISSION (MOV) instruction is found more frequently than others in programs written in the instruction codes of the SM-3 UVK. The conditional code digits Z and N are set according to the contents of the operand-source during its execution. This permits one to avoid in some cases the use of the supplementary test instruction (TST) at points of program branching. Digit V is dropped to zero and the contents of digit C do not change. The operation is performed in similar fashion during byte transmission. Recording is performed in the lowest byte of the register upon transmission of a byte from the memory to the register of the processor, which has a 16-digit format, while the sign of the operand-source is "distributed" in the highest byte. For example, if the number 350_8 is contained in the byte by address 1001, the number 177750_8 will be recorded in register R3 after execution of the instruction MOVB 1001, R3.

When executing the instructions ADD (ADDITION) and SUB (SUBTRACTION), the result of the operation is stored by the address of the second operand, i.e., the receiver. The previous contents of the receiver are lost. These instructions do not perform operations on bytes. Setting the conditional codes corresponds completely to standard definitions of these codes. This means that digit V is set to one if the

Table 1.6. Two-Address Arithmetic-Logic Instructions

Number of Item	Instruction	Mnemonic Code	Operating Code	Algorithm	Description
1	TRANSMISSION	MOV	01	(prm) (ist)	Contents of source are transmitted through receiver address
2	COMPARISON	CMP	02	(ist) — (prm)	Contents of receiver are subtracted from contents of source. Both operands do not change
3	DIGIT CHECK	BIT	03	(ist) & (prm)	Logic multiplication operation over contents of source and receiver is executed. Both operands do not change
4	DIGIT CLEAR	BIC	04	(prm) (prm) & $\overline{\text{(ist)}}$	Digits of source contents equal to one, drop corresponding digits from receiver contents
5	DIGIT SETTING	BIS	05	(prm) (prm)! (ist)	Logic addition operation on contents of source and receiver is executed
6	ADDITION	ADD	06	(prm) (prm) + + (ist)	Contents of Source and receiver are added
7	SUBTRACTION	SUB	16	(prm) (prm) - - (ist)	Contents of source are subtracted from contents of receiver

Table 1.7. Supplementary Arithmetic-Logic Instructions of SM-4

Number of Item	Instruction	Mnemonic Code	Operating Code	Algorithm	Description
1	MULTIPLICATION	MUL	070	R_n, $R_{n+1} \leftarrow R^*_n$ (ist)	The contents of register R_n are multiplied by the contents of the source. The result of the operation is stored in registers R_n and R_{n+1}
2	DIVISION	DIV	071	R_n, $R_{n+1} \leftarrow R_n$, R_{n+1}/(ist)	The double word consisting of the contents of registers R_n and R_{n+1} is divided by the contents of the source. The result of the operation is stored in R_n (quotient) and in R_{n+1} (remainder)
3	MULTIPLE SHIFT	ASH	072	--	The contents of register R_n are shifted by N digits to the left (N < 0) or to the right (N > 0). The number of shifts of N is found in the sixth lowest digits of the source.
4	COMBINED MULTIPLE SHIFT	ASHC	073	--	The double word consisting of the contents of registers R_n and R_{n+1} is shifted by N positions to the left (N > 0) or to the right (N < 0). The number of shifts of N is found in the sixth lowest digits of the source
5	EXCLUDING "OR"	XOR	074	(prm)$\leftarrow$(prm) $\oplus$ R_n	The operation excluding "OR" is executed on the contents of the selected register and receiver. The result is placed according to the address of the receiver

result of addition (or subtraction) goes beyond the range -2^{15}-2^{15}-1. Digit C is set if the result goes beyond the range of a representation without a sign. Overflow can also be determined by another method. During addition, digit V is set to one if both operands had identical signs and the result had an opposite sign. During subtraction, digit V is set to one if the operands had different signs and if the sign of the result coincides with that of the source. Digit C is set to one if the result goes beyond the range of the representation without a sign. In other words, during addition, digit C is set to one if there was carry from the highest digit of the result and during subtraction digit C is set to one if this carry was not present.

The instruction COMPARISON (COMP) subtracts the contents of the receiver from those of the source. In this case the contents of the source and receiver do not change since the result of subtraction is not stored anywhere. Therefore, the only result of this operation is setting the digits of the conditional codes. These digits are set the same as when executing instructions SUB if the difference in setting the overflow digit V is not considered. Since the contents of the receiver are subtracted from those of the source when executing the instruction CMP (the contents of the source are subtracted from those of the receiver when executing the instruction SUB), digit V is set to one if the operands had different signs and if the sign of the result coincides with that of the receiver rather than the source. The instruction CMP is used to compare the contents of two elements (registers or memory cells) at the points of program branching.

The instruction DIGIT SETTING (BIS) executes the operation of logic addition of the contents of the source and receiver. This instruction is used to set a specific combination of digits (indicated in the source) in the receiver. All the digits previously set in the receiver remain in the same state. Digit V is dropped to zero and the value of digit C does not change.

The instruction DIGIT CLEAR (BIC) executes the operation of logic multiplication of the contents of the receiver and of the inverted contents of the source. This instruction is used to drop the specific combination of digits (indicated in the source) in the receiver to zero. All the digits previously set in the receiver remain in the same position. Digit V is dropped to zero and the value of digit C does not change.

The operation of logic multiplication of the contents of the source and receiver occurs by the instruction DIGIT TEST (BIT). Only the conditional codes are set as a result. The contents of the source and receiver do not change. The instruction is used to check the setting of a specific combination of digits (indicated in the source) in the receiver. This check is usually accomplished at the points of programmer branching. Digit V is dropped to zero while the value of digit C does not change.

Supplementary arithmetic-logic instructions of the SM-4. Formal description of these instructions is presented in Table 1.7. These instructions are also related to the group of two-address instructions, but have a different format (Figure 1.7). As can be seen from the figure, the processor register is always indicated as one of the operands. The source-operand is formed by the same rules as the operand in single-address instructions.

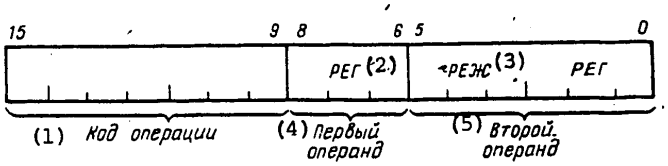


Figure 1.7. Format of Supplementary Arithmetic-Logic Instructions of SM-4 UVK

Key:

1. Operating code
2. Register
3. Mode
4. First operand
5. Second operand

When executing the instruction MULTIPLICATION (MUL), the register indicated in the instruction code is used as the receiver-operand. Since 32 binary digits are required to represent the results of multiplication of two 16-digit numbers, this result is carried to two registers: indicated in the instruction code and in the one following it by number. For example, if register 4 is indicated in the instruction code, the result will be found in registers R4 and R5 after execution of instruction MUL. If the number of the register of the receiver is odd, only the lowest part of the result in this register is stored. The digit is dropped to zero and digit C is set to one if the result of the operation goes beyond the range $-2^{15}-21^{-15}-1$.

Two registers are also used in execution of the instruction DIVISION (DIV). Thus, the 32-digit dividend contained in registers R_n and R_{n+1} is divided by the 16-digit divisor which is found in the source-operand. The result of division is transmitted to register R_n (the quotient) and to register R_{n+1} (the remainder). The number of register R_n should be even. Digit V is set to one in two cases: if the divisor is equal to zero and if the absolute value of the highest part of the dividend (i.e., the contents of the register) is greater than the absolute value of the divisor. In this case the instruction is not executed since more than 15 digits are required to represent the absolute value of the quotient. Digit C is set to one if the divisor is equal to zero.

The instruction MULTIPLE SHIFT (ASH) shifts the selected register to the right or left by K positions. The number of K positions is stored in the supplementary code in the six lowest digits of the source. If capital K is less than zero, a shift to the right is made and if K is greater than zero, a shift to the left is made. Thus, the contents of the register can be shifted by 32 positions to the right and by 31 positions to the left when executing a single instruction ASH. If K is equal to zero, the contents of the register. Digit V is set to one if the sign of the digit of the selected register changes during the shift. The value of digit 15 (with a shift to the left) or zero (with a shift to the right), which was in the register prior to the last shift, is carried to digit C.

The instruction COMBINED MULTIPLE SHIFT (ASHC) is used when working with double accuracy. The double word consisting of the register indicated in the instruction and the register following it by number is shifted when executing this instruction.

The number of shifts and setting of digits V and C are determined the same as in the instruction ASH.

The instruction EXCLUDING OR (XOR) fulfills digit by digit addition modulo 2 (otherwise the operation "EXCLUDING OR") of the source and receiver operands is executed. Digit V is dropped to zero and the value of digit C does not change.

Floating arithmetic instructions of the SM-4 UVK. Instructions for executing all four arithmetic operations over numbers with floating decimal (floating arithmetic instructions) are provided in the SM-4 UVK. Formal description of these instructions is presented in Table 1.8.

The exponent (eight digits) separates the mantissa from the sign of the mantissa. The mantissa is always normalized, i.e., the decimal point is located to the left of the most significant digit. The most significant digit of the normalized mantissa is not stored in the memory since it is always equal to one in positive numbers and it is always equal to zero in negative numbers. The exponent changes accordingly upon normalization of the number. The exponent is stored by a value increased by 200_8 (128_{10}). The sign of the exponent is stored in the 14th digit of the highest half of the number and is considered as a one for a positive exponent and as a zero for a negative exponent. Thus, the exponent may vary from -128 to +127. The result of the operation with floating decimal is always distinct from zero. If the exponent is equal to zero, the number is considered equal to zero regardless of the sign digit and value of the mantissa. In this case zeroes are formed by apparatus in all 32 digits of the number.

Table 1.8. Floating Arithmetic Instructions of SM-4 UVK

(1) № п/п	(2) Команда	(3) Мнемоника	(4) Код операции	(5) Алгоритм
1	СЛОЖЕНИЕ (6)	FADD	07500	[(R)+4, (R)+6]←[(R)+4, (R)+6]+[(R), (R)++2], если результат$\geqslant 2^{-128}$, иначе [(R)+4, (R)++6]←0 (10) (11)
2	ВЫЧИТАНИЕ (7)	FSUB	07501	[(R)+4, (R)+6]←[(R)+4, (R)+6]−[(R), (R)++2], если результат$\geqslant 2^{-128}$, иначе [(R)+4, (R)++6]←0 (10) (11)
3	УМНОЖЕНИЕ (8)	FMUL	07502	[(R)+4, (R)+6]←[(R)+4, (R)+6]×[(R), (R)++2], если результат$\geqslant 2^{-128}$, иначе [(R)+4, (R)++6]←0 (10) (11)
4	ДЕЛЕНИЕ (9)	FDIV	07503	[(R)+4, (R)+6]←[(R)+4, (R)+6]/[(R), (R)++2], если результат$\geqslant 2^{-128}$, иначе [(R)+4, (R)++6]←0 (10) (11)

Key:

1. Number of item
2. Instruction
3. Mnemonic code
4. Operating code

[Key continued on following page]

[Key continued from preceding page]

5. Algorithm
6. ADDITION
7. SUBTRACTION
8. MULTIPLICATION
9. DIVISION
10. If the result
11. Otherwise

Digits 3-16 are shifted under the operating code in the floating arithmetic instruction format. The three lowest digits indicate the register which serves as the operand stack. The operands in the stack are arranged in the following manner (the addresses of the memory cells are indicated from the left):

(R)--highest half of operand B;

(R)+2--lowest half of operand B;

(R)+4--highest half of operand A;

(R)+6--lowest half of operand A.

The result of the operation is stored in cells (R)=4 and (R)+6. The stack index contains the address of the first word of the result after execution of the instruction. Digits V and C are dropped to zero.

Carry Instructions

Formal description of the carry instructions is presented in Table 1.9. The highest byte of the instruction contains the operating code and the lowest byte contains the eight-digit shift, which is a number with sign which determines the carry address. This address is calculated by the processor in the following manner:

the sign digit of the shift byte is copied in digits 8-15;

the result is multiplied by two;

the result is added to the value of the instruction counter to find the carry address.

The assembler carries out reverse conversion of the carry address to form the shift byte.

The eight-digit shift permits carry by 200_8 words (or 400_8 bytes) of relatively current value CK backward and by 177_8 words (376_8 bytes) forward.

When executing the carry instructions, the processor analyzes the logic expression in which digits of the conditional code of the SSP are used as the Boolean variables. Transfer of control by the address determined by the shift value stored in the instruction code or carried to the following instruction is accomplished on the basis of this analysis.

All carry instructions can be conditionally divided into four groups. The first group includes a single instruction--UNCONDITIONAL CARRY (BR). Transfer of control

Table 1.9. Carry Instructions

Number of Item	Name of Carry	Mnemonic Code	Operating Code	Carry Condition
1	UNCONDITIONAL	BR	0004	
2	BY INEQUALITY TO ZERO	BNE	0010	Z = 0
3	BY EQUALITY TO ZERO	BEQ	0014	Z = 1
4	BY PLUS	BPL	1000	N = 0
5	BY MINUS	BMI	1004	N = 1
6	BY ABSENCE OF OVERFLOW	BVC	1020	V = 0
7	BY OVERFLOW	BVS	1024	V = 1
8	BY ABSENCE OF CARRY	BCC	1030	C = 0
9	BY CARRY	BCS	1034	C = 1
10	BY "GREATER THAN OR EQUAL TO ZERO"	BGE	0020	$N \oplus V = 0$
11	BY "LESS THAN ZERO"	BLT	0024	$N \oplus V = 1$
12	BY "GREATER THAN ZERO"	BGT	0030	$Z!(N \oplus V) = 0$
13	BY "LESS THAN OR EQUAL TO ZERO"	BLE	0034	$Z!(N \oplus V) = 1$
14	SIGNLESS BY "GREATER THAN ZERO"	BHI	1010	C!Z = 0
15	SIGNLESS BY "LESS THAN OR EQUAL TO ZERO"	BLOS	1014	C!Z = 1
16	SIGNLESS PY "GREATER THAN OR EQUAL TO ZERO"	BHI	1030	C = 0
17	SIGNLESS BY "LESS THAN ZERO"	BLO	1034	C = 1

is always made when executing this instruction regardless of the state of the conditional code digits.

The second group comprises "simple" conditional carry instructions. This name is related to the fact that the operating algorithm of these instructions depends on "simple" conditions. For example, when executing the BEQ instruction, transfer of control occurs if the digit Z = 1 and when executing the BRL instruction transfer is made if digit N = 0.

The third group contains instructions of sign conditional carries. They are used when working with numbers in the range $-2^{15}-2^{15}-1$ (or -2^7-2^7-1 for operations with bytes). In this case transfer of control depends on a more complex logic function. For example, transfer of control by the BLT instruction is made if the condition $N \oplus V = 1$, where $\oplus$ is the operation "excluding OR," is fulfilled.

The instructions of the fourth group are similar to those of the third group. However, they are used only when working with numbers in the signless range of $0-2^{16}-1$ (or $0-2^8-1$ for operation with bytes).

Let us consider an example to understand the difference between the instructions of the third and fourth groups. Let us assume that the number 177777_8 is located in register R0 and that the number 000001 is located in register R1. In this case, upon execution of the routine fragment

```
CMP  R0,  R1  ; compare the contents of R0 and R1,

BHI  A  ; carry by greater than
```

Transfer of control by address A does not occur since the number 177777 corresponds to -1 in sign representation, which is naturally less than +1.

If BHI instruction is used, the routine fragment is written in the following manner:

```
CMP  R0,  R1 ;  compare the contents of R0 and R1,

BHI A; carry by greater than.
```

In this case transfer of control is made by address A since the number 177777_8 is greater than +1 in signless representation.

Remaining Instructions

The instructions, each of which has its own features and is unrelated to any of the groups described above, are described in this section. Formal description of these instructions is presented in Table 1.10.

The instruction of absolute unconditional carry (JMP) is intended for unconditional transfer of control within the program. The instruction format is similar to that of single-address instructions (see Figure 1.4, a). The control transfer address is determined by the same rules as the address of the operand in single-address instructions. Thus, transfer of control to any memory cell is possible (unlike the BR instruction). It is obvious that mode zero loses meaning upon formation of the address. Therefore, internal interrupt by vector 10 occurs in the given case.

Instructions reversion (JSR) and return from subroutines (RTS). The following main operations must be executed when organizing work with subroutines: transfer of control to the subroutine, storage of the return address in the main routine and return of control to the main routine.

These operations are executed in the following manner in the SM-3 and SM-4 UVK:

a) the control transfer address is formed in the subroutine reversion instruction (JSR) by the same rules as the address of the operand in arithmetic-logic instructions. The same as for the JMP instruction, the use of mode zero in formation of the address is meaningless and causes internal interruption by vector 10. The format of the instruction is similar to that of the supplementary instructions of the SM-4 UVK (see Figure 1.7), but the register does not contain the operand but the return address (see paragraph b);

b) when executing the JSR instruction, the return address, i.e., the current value of the instruction counter, is stored in one of the RON (the programmer selects the register and indicates it in the instruction code), the contents of which are in turn stored in the stack (the contents of the US are first reduced by one-half);

c) when executing the subroutine return instruction (RTS), a procedure inverse to that described above is carried out and namely: the contents of the

Table 1.10. Remaining Instructions

№ of Item	Instructions	Mnemonic Code	Operating Code	Algorithm	Description
1	ABSOLUTE UNCONDITIONAL CARRY	JMP	0001	CK←(prm)	Control is transferred by address of receiver
2	CARRY TO SUBROUTINE	JSR	004	↓(UC)←(R_n) R_n←(CK) CK←(prm)	Control is transferred by address of receiver. The contents of register R_n are recorded in the stack. The return address is recorded in register R_n
3	RETURN FROM SUBROUTINE	RTS	0002	CK←(R_n) R_n←(UC)↑	Control is transferred by address stored in register R_n. The contents of register R_n are restored from the stack.
4	RETURN FROM SUBROUTINE WITH CLEARING OF STACK	MARK	0064	UC←(UC)n + 2 X N CK←(R5) R5←(UC)↑	The stack is reduced by 2 X N, where N is a number recorded in digits 0-5 of the instruction code and output from the subprogram is by register R5
5	CARRY BY COUNTER	SOB	077	R_n←$(R)_n$-1, if result ≠ 0 CK←(CK) + 2 X smshch	Until the result of subtraction is equal to zero, control is transferred by the address determined by the shift, otherwise it is determined by the next instruction
6	CHANGE OF STATE OF PROCESSOR	EMT TRAP IOT BPT	104 1044 000004 000003	↓(UC)←(SSP) ↓(UC←(CK) CK←(N) CCP←(N+2)	Interrupt procedure is executed by vector N. N = 30 (EMT), 34 (TRAP), 20 (IOT) and 14 (BPT)
7	RETURN FROM INTERRUPT	RTI RTT	000002 000006	CK←(UC)↑ CCP←(UC)↑	The values of CK and SSP are restored from stack
8	RESET	RESET	000005	--	INIT signal is formed
9	ANTICIPATION OF INTERRUPT	WAIT	000001	--	All operations stop. Emerging from this condition is only by interrupt
10	STOP	HALT	000000	--	All operations stop. Emergence from this state is only when the key "Continuation" is pressed

selected register are carried to the instruction counter and then its initial contents are carried to this register from the stack. After this the stack index is increased by two, i.e., it is returned to the state in which it was prior to subroutine reversion.

The format of the RTS instruction consists of the field of the operating code (digits 4-15) and the field in which the number of the communications register (digits 0-3) is indicated. The same register should be used in the RTS instruction as in the JSR instruction, by which reversion to the given subroutine is executed.

If register SK is used as the communications register, the return address (the current contents of the SK) will be stored in the stack upon reversion to the subroutine and this address will be restored from the stack upon return from the subroutine by the RTS instruction. The use of other registers simplifies the task of the subroutine independent variables.

The described structure of working with subroutines provides an essentially unlimited depth of embedding of subroutines into each other (it is limited only by the size of the memory zone shifted to the stack), repeated entry of subroutines and convenience of assigning the subroutine independent variables. An example of working with the routines is presented in Table 1.11.

The subroutine independent variables are arranged directly behind the JSR instruction code in the given example. Therefore, the address of the first of the independent variables rather than the return address is stored in register R5. The subroutine should be written in the following manner to use the independent variables (for example, to registers R1 and R2):

```
SUBR: MOV (R5) +, R1
      MOV (R5) +, R2
      PTS  R5
```

Thus, the independent variables are transferred to registers R1 and R2 inside the subroutine while register R5 contains the return address as a result of execution of two instructions in the autoaugmentation mode.

The subroutine return with stack clear instruction (MARK) is realized only in the SM-4 UVK. It permits automatic return of the stack index to the initial state if the independent variable of the subroutine is transmitted through the stack.

Let us consider an example of using the MARK instruction. Reversion to subroutine is written thusly:

```
     MOV R5, -(SP); the contents of R5 are recorded in the stack;
     MOV ARG1, -(SP); N independent variables which should be transferred to the
subroutine are recorded in the stack;
     MOV ARGN, -(SP)
     MOV # MAPKN -(SP); the MARK instruction is recorded in the stack;
     MOV SP, R5; the address of the MARKN instruction is carried to R5;
     JSP PC, SUBR; carry to subroutine.
```

The contents of the stack at this moment have the form:

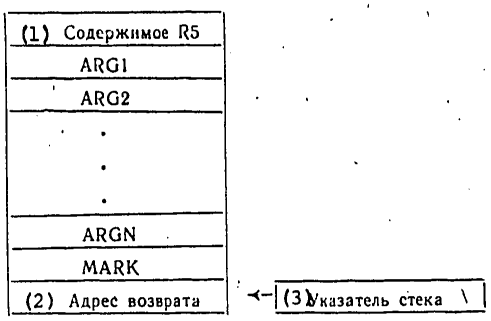
Table 1.11. Example of Working With Subroutines

(1) Мнемоника команды	(2) Код команды	(3) Описание	Содержимое регистров и ячеек памяти (4)	
			(5) до выполнения команды	(6) после выполнения команды
JSR R5, @# SUBR .WORD ARG1, ARG2	004537 —	(7) Управление передается подпрограмме SUBR. Содержимое регистра R5 запоминается в стеке, адрес ячейки, следующей за командой, запоминается в регистре R5	(R5) = 000100 (776) = 000000 (УС) = 001000 (1000) = 012706 (СК) = 002000 (2000) = 004537 (2002) = SUBR (2004) = ARG1 (2006) = ARG2	(R5) = 002004 (776) = 000100 (УС) = 000776 (1000) = 012706 (СК) = SUBR (2000) = 004537 (2002) = SUBR (2004) = ARG1 (2006) = ARG2

Key:

1. Instruction mnemonic code
2. Instruction code
3. Description
4. Contents of registers and memory cells
5. Prior to execution of instruction
6. After execution of instruction
7. Control is transferred to subroutine SUBR. The contents of register R5 are stored in the stack and the address of the cell following the instruction is stored in register R5

Note. SUBR--address of subroutine and ARG1 and ARG2--independent variables of subroutine.



Key:
1. Contents of R5
2. Return address
3. Stack index

Control is transferred to the subroutine SUBR, which should be completed by execution of RTS instruction of R5. The return address is carried to register R5 and the address of the MARKN instruction, which will also be executed in the next step of the routine, is carried to register CK. The stack is reduced by N cells after its execution and then the contents of R5, i.e., the return address, enter CK from R5, while the current cell of the stack in which the old value of register R5 is stored enters R5. Thus, complete exit from the subroutine is accomplished with restoration of the contents of R5 and of the initial value of the stack index.

The processor change of state instructions (EMT, TRAP, IOT and BPT) are actually interrupts which are induced by the programmer himself inside the routine and have their own interrupt vectors. When executing these instructions, a procedure is accomplished similar to that described above for interrupt processing from external devices. The operating code of the EMT and TRAP instructions occupies the top byte of the instruction code.

The lowest bytes of the EMT and TRAP instructions can be used by the programmer to enter any code. Thus, a routine which will analyze the lowest byte of the instruction and which will transfer control to one of 256 possible subroutines can be entered in the cell to which control is transferred upon execution of the instruction.

Compared to the JSR instruction, the EMT and TRAP instructions have the following advantages: they always occupy one cell of the OZU while the JSR instruction usually occupies two cells. Using these instructions, the programmer can establish the word of state (the priority of the processor is especially important in this case) which is required when executing the subroutine. This capability may be significant when writing real-time routines.

However, a disadvantage of these instructions is the significantly greater time of execution.

Note. The EMT instruction is used extensively in standard software systems. Therefore, use of it in user routines is not recommended since correct execution of systems routines is not guaranteed.

The values of the lowest bytes are not given in the IOT and BPT instructions; therefore, they are used for access to a single subroutine. Like the EMT instruction, they are reserved for systems use.

The interrupt return instructions (RTI and RTT) accomplish a procedure opposite with respect to that which was described above for interrupt processing. Therefore, the interrupt processing subroutines induced by external devices and internal factors and also the subroutines, control to which is transferred after execution of EMP, TRAP, IOT and BPT instructions, should be terminated with these instructions.

The difference between RTI and RTT instructions includes the following: RTT prohibits interrupt through the following digit of the SSP. This interrupt can be realized only after execution of the first instruction following the RTT and upon execution of the RTI instruction this interrupt is possible immediately after completion of execution of the RTI instruction. The format of the RTI and RTT instructions consists only of the field of the operating code.

Note. The RTT instruction is used only in SM-4 UVK. The RTI instruction is executed in the SM-3 UVK the same as the RTT instruction in the SM-4 UVK.

The counter carry instruction (SOB) is realized only in the SM-4 UVK. It is convenient for organization of cycles. When it is executed, the contents of one of the registers R0-R5 (the programmer selects the register) is reduced by one. If the value of the register is not equal to zero, control is transferred by the address which is determined by the value of shift in the six lowest digits of the instruction. If the value of the register is equal to zero, then control is transferred to the next instruction. Thus, to organize the cycle, the programmer has only to enter the number of repetitions of the cycle in the register and to place the SOB instruction at the end of the cycle.

Note. The SOB instruction is used to transfer control only with a reduction of the addresses, i.e., the shift is always subtracted from the instruction counter.

The conditional code set-reset instructions have the format shown in Figure 1.8. Digit 4 indicates that the following should be executed by the instruction: setting (one) or reset (zero) of the conditional code. The digits 0-3 indicate which of the digits of the word of state should be set to one or reset (ones are written in the corresponding instruction digits and zeroes are written in the digits for which no action is necessary).

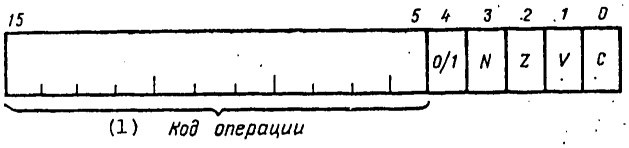


Figure 1.8. Format of Conditional Code Set-Reset Instructions

Key:
1. Operating code

The mnemonic notations of these instructions are presented in Table 1.12.

Table 1.12.

(1) Мнемоника команды	(2) Операция	(3) Код операции
CLC	Сброс C (4)	000241
CLV	Сброс V (5)	000242
CLZ	Сброс Z (6)	000244
CLN	Сброс N (7)	000250
SEC	Установка единицы в C (8)	000261
SEV	Установка единицы в V (9)	000262
SEZ	Установка единицы в Z (10)	000264
SEN	Установка единицы в N (11)	000270
—	Сброс всех разрядов кода условий (12)	000257
—	Установка единицы во все разряды кода условий (13)	000277
—	Нуль-операция (14)	000240, 000260

Key:

1. Instruction mnemonic code
2. Operation
3. Operating code
4. Reset C
5. Reset V
6. Reset Z
7. Reset N
8. Setting of one in C
9. Setting of one in V
10. Setting of one in Z
11. Setting of one in N
12. Reset of all digits of conditional code
13. Setting of one in all digits of conditional code
14. Zero operation

The RESET (RESET) instruction. When executing this instruction, a common reset signal is formed on the INIT line of the "Common bus" interface which can be used to set the VU to the initial state. This signal is completely similar to that which was generated when the "Start" key on the processor console was pressed.

The INTERRUPT anticipation (WAIT) instruction stops execution of all operations by the processor. A way out of this state is possible only upon interrupt from the VU. The address of the instruction following WAIT is stored in the stack upon interrupt and execution of the main routine is restored after completion of work of the interrupt processing routine. Since the processor has no access to the "Common bus" interface during execution of the WAIT instruction, the interrupt from the VU is serviced at maximum speed. The STOP (HALT) instruction also stops execution of all operations by the processor. Interrupts from the VU are prohibited. The "Continuation" key on the processor console is pressed to get out of this state.

1.5. Characteristics of Organizing Work With Memory in the SM-4 UVK

The Stack Limiter

One of the configurational characteristics of the SM-3 and SM-4 UVK is the apparatus capabilities of organizing the stack memory. The programmer usually sets the stack index to the beginning of its routine. The lower bound of the stack constantly changes value and may be below the permissible value during access to subroutines, during interrupt processing and when using the stack by the programmer

himself for temporary storage of information since the lowest addresses of the memory in the developed programming systems have been shifted to the interrupt vectors. Therefore, equipment security of the interrupt vector zone is provided in the SM-3 and SM-4 UVK. If the value of the stack index (R6) is equal to or less than 400, internal interrupt by vector 4 occurs.

If the stack must be arranged in an arbitrary memory zone rather than in the initial zone, distribution of the stack to another memory zone in which the routines are located is possible. The apparatus stack limiter, which sets the lower bound of the stack by the routine, permits one to avoid this in the SM-4 UVK. An internal interrupt occurs if this boundary is violated.

The lower stack boundary can vary with discreteness of 200_8 words and the information about it is recorded in a special register of the stack limiter. Access to this register can be gained from the routine by the address 777774.

Digits 8-15 of this register contain information about the stack boundary. These digits are dropped by pressing the "start" key on the processor console or by the RESET instruction. The eight lowest digits are not used.

If access by the stack address, which exceeds (becomes less than) the boundary set in the register of the stack limiter (OS), is executed in the instructions, the violation of the stack boundary is recorded. A so-called "yellow" zone of 16 words located below the stack boundary exists. Violation of it is recorded upon access to this zone. In this case all operations in this zone are prohibited and interrupt of the routine by vector 4 is then induced. This interrupt in itself uses the stack, automatically leading to a second violation of the boundary, but it is executed without recording of the additional violation if only the stack address did not indicate the "red" zone.

Violation of the "red" zone is prohibited during access to the stack (an odd stack address or nonexistent address are other uncorrectable stack errors). The operation which induced this violation is rejected and interrupt is executed by vector 4.

The contents of the stack limiter register are compared to the stack address to determine violation of the stack boundary.

The "red" and "yellow" zones are determined in the following manner: the "red" zone $\leq$ (OS) + $(337)_8$ and the "yellow" zone = (OS) + (from 340 to $377)_8$.

If the contents of the stack limiter register are equal to zero, the "yellow" zone occupies cells with addresses from 340 to 377, while the "red" zone occupies cells from 000 to 377.

The Memory Dispatcher

Another piece of equipment of the SM-4 UVK is the memory dispatcher, which is used to increase the volume of OZU up to 124K words. The 16-digit format of the word does not permit addressing of the memory with volume greater than 32K words. Therefore, expansion of the memory is intended mainly for internal storage and to execute several tasks, each of which occupies no more than 32K words, rather than for storage and execution of a single task with volume greater than 32K words

(although this capability exists). The control routine which distributes the memory among tasks and which performs dispatcher functions upon transfer of control of one or another task is required to perform several tasks. Therefore, two operating modes--user and systems--are provided in the SM-4 UVK. The mode in which the processor is at a current moment is determined by digits 14 and 15 of the SSP. When the mode changes, it may become necessary to exchange information between the current routine and that which was executed prior to the change of mode. This exchange can be accomplished through the stack memory zone. There are two stack equipment indexes in the SM-4 UVK. One of them operates in the systems mode and the other operates in the user mode. Moreover, the index is denoted by R6 both in the systems routine and in all user routines. One of the indexes is selected during execution of the routine as a function of the current mode. Thus, two stack zones--systems and one of the user zones--exist simultaneously. The stack limiter can be used to prevent intersection of these zones. Special instructions: TRANSMISSION FROM MEMORY ZONE OF PREVIOUS MODE (MFPI) and TRANSMISSION TO MEMORY ZONE OF PREVIOUS MODE (MTPI) are used to exchange information between these zones.

The principle of memory expansion includes addition of the value of the address formed by the instruction to a specific 18-digit shift. The extent of the shift varies upon transition to another problem. Thus, several routines encoded in the same addresses may be located in the memory simultaneously. Any 16-digit address coming from the processor is first entered in the memory dispatcher, where it is converted to the actual 18-digit address of the OZU which prints it out to the address lines of the "Common bus" interface. Let us subsequently call the addresses formed by the processor instructions virtual addresses and the addresses issued by the memory dispatcher to the address lines of the "Common bus" interface physical addresses.

A virtual address is converted to a physical address in the following manner. The three highest digits 13-15 of the virtual address are interpreted as the number of one of eight shift registers. The contents of digits 6-12 of the virtual address are added to the contents of digits 0-11 of the selected shift mode. The derived 12-digit sum and the remaining six digits of the virtual address (0-5) form the physical address. The entire field of virtual addresses is divided into eight pages, each of which can be arranged at any point of the memory.

Formation of the physical address is illustrated by Figure 1.9. The shift register contains the 12-digit field of the page address. However, this field can be regarded as an 18-digit field in which the lowest six digits are equal to zero. Thus, one can control the position of the page in the memory with discreteness of 32 words. This file of 32 words is called a block. Therefore, digits 6-12 of the virtual address may be regarded as a number while digits 0-5 may be regarded as a shift inside the block. The sum of the contents of the selected shift register and of digits 6-12 of the virtual address forms the number of the physical block.

A page description register, which contains information about the method of access to the page, length of the page and the indicator of recording to the page, corresponds to each shift register of the page.

The accessibility of the page is provided by corresponding setting of a two-digit code in the page description register. The page may be accessible for recording and readout, only for readout and completely inaccessible for both recording and

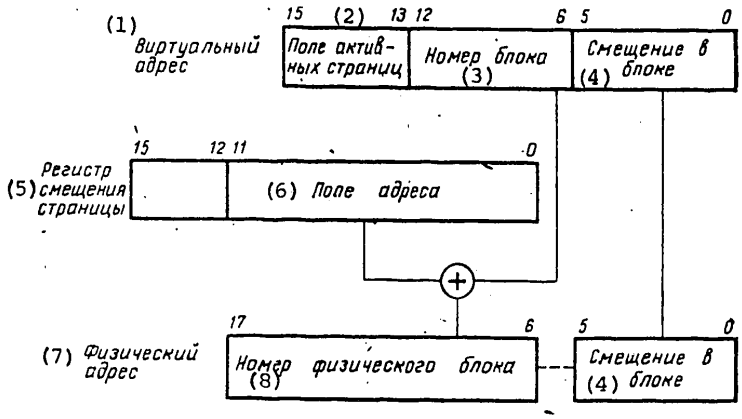


Figure 1.9. Diagram of Formation of Physical Address

Key:

1. Virtual address
2. Field of active pages
3. Number of block
4. Shift in block
5. Register of page shift
6. Address field
7. Physical address
8. Number of physical block

readout. The latter means that the address field corresponding to this page cannot be used in problem solving. This permits the memory to be protected against the influence of one task on others. For example, if a storage capability equal to 20K words is allocated for the task, the access code which prohibits access to these pages will be set in the description registers of the sixth, seventh and eighth pages. If the task forms access to one of these pages through error of the programmer or due to the effect of external factors (in real object control tasks), this access is not executed and internal interrupt occurs.

If the system contains information which immediately uses several problems, a page (or part of it) is allocated to each problem in the address field, upon access to which the problem achieves access to the required information. Since this information may be required after completion of work of the given problem and transition to the next problem, an access code corresponding to the mode in which only readout is possible is set in the page description register.

The length of the page (in the blocks) is determined in the description register if a memory whose capacity is not a multiple of 4K is allocated for problem solving. The length of the page varies from 1 to 128 blocks, i.e., from 32 words to 4K words.

The page description register also contains the page recording indicator. The page recording indicator permits a saving of the time which may be expended on re-recording to the external memory of unmodified memory zones (from the time of their last callup to the internal storage) required for other purposes. This zone can be used immediately and the routine is not spoiled in this case since an exact copy of it is still available in the external memory. If at least one recording to the given page is made during problem solving, the indicator is set to one.

Still another set of shift and page description registers is provided for working in the systems mode in the memory dispatcher. The memory dispatcher selects the required set of registers as a function of the code set in digits 14 and 15 of the SSP. Thus, a systems routine may also be divided into pages and arranged in any point of the memory.

The routine operating in the systems mode can utilize all capabilities of the system. There are certain restrictions when working in the user mode. Use of one of the user routines which may affect the state of other routines is prohibited. The user routine cannot execute some instructions (for example, HALT and RESET). If one of the impermissible instructions is encountered in the user routine, this instruction is not executed and internal interrupt occurs. Moreover, it cannot perform input-output operations, which is provided in the following manner. Access to the VU is accomplished by addresses 160000-177776 (the highest 4K of the addressable field) with the memory dispatcher switched off in the SM-3 and SM-4 UVK. Actually, the VU have addresses in the range of 760000-7677776. Therefore, upon access to the lowest addresses, the processor automatically displays ones on the two lowest address lines of the "Common bus" interface. If the memory dispatcher is switched on in the SM-4 UVK, the state of these lines depends on the page shift registers. A value equal to 760000 is usually set in the eighth systems shift register. Thus, the systems routine permits access to the VU.

Upon transition to the user task, the user set of shift registers is filled by the values which were determined during distribution of the memory for this task. If the total possible storage capacity (32K words) is not allocated for solution of this problem, access to the virtual addresses is usually not possible in the range of 160000-177776. If the complete storage capacity is allocated for solution of the problem, the eighth shift register is loaded with a value which physicallv corresponds to the beginning of some memory zone rather than to the beginning of the VU registers.

[Excerpts] Characteristics of the line groups. The level of the logic one in the active state on the lines of the first RP [Transfer authorization] [7:4] and RPD [Direct access authorization] group corresponds to high voltage (+3, 4V), while they themselves are at a low level ($\leq$ 8V) in the passive state, which corresponds to a logic zero.

The signals of the lines of the first group also terminate on the ends of the matching resistor dividers (see Figure 2.12, b). The resistor parameters are the same as those of the lines of the third group.

A schematic diagram of realizing the lines of the third group of the OSh [Common bus] is shown in Figure 2.12, a.

The parameters of the matching resistors are the following: R_1 = 150 ohms $\pm$ 2 percent and R_2 = 300 ohms $\pm$ 2 percent. The output of the resistors is 0.25 watts each.

The lines of the second group have one each matching resistor of 300 ohms $\pm$ 2 percent (0.25 W) on the ends, connected in parallel to a 0.001 µF capacitor to voltage of +5 V.

The ASP [Power supply emergency] (ACLO) and AIP [Power source emergency] (DCLO) signals should maintain the corresponding lines at the low level ($\leq$ + 0.8 V) even if the voltage in the device signalling the loss of power supply completely disappears.

The presence of matching dividers on the resistors on both ends and a certain number of load units (up to 20 pairs of IST [Source] and PRM [Receiver]), distributed along these lines, is typical for the lines of the third group (see Table 2.4). Arrangement of the PST and PRM along the lines can be arbitrary (cluster, uniform or mixed), determined by the configuration of the system. The outer IST and PRM can be arranged behind the matching divider on resistors at a distance of not more than 60 cm. If the divider is located at the end of the line, no special requirements are placed on the minimum distance between the matching divider and the IST or PRM. The length of the lead connecting the IST or PRM to the bus line and executed by printed circuit or a twisted pair should not exceed 60 cm. In this case the total capacitance which shunts the line should not exceed 30 pF.

All the matching resistors (with the exception of the resistors of group 1) are structurally assembled on a printed circuit card, called a common bus choke (ZOSh). The ZOSh dividers are powered from the sources of the devices in which they are installed.

The RP and RPD lines of group 1 do not always pass from one physical end of the OSh to the other (the source is the processor arbitrator). Any of the lines of this group can be interrupted in each device located at a given level of priority on the OSh and propagation of an RP or RPD signal along it may proceed further if the given device is not a request source. Since the signals on the RP and RPD lines are relayed in devices having their own power supply sources of +5 V, variation of the voltage of +5 V (within permissible limits) on the ZOSh resistors in no way affects the state of the equilibrium levels on these lines.

To measure the equilibrium level of the voltage or to follow the shape or front of the pulse on the RP and RPD lines, a check must be made at the specific points of interest of the OSh directly on the devices.

Interface amplifiers specially designed for mainline transmission (sources--IST) and reception (receivers--PRM) of information are used to connect the devices to the "Common bus" lines. IS [Integrated circuits] of series K559: K559 IP1--four mainline transmitters, K559 IP2--four mainline receivers and K559 IP3--four receivers and four transmitters with common control, are used as the interface amplifiers in devices of the SM3 and SM4 UVK.

Integrated circuits with electrical and time parameters presented in Table 2.5 are used as the standard signal receivers from the "Common bus" which meet common requirements.

Integrated circuits with electrical and time parameters no worse than those given in Table 2.6 are used as standard sources which meet the requirements of signal transfer through the "Common bus."

The total value of the maximum output current of the logic one for the source (I^1_{vykh} = 120 μA) and the maximum input current of the logic one for the receiver (I^1_{vkh} = 200 μA) connected to a line equal to 320 μA with capacitive load not exceeding 30 pF is taken as the load unit for direct current for a "Common bus" line.

Table 2.5. Main Parameters of Standard Receivers

Number of Item	Parameter	Maximum Value of Parameter	Remarks
1	Input threshold voltage for switching from high level (logic 1) to low level (logic 0) $U^{1.0}_{por}$, V	No more than 2.5	Corresponds to maximum (lower) value of logic one
2	Input threshold voltage for switching from low level to high level $U^{1.0}_{por}$, V	Not less than 1.4	Corresponds to upper value of logic zero
3	Input current of logic one I^{1}_{vkh}, μA	Not more than 200	With input voltage of 2.4 V
4	Input current of logic zero I^{0}_{vkh}, μA	Not more than -10	Inflowing current (-) at input voltage of 0 V
5	Output voltage of logic one U^{1}_{vykh}, V	Not less than 2.5	
6	Output voltage of logic zero U^{0}_{vykh}, V	Not more than 0.5	
7	Output current of logic one I^{1}_{vykh}, mA	Not less than 0.4	
8	Output current of logic zero I^{0}_{vykh}, mA	Not less than 8.0	
9	Propagation delay time upon switching on of $t^{1.0}_{zd.r}$, NS	Not more than 30	
10	Propagation delay time upon switching off of $t^{0.1}_{zd.r}$, NS	Not more than 30	

Table 2.6. Main Parameters of Standard Sources

Number of Item	Parameter	Maximum Value of Parameter	Remarks
1	Input voltage of logic one U^{1}_{vkh}, V	Not less than 2.0	
2	Input voltage of logic zero U^{0}_{vkh}, V	Not more than 0.8	
3	Input current of logic one I^{1}_{vkh}, μA	Not more than 100	
4	Input current of logic zero I^{0}_{vkh}, mA	Not more than -4.0	Inflowing current (-)
5	Output voltage of logic one U^{1}_{vykh}, V	Not less than 3.5	
6	Output voltage of logic zero U^{0}_{vykh}, V	Not more than 0.8	With output current of 70 mA
7	Output current of logic one I^{1}_{vykh}, μA	Not more than 120	With voltage of 3.4 V at output; leakage current
8	Output current of logic zero I^{0}_{vykh}, mA	Not less than 70	
9	Propagation delay time upon switching on $t^{1.0}_{zd.r}$, NS	Not more than 30	
10	Propagation delay time upon switching off $t^{0.1}_{zd.r}$, NS		

Note. The output stage of the OSh source should be organized by the type of component with open collector

A diagram of the load unit is shown in Figure 2.13.

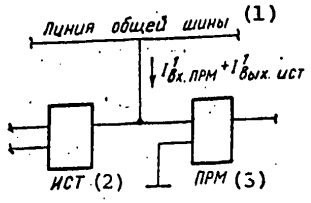


Figure 2.13. Diagram of Load Unit on OSh

Key:
1. Common bus line
2. Source
3. Receiver

Requirements on the main cable. The communications mainline which connects the devices to the system consists of a combination of series-connected segments of flat multiconductor cable and groups of wiring joints directly on the general wiring panels of the blocks and devices.

The cable has printed circuit pieces on the ends designed for installation in a standard interface disconnect and connects the contacts of the pieces of the same type.

Cable of different length--0.6, 1.0, 1.5, 2.5, 3.3, 5.0 and 8.3 meters--is used as a function of the location of the devices.

When additional devices are connected, one should take into account that the total length of the main communications line should not exceed 15.0 meters (without using interface expander devices).

Flat cable which meets the following requirements is suitable for realization of the "Common bus": wave impedance should be 100 $\pm$ 20/10 ohms, the signal propagation delay time should not be more than 5.2 ns per meter and electric resistivity of each signal and shielding (ground) conductor should not be more than 0.4 ohms per meter.

The signal conductors should alternate in the cable with the ground conductors to shield the signal conductors against crosstalk.

The interface disconnect. A two-row disconnect of the "Socket 03.094.01.30.21" type (TU-77/801-805/265) is used to install the printed circuit pieces of the "Common bus" cable in SM-3 and SM-4 complexes. The Unitra-Eltra Company of the Polish Peoples Republic is the manufacturer. The designation of the disconnect contacts in application to the "Common bus" is presented in Table 2.7.

The maximum permissible cable length (for all transmission lines) with regard to the permissible length of the leads from the lines to the source and receiver has been established at 15.0 meters. This length was selected with regard to the parameters of the main amplifiers and realization of the main line by an exceptionally flat cable with parameters indicated above.

Table 2.7. Structure of "Common Bus" Disconnect

Обозначение сигнала (1)		Номер контакта на стороне разъема (4)		Обозначение сигнала	
на русском языке (2)	на английском языке (3)	a/100	b/200	на русском языке	на английском языке
1	2	3	4	5	6
ПИТАНИЕ+5В (5)	POWER+5B	1	1	ПИТАНИЕ+5В	POWER+5B
РЕЗЕРВ (Р)(6)	RESERVE (R)	2	2	РЕЗЕРВ (Р)	RESERVE (R)
ЗЕМЛЯ (7)	GROUND	3	3	ЗЕМЛЯ	GROUND
—ОШ ПРЕР (8)	BUSINTR L	4	4	—ОШ ПОД(20)	BUS INIT L
ЗЕМЛЯ (7)	GROUND	5	5	ЗЕМЛЯ	GROUND
—ОШ Д00 (9)	BUS D00L	6	6	—ОШ Д01 (9)	BUS D01 L
—ОШ Д02	BUS D002 L	7	7	—ОШ Д03	BUS D03 L
—ОШ Д04	BUS D04 L	8	8	—ОШ Д05	BUS D05 L
—ОШ Д06	BUS D06 L	9	9	—ОШ Д07	BUS D07 L
ЗЕМЛЯ (7)	GROUND	10	10	ЗЕМЛЯ	GROUND
—ОШ Д08	BUS D08 L	11	11	—ОШ Д09	BUS D09 L
—ОШ Д10	BUS D10 L	12	12	—ОШ Д11	BUS D11L
—ОШ Д12	BUS D12 L	13	13	—ОШ Д13	BUS D13 L
—ОШ Д14	BUS D14 L	14	14	—ОШ Д15	BUS D15 L
ЗЕМЛЯ	GROUND	15	15	ЗЕМЛЯ	GROUND
—ОШ КО(10)	BUS PAL	16	16	—ОШ К1(21)	BUS PBL
—ОШ ПВВ(11)	BUS SACKL	17	17	—ОШ ЗАН(22)	RUS BBSYL
ЗЕМЛЯ	GROUND	18	18	ЗЕМЛЯ	GROUND
ОШ РПД (12)	BUS NPG(IN)H	19	19	ОШ РПД(12)	BUS NPG(OUT)H
—ОШ ЗПД(13)	BUS NPRL	20	20	РЕЗЕРВ (Р)	RESERVE (R)
ОШ РП7 (14)	BUS BG7(IN)H	21	21	ОШ РП7(14)	BUS BG7(OUT)H
РЕЗЕРВ (Р) (6)	RESERVE (R)	22	22	—ОШ ЗП7(15)	BUS BR7 L
ОШ РП6	BUS BG6(IN)H	23	23	ОШ РП6	BUS BG6(OUT)H
—ОШ ЗП6(15)	BUS BR6 L	24	24	РЕЗЕРВ (Р)	RESERVE (R)
ОШ РП5	BUS BG5(IN)H	25	25	ОШ РП5	BUS BG5(OUT)H
РЕЗЕРВ (Р)	RESERVE(R)	26	26	—ОШ ЗП5	BUS BR5L
ОШ РП4	BUSBG4(IN)H	27	27	ОШ РП4	BUS BG4(OVT)H
—ОШ ЗП4	BUS BR4 L	28	28	РЕЗЕРВ (Р)	RESERVE (R)
—ОШ АСП (16)	BUS ACLO L	29	29	—ОШ АИП (23)	BUS DCLOL
—ОШ А00 (17)	BUS A00 L	31	31	—ОШ А01	BUS A01 L
—ОШ А02	BUS A02 L	32	32	—ОШ А03	BUS A03 L
—ОШ А04	BUS A04 L	33	33	—ОШ А05	BUS A05 L
—ОШ А06	BUS A06 L	34	34	—ОШ А07	BUS A07 L
—ОШ А08	BUS A08 L	35	35	—ОШ А09	BUS A09 L
—ОШ А10	BUS A10 L	36	36	—ОШ А11	BUS A11 L
—ОШ А12	BVUS A12 L	37	37	—ОШ А13	BUS A13 L
—ОШ А14	BUS A14 L	38	38	—ОШ А15	BUS A15 L
—ОШ А16	BUS A16 L	39	39	—ОШ А17	BUS A17 L
РЕЗЕРВ (Р)	RESERVE(R)	40	40	РЕЗЕРВ (Р)	RESERVE (R)
РЕЗЕРВ (Р)	RESERVE(R)	41	41	РЕЗЕРВ (Р)	RESERVE (R)
РЕЗЕРВ (Р)	RESERVE(R)	42	42	РЕЗЕРВ (Р)	RESERVE (R)
—ОШ У0 (18)	BUS C0L	43	43	—ОШ У1 (24)	BUS C1 L
ЗЕМЛЯ	GROUND	44	44	ЗЕМЛЯ	GROUND
—ОШ СХЗ(19)	BUSMSYNL	45	45	—ОШ СХИ(25)	BUS SSYNL
ЗЕМЛЯ	GROUND	46	46	ЗЕМЛЯ	GROUND
РЕЗЕРВ (Р)(5)	RESERVE(R)	47	47	РЕЗЕРВ (Р)	RESERVE (R)
ПИТАНИЕ +5В	POWER+5B	48	48	ПИТАНИЕ+5В	POWER+5B

Note. The Latin letters "a" and "b" denote the series of contacts on the socket, while the numbers "100" and "200" denote the corresponding sides of the printed circuit pieces of the bus cables or interface cards installed in these sockets.

Key:

1. Notation of signal
2. In Russian language
3. In English language
4. Number of contact on side of disconnect

[Key continued on following page]

[Key continued from preceding page]

5. Power + 5V
6. Reserve (R)
7. Ground
8. Common bus interrupt
9. Common bus D
10. Operating code bus
11. Selection confirmation bus
12. Direct access authorization bus
13. Direct access request bus
14. Transfer authorization bus
15. Transfer request bus
16. Power system emergency bus
17. Common bus A
18. Control bus O
19. Dispatcher synchronization bus
20. Preparation bus
21. Checking bus K1
22. Engaged bus
23. Power source emergency bus
24. Operation control bus
25. Executor synchronization bus

The load capacity of the bus is limited to a maximum of 20 load units. This limit was established on the basis of the condition for providing an adequate noise reserve at the given source and receiver parameters.

Means of expanding the interface capabilities. It is recommended that a special device--a signal relay (one or several), called an interface expander OSh SM EVM (RIF SM)--be used when it is required to transmit signals over interface lines by a distance exceeding the maximum permissible length of 15.0 meters or to increase the load units above 20. Each of these devices loads the main segment of the bus with a single load unit, but provides the capability of additional connection of up to 19 load units and a length up to 15.0 meters. The RIF SM can be used every 15.0 meters or less. It divides the entire main communications line of the complex into a number of independent segments (sections) with identical capabilities. The use of an expander circuit does not affect the operating algorithm of the interface, but introduces an additional delay (not more than 350 nanoseconds per RIF) during propagation of signals over series-connected segments of the bus.

Each additional section of the bus should begin and end with matching dividers on the resisters (located on the ZOSh), the equivalent resistance of which is equal to the wave impedance of the interface cable.

Chapter 5.

DESIGN OF CONTROL COMPUTER COMPLEXES

5.1. Classification of Complexes

SM-3 and SM-4 complexes are hardware complexes (KTS) of the SM EVM with "Common bus" interface, the configuration and software of which are determined by SM-3P and SM-4P processors. These complexes are program-compatible "from bottom to top" and have a unified nomenclature of external devices. SM-3 and SM-4 complexes are conditionally divided into basic, specific, standard and problem-oriented as a function of the makeup, consideration of user requirements and so on.

Basic complexes are hardware and standard software complexes of specific composition (fixed, determined by specifications) designed for use as the computer nucleus

Table 4.1. Main Characteristics of Operating Systems of SM-3 and SM-4 UVK

(1) Характеристики операционной системы	(2) Операционные системы общего назначения			(3) Операционные системы реального времени				Операционные системы (4) разделения времени	
	(5) ДС СМ	(6) ПЛОС СМ	(7) ДОС СМ	(8) ПЛОС РВ	(9) ФОБОС	(10) ДОС РВ	(11) ОС РВ	(12) ДИАМС	(13) ДОС РВР
1	2	3	4	5	6	7	8	9	10
Тип УВК (14)	(15) СМ-3, СМ-4 (16)	СМ-3, СМ-4	СМ-3, СМ-4	СМ-3, СМ-4	СМ-3, СМ-4	СМ-3, СМ-4	СМ-3, СМ-4	СМ-3*, СМ-4	СМ-4
Носитель системы (17)	ПЛ (18)	ПЛ	МД (19)	ПЛ	МД	МД	МД	МД	МД
Минимальный объем оперативной (20) памяти, К слов	8	8	16	12	16	16	16	16	40
Максимальный объем оперативной (21) памяти, К слов	28	28	28	28	28	28	124	124	124
Возможность обслуживания (22)	(23) Однопользовательская	Однопользовательская	(24) Многопользовательская	Однопользовательская	Однопользовательская	Многопользовательская	Многопользовательская	Многопользовательская	Многопользовательская
Наличие (25) мультипрограммной работы	Нет (26)	Нет	Нет	Есть (27)	Есть	Есть	Есть	Есть	Есть
Число одновременно выполняемых программ (28)	—	—	—	127+(29) +1 фоновая	(30) 1 оперативная+ +1 фоновая	127+ +1 фоновая	250, (31) уровней приоритета	40	24
Наличие (32) средств телеобработки	Нет (26)	Нет	Нет	Есть (27)	Нет	Есть	Есть	Есть	Есть
Число (33) подключаемых терминалов	—	—	—	8	—	8	32	64	24
Языки (34) программирования	(35) Диалоговый язык ДС	(36) Ассемблер	(37) Макроассемблер, Фортран-IV	Ассемблер	Макроассемблер, Фортран-IV	Ассемблер	Макроассемблер, Фортран-IV	(38) Диалоговый язык ДИАМС	(39) Бэйсик-плюс

*Only with the presence of an arithmetic expander in the SM-3

Key:

1. Characteristics of operating system
2. General-purpose operating systems
3. Real-time operating systems
4. Time-sharing operating systems
5. Dialogue programming system
6. Paper tape operating system
7. Disk operating system
8. Real-time paper tape operating system
9. Real-time basic background-operating system

[Key continued on following page]

[Key continued from preceding page]

10. Real-time disk operating system
11. Real-time operating system
12. Multiterminal time-sharing dialogue operating system
13. Time-sharing disk operating system
14. Type of UVK
15. SM-3
16. SM-4
17. System carrier
18. Punch tape
19. Magnetic disc
20. Minimum internal storage capacity, K words
21. Maximum internal storage capacity, K words
22. Servicing capability
23. Single-user
24. Multiuser
25. Presence of multipgroram
26. No
27. Yes
28. Number of simultaneously executed routines
29. 127 + 1 background
30. 1 operational + 1 background
31. 250 priority levels
32. Presence of remote processing facilities
33. Number of connected terminals
34. Programming languages
35. Dialogue language of dialogue system
36. Assembler
37. Macroassembler and Fortran-IV
38. DIAMS dialogue language
39. Basic-plus

in design of information, measuring, control and computer complexes of different composition and designation.

Specific complexes are general-purpose complexes whose composition is determined by the customer's specifics according to the coordinated technical assignment. The composition of the delivered equipment usually includes a basic or standard complex supplemented by the necessary equipment from the KTS nomenclature of the SM EVM (devices, blocks and modules). A specified complex is supplied with standard software and minimum general systems documentation developed by the manufacturing plant or user with the consultative assistance of the manufacturing plant. The complex has no delivery specifications and therefore the manufacturing plant (supplier) conducts no additional tests of the specified complex in assembled form. All individual devices and units are checked for conformity to specifications at the manufacturing plants; the given operating system is generated to the corresponding configuration of the complex by the supplier.

All the specifications included in the specified complex (additional devices, structural components, cables and so on) are nomenclature articles with a confirmed price. The selling price of a specified complex is determined by agreement for delivery by the total prices of the constituent parts.

Standard complexes (standard specified complexes--TSK) occupy an intermediate position between the basic and specified complexes. Documentation for them is worked out by the head organization for computer technology and the manufacturer to simplify ordering and development of specified complexes by customer orders. The functional capabilities of TSK are considerably wider than those of basic complexes and it is simpler to construct specified complexes for specific applications on their basis.

A typical specified complex, in addition to the selected basic complex, includes devices, modules, dispatchers and bays. For example, interface matching modules for connection of communications devices with the object are from SM-1 and SM-2 nomenclature (USS OSh/2K) or for communications with machines of series YeS EVM (USVM), USO bays with variants of sets of modules for design of control complexes, common bus switch (PSh) devices, interprocessor communications adapters (AMS) for creation of multiprocessor complexes and complexes with variable structure for systems of enhanced viability and productivity, remote communications adapters (BS ADS) for remote processing complexes and so on.

TSK are divided into standard specified computer complexes (TS VK), standard specified control computer complexes (TS UVK), standard specified nonprocessor complexes or standard subcomplexes (parts of complexes) and standard bays (TSS) as a function of the composition of the hardware and standard software. The main characteristics of standard specified complexes are presented in Table 5.1.

Different configurations of standard specified complexes based on the SM-3 and SM-4 are illustrated by Figures 5.1-5.3: remote processing TS VK with four remote terminals which includes two magnetic tape stores and two magnetic disk stores (Figure 5.1), TS UVK which utilizes object communications devices with 2K interface connected through USS OSh/2K communications-matching devices (Figure 5.2) and TS UVK which utilizes object communications devices (UVA and UVD) with OSh interface (Figure 5.3).

Problem-oriented complexes of the SM EVM (POK SM EVM) are sets of hardware, software, methodical, planning and organizing solutions on realization of a given set of problems of automation of a specific class of objects combined by a common information processing technology and unanimity of information processing modes and operating conditions.

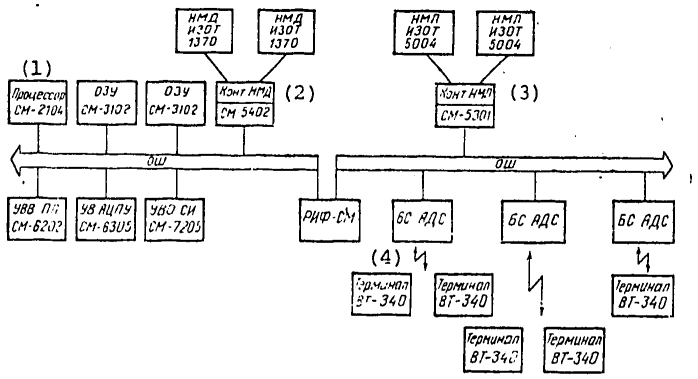


Figure 5.1. Standard Specified Multiterminal Complex of SM-4

Key:
1. Processor
2. NMD monitor
3. NML monitor
4. Terminal

Table 5.1.

(1) Условное обозначение комплекса	(2) Основное назначение	(3) Тип носителя для генерации программных средств			(4) Основная характеристика								
		(5) ПЛ	(6) МД	(7) МЛ	(8) пакетная обработка	(9) обработка в режиме реального времени	(10) обработка в режиме реального времени, высокореактивная	(11) обработка в режиме разделения времени	(12) телеобработка данных	(13) ведение баз данных	(14) диалоговый режим	(15) обработка графической информации	(16) однозадачный режим
1	2	3	4	5	6	7	8	9	10	11	12	13	14
(36) СМ-3-01	Базовый (37) дисковый общего назначения (вариантный)	+	+		+	×					+		+
СМ-3-01.01			+		+		×						
СМ-3-01.02			+		+		×						
СМ-3-02	Базовый (38) дисковый минимального состава	+	+		+	×					+		+
СМ-3-03	Базовый минимального состава (39)	+				×					+		+
СМ-3-04	Базовый (40)	+									+		+
СМ-3-05.01	ТСК с МЛ (кассетный, минимальный состав) (41)	+			+	×	×				+		+
СМ-3-05.02	»	+			+	×	×				+		+
СМ-3-06	ТСК с гибкими МД (вариантный) (42)	×			+								
СМ-3-06.01		+			+	×	+				+		+
СМ-3-06.02					+		+				+		
СМ-3-06-03		+			+	×	+				+		+
СМ-3-07	ТСК расширенный общего назначения (вариантный) (43)				+		×						
СМ-3-07.01		×	+	+	+	+	×			+	+		
СМ-3 07.02		×	+	+	+	+	×			+	+		

[Table continued on following page]

Table 5.1. [Continued from preceding page]

обработки информации						Операционная система (24)									(35) Примечание
(17) двухзадачный режим	(18) многозадачный режим	(19) многотерминальная обработка	(20) режим повышенной надежности: (21) резервирование процессора	(22) резервирование внешних устройств	(23) многомашинная обработка	(25) ПЛОС, ДС СМ	(26) ПЛОС РВ	(27) ДОС	(28) ДОС РВ	(29) ФОБОС	(30) ОС РВ	(31) ДИАМС	(32) ДОС РВР	(33) ДОС+СТОД	(34) ДОС АРМ
15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	+					+	×	+	×	×						28К слов, ПЛ, НМД (2,4 Мбайт) (44)
																Две стойки (45)
																Одна стойка (46)
	+					+	×	+	×	×						16К слов, ПЛ, НМД (2,4 Мбайт), одна стойка (47)
						+	×									16К слов, ПЛ, одна стойка (48)
						+										8К слов, ПЛ, одна стойка (49)
						+	×									32К слов (28К), ПЛ, КНМЛ (2×100 Кбайт) (50)
						+	×									16К слов (51)
									+							28К слов, ГНМД (2×250 Кбайт) (52)
+						+	×			+						ПЛ, КНМЛ (53)
+						+	×			+						
+						+	×			+						Нет УВВПЛ (54)
								+	×	+	×					28К слов, НМД (2×2,4 Мбайт), НМЛ (2×20 Мбайт), АЦПУ, РА (55)
	+					×	×	+	×	+	+					
	+					×	×	+	×	+	+					

[Table continued on following page]

Table 5.1. [Continued from preceding page]

Условное обозначение комплекса	Основное назначение	Тип носителя для генерации программных средств			Основная характеристика									
		П	МД	М	пакетная обработка	обработка в режиме реального времени	обработка в режиме реального времени, высокоэффективная	обработка в режиме разделения времени	телеобработка данных	ведение баз данных	аналоговый режим	обработка графической информации	однопрограммный режим	
1	2	3	4	5	6	7	8	9	10	11	12	13	14	
СМ-3-08	ТСК с УСО-ОШ (56)	+		+	×	+								
СМ-3-08.01		×	+	+	×	+	+			×	+			
СМ-3-08.02		×	+	+	×	+	+			×	+			
СМ-3-09	ТСК с УСО-2К (вариантный) (57)	+		+	×	+								
СМ-3-09.01			+	+		+	+			×	+			
СМ-3-09.02			+	+		+	+			×	+			
СМ-3-09.03			+	+		+	+			×	+			
СМ-3-10	ТСК (58) многотерминальный с телеобработкой информации		+	+		+		+	+	+	+			
СМ-3-10.01														
СМ-3-10.02														
СМ-3-11	ТСК графический (59)		+	+		+		×			+	+		
СМ-4.01	Базовый дисковый (60)	+	+		+	+	+			+	+		+	
СМ-4-02.01	»	+	+		+	+	+			+	+		+	

[Table continued on following page]

Table 5.1. [Continued from preceding page]

обработки информации						Операционная система										Примечание
двухзадачный режим	многозадачный режим	многотерминальная обработка	режим повышенной надежности: резервирование процессора	режим повышенной надежности: резервирование внешних устройств	многомашинная обработка	ПЛОС, ДС СМ	ПЛОС РВ	ДОС	ДОС РВ	ФОБОС	ОС РВ	ДИАМС	ДОС РВР	ДОС+СТОД	ДОС АРМ	
15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
									+	×						28К слов, (61) НМД (2×2,4 Мбайт), НМЛ (2×20 Мбайт), ПЛ,
+	+					×	×	×	+	+	×					(62) Вариантность УСО
+	+					×	×	×	+	+	×					
									+	×						28К слов, (63) НМД (2×2,4 Мбайт), НМЛ (2×100 Мбайт), ПЛ
+	+					×	×	×	+	+	×					Две стойки УСО (64)
+	+					×	×	×	+	+	×					Одна стойка УСО (65)
+	+					×	×	×	+	+	×					Одна стойка УСО и УВБ-100 (66)
	+	+									×	+		+		28К слов, (63) НМД (2×2,4 Мбайт), НМЛ (2×100 Мбайт), ПЛ
																Восемь удаленных терминалов (67)
																Четыре удаленных терминала (68)
	+	+			+					+	×					28К слов, НМД (2×2,4 Мбайт), НМЛ (2×20 Мбайт), ПЛ, ГНМД, АЦПУ, ЭПГ, СМ (69)
+	+								+	×	+	×				28К слов, ПЛ, НМД (2,4 Мбайт), две стойки (70)
+	+								+	×	+	×				32К слов, ПЛ, НМД (2×2,4 Мбайт), две стойки (71)

[Table continued on following page]

Table 5.1. [Continued from preceding page]

Условное обозначение комплекса	Основное назначение	Тип носителя для генерации программных средств			Основная характеристика									
		П.Л	М.Д	М.Л	пакетная обработка	обработка в режиме реального времени	обработка в режиме реального времени, высокоэффективная	обработка в режиме разделения времени	телеобработка данных	ведение баз данных	диалоговый режим	обработка графической информации	одновадачный режим	
1	2	3	4	5	6	7	8	9	10	11	12	13	14	
СМ-4-02	Базовый с МЛ общего назначения (72)	+	+	+	+	+	+			+	+		+	
СМ-4-03	Базовый с МЛ общего назначения (72)	+	+		+	×					+		+	
СМ-4-04	Базовый минимального состава (73)	+	+		+	+					+		+	
СМ-4-05	ТСК с гибкими МД (74)													
СМ-4-05.01		+	+		+	×	+				+		+	
СМ-4-05.02			+		+		+				+			
СМ-4-06	ТСК с УСО-2К (75)	×	+	+		+	+			×	+			
СМ-4-06.01														
СМ-4-06.02														
СМ-4-06.03														
СМ-4-07	ТСК (76) многотерминальный с телеобработкой для многомашинных комплексов		+								-			
СМ-4-07.01			+	+		+		+	+	+	+			
СМ-4-07.02			+	+		+		+	+	+	+			
СМ-4-07.03			+	+		+		×	+	×	+			

[Table continued on following page]

Table 5.1. [Continued from preceding page]

обработки информации						Операционная система										Примечание
			режим повышенной надежности													
двухзадачный режим	многозадачный режим	многотерминальная обработка	резервирование процессора	резервирование внешних устройств	многомашинная обработка	ПЛОС, ДС СМ	ПЛОС РВ	ДОС	ДОС РВ	ФОБОС	ОС РВ	ДИАМС	ДОС РВР	ДОС+СТОД	ДОС АРМ	
15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
+	+							+	×	+	×					(77) 32К слов, ПЛ, НМД (2×2,4 Мбайт), НМЛ (20 Мбайт)
	+							+	×	+	×					64К слов, ПЛ, НМД (2×2,4 Мбайт), НМЛ (20 Мбайт), АЦПУ (78)
	+							+	×	+	×					32К слов, ПЛ, НМД (2,4 Мбайт), одна стойка (79)
																32К слов, ГНМД (2×250 Кбайт) (80)
+								+	×							ПЛ (81)
+																
+	+							×	×	×	+					32К слов, ПЛ или ГНМД (82)
																НМД (2×2,4 Мбайт) (83)
																НМЛ (2×20 Мбайт) (84)
																КНМД (2×100 Кбайт), ОЗУ (85) 64К слов
																(86) 64К слов, ПЛ, НМД (2×0,4×2,4 Мбайт), НМЛ (2×20 Мбайт), или КНМЛ (2×100 Кбайт), четыре — восемь терминалов, сопряжение с ЕС ЭВМ
	+	+			+							+	+	×		
	+	+			+							+	+	×		
	+	+			+							+	×	+		

[Table continued on following page]

Table 5.1. [Continued from preceding page]

Условное обозначение комплекса	Основное назначение	Тип носителя для генерации программных средств			Основная характеристика								
		ПЛ	МД	МЛ	пакетная обработка	обработка в режиме реального времени	обработка в режиме реального времени, высокореактивная	обработка в режиме разделения времени	телеобработка данных	ведение баз данных	аналоговый режим	обработка графической информации	однозадачный режим
1	2	3	4	5	6	7	8	9	10	11	12	13	14
СМ-4-08	ТСК графический для многомашинных комплексов (87)		+	×									
СМ-4-08.01			+	+		+		×			+	+	
СМ-4-08.02													
СМ-4-09	ТСК двухпроцессорный резервированный с УСО-2К (88)		+	+									
СМ-4-09.01		×	+	+	+	+	+			×	+		
СМ-4-09.02		×	+	+	+	+	+			×	+		
СМ-4-09.03		×	+г	+		+	+			×	+		
СМ-4-09.04		×	+г	+		+	+			×	+		
СМ-4-10	ТСК двухпроцессорный с резервированием с УСО-ОШ (89)		+										
СМ-4-10.01		×	+	+		+	+	×		×	+		
СМ-4-10.02		×	+	+		+	+	×		×	+		
СМ-4-10.03		×	+г	+		+	+	×		×	+		
СМ-4-10.04		×	+г	+к		+	+	×		×	+		

[Table continued on following page]

Table 5.1. [Concluded]

обработки информации						Операционная система										Примечание
			режим повышенной надежности													
двухзадачный режим	многозадачный режим	многотерминальная обработка	резервирование процессора	резервирование внешних устройств	многомашинная обработка	ПДОС, ДС СМ	ПДОС РВ	ДОС	ДОС РВ	ФОБОС	ОС РВ	ДИАМС	ДОС РВР	ДОС+СТОД	ДОС АРМ	
15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
																ЭПГ СМ 96К слов, ПЛ, НМД (90)
	+	+			+								×		+	(2×2,4 Мбайт), НМЛ, АДС
																УСВМ А71118 (или два ЭПГ СМ), БС АДС (91)
																(92)
	+	+	+	+				×	×		+					128 (124)К слов, ПЛ, НМД (2 Мбайт) или ГНМД, НМЛ (2×2×20 Мбайт)
	+	+	+	+				×	×		+					или КНМЛ (2×2×100 Кбайт)
	+	+	+	×				×	×		+					Вариантность УСО (93)
	+	+	+	×				×	×		+					
																(94)
		+	+	+				×	×		+					32К слов, ПЛ, НМД (2,4 Мбайт) или ГНМД, НМЛ (2×2×20 Мбайт) или КНМЛ (2×2×100 Кбайт)
		+	+	+				×	×		+					
		+	+	×				×	×		+					Связь через ПШ (95) Вариантность УСО (96)
		+	+	×				×	×		+					

Notations: + --used in the main version; X--use in different versions is possible; g--floppy and k--cassette

[Key on following page]

[Key continued from preceding page]

1. Notation of complex
2. Main designation
3. Type of carrier for software generation
4. Main characteristics of information processing
5. Punch tape
6. Magnetic disk
7. Magnetic tape
8.
9. Real-time processing
10. High-response real-time processing
11. Time-sharing processing
12. Remote data processing
13. Data base management
14. Dialogue mode
15. Graphical information processing
16. Single-task mode
17. Two-task mode
18. Multitask mode
19. Multiterminal processing
20. Increased reliability mode
21. Processor redundancy
22. External device redundancy
23. Multimachine processing
24. Operating system
25. Paper tape operating system and dialogue programming system
26. Time-sharing paper tape operating system
27. Disk operating system
28. Time-sharing disk operating system
29. Basic real-time background-operating system
30. Time-sharing operating system
31. Multiterminal time-sharing dialogue operating system
32. Time-sharing disk operating system
33. Disk operating system plus remote data processing system
34. Disk operating system of automated operator's position
35. Comments
36. SM
37. General-purpose basic disk (variant)
38. Minimum composition basic disk
39. Minimum-composition basic disk
40. Basic
41. Magnetic tape TSK (cassette, minimum composition)
42. Floppy magnetic disk TSK (variant)
43. Expanded general-purpose TSK (variant)
44. 28K words, punch tape, magnetic disk storage (2.4 Mbytes)
45. Two bays
46. One bay
47. 16K words, punch tape, magnetic disk storage (2.4 Mbytes) one bay
48. 16K words, punch tape, one bay
49. 8K words, punch tape, one bay
50. 32K words (28K), punch tape, multiple magnetic tape storage (2 X 100 Kbytes)
51. 16K words
52. 28K words, floppy magnetic disk storage (2 X 250 Kbytes)
53. Punch tape and multiple magnetic tape storage
54. No punch tape UVV
55. 28K words, magnetic disk storage (2 X 2.4 Mbytes), magnetic tape storage (2 X 20 Mbytes), alpha-numeric printer, arithmetic expander
56. TSK with USO
57. TSK with USO-2K (variant)
58. Multiterminal remote information processing TSK
59. Graphical TSK
60. Basic disk
61. 28K words, magnetic disk storage (2 X 2.4 Mbytes), magnetic tape storage (2 X 20 Mbytes), punch tape
62. USO variant
63. 28K words, magnetic disk storage (2 X 2.4 Mbytes), magnetic tape storage (2 X 100 Mbytes), punch tape
64. Two USO bays
65. One USO bay
66. One USO bay and UVB-100
67. Eight remote terminals
68. Four remote terminals

[Key continued on following page]

69. 28K words, magnetic disk storage (NMD) (2 X 2.4 Mbytes), magnetic tape storage (NML) (2 X 20 Mbytes), punch tape (PL), floppy magnetic disk storage (GNMD), alphanumeric printer (ATsPU), EPG and SM
70. 28K words, PL, NMD (2.4 Mbytes), two bays
71. 32K words, PL, NMD (2 X 2.4 Mbytes), two bays
72. Basic general-purpose magnetic tape
73. Minimum composition basic
74. Floppy magnetic disk TSK
75. USO-2K TSK
76. Multiterminal TSK with remote processing for multimachine complexes
77. 32K words, PL, NMD (2 X 2.4 Mbytes), NML (20 Mbytes)
78. 64K words, PL, NMD (2 X 2.4 Mbytes), NML (20 Mbytes), ATsPU
79. 32K words, PL, NMD (2.4 Mbytes), one bay
80. 32K words, GNMD (2 X 250 Kbytes)
81. Punch tape
82. 32K words, PL or GNMD
83. NMD (2 X 2.4 Mbytes)
84. NML (2 X 20 Mbytes)
85. KNMD (2 X 100 Kbytes), OZU of 64K words
86. 64K words, PL, NMD (2 X 0.4 X X 2.4 Mbytes), NML (2 X 20 Mbytes) or KNML (2 X 100 Kbytes), 4-8 terminals, integration with YeS EVM
87. Graphical TSK for multimachine complexes
88. Two-processor redundant TSK with USO-2K
89. Two-processor redundant TSK with USO-OSh
90. EPGSM, 96K words, PL, NMD (2 X 2.4 Mbytes), NML and ADS
91. USVM A71118 (or two EPG SM), BS ADS
92. 128 (124)K words, PL, NMD (2 Mbytes) or GNMD, NML (2 X 20 Mbytes) or KNML (2 X 100 Kbytes)
93. Variant of USO
94. 32K words, PL, NMD (2.4 Mbytes) or GNMD, NML (2 X 20 Mbytes) or KNML (2 X 100 Kbytes)
95. Communications through PSh
96. Variant of USO

These complexes have the following main features:

besides standard facilities of the SM EVM, complexes, devices and software, they include nonstandard devices, specially developed modules of operating systems, applied routine packs and so on;

the complexes are usually developed by the leading systems organization with participation of SVT developer organizations with regard to the characteristics of application of the given complex in a specific set of objects;

the composition of the hardware and software of the POK is refined when designing a user complex for a specific object on the basis of the POK, generation of the applied program packs of the POK, parametric adjustment of the software modules of the POK and so on are fulfilled. A user complex based on a POK is designed by its methodical materials.

A multiple user complex can be designed on the basis of several POK. Examples of POK are ARM [Automated operator's position] and IVK [Measuring computer complex]

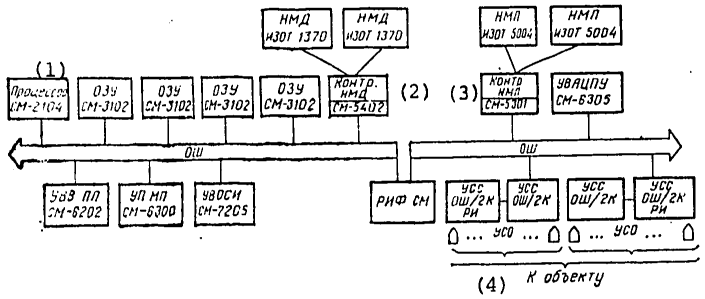


Figure 5.2. Standard Specified Complex of SM-4 With Complete Standard Bays of USO Based on USO SM-1 and SM-2 Modules

Key:
1. Processor
2. NMD monitor
3. NML monitor
4. To object

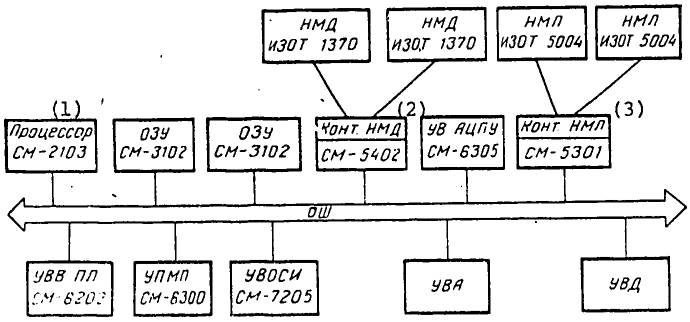


Figure 5.3. Standard Specified Complex of SM-3 With USO SM EVM

Key:
1. Processor
2. NMD monitor
3. NML monitor

complexes (see Chapter 6). A nonstandard operating system SOD ARM and applied program packs was developed during creation of the ARM and connection of such nonstandard devices as semiautomatic graphical information input devices, graph plotters and magnetic tape storage devices to the SM-3 and SM-4 was provided. The CAMAC dispatcher, a number of CAMAC modules, a CAMAC monitor and applied program packets, ASET dispatcher and IVK-7 and IVK-8 monitor were developed during creation of the POK IVK.

Table 5.2. Configuration Data of SM EVM Device

(1) Наименование	(2) Конструктивное исполнение	(3) Место установки	Количество стандартных мест (4)	Нагрузка на ОШ, ед. н. (5)	Потребление по переменному току (6)	Основные технические характеристики (7)
1	2	3	4	5	6	7
Процессоры СМ-3П, СМ-4П: (8) СМ-2103, СМ-2104	(9) АКБ	(10) Стойка	6U	1	500 В·А (11) (14)	
Расширитель арифметики (12)	БС (13)	»	1,5U	1	По постоянному току 20 Вт	Время операции 4,0—4,5 мкс, разрядность данных: 8, 16, 32 (15)
Оперативное запоминающее устройство СМ-3101 (16)	АКБ	»	8U	2	300 В·А	Емкость 32К слов, время цикла 1,2 мкс (17)
Блок ферритовой памяти СМ-3100 (18)	АКБ	»	6U	1	800 В·А	Емкость 32К слов, время цикла 1,2 мкс
Устройство оперативной памяти СМ-3102 (19)	АКБ	»	6U	1	500 В·А	Емкость 16К слов, время цикла 1,2 мкс (20)
Устройство ввода-вывода перфоленточное СМ-6201: (21) контроллер М1301, МР51	БЭ(22)	АКБ	6U	1	400 В·А	Скорость считывания 300 строк/с, скорость вывода 50 строк/с (23)
Устройство ввода-вывода перфоленточное СМ-6202: (24)						
контроллер (25)	БЭ	АКБ	6U	1	350 В·А	Скорость считывания 300 строк/с, скорость перфорации 50 строк/с
перфостанция (26)	АКБ	Стойка	6U	—		
Устройство печатающее алфавитно-цифровое СМ-6300: контроллер DZM-180 (27)	БЭ	(28) Консольное исполнение		1	260 В·А; (29) по постоянному току 75 Вт	(30) Скорость печати 180 зн./с, размер строки 132 слова

Key:

1. Name
2. Design version
3. Place of installation
4. Number of standard locations
5. Load on common bus, load units
6. Alternating current consumption
7. Main specifications
8. SM-3P, SM-4P processors: SM-2103 and SM-2104
9. Self-contained complete block
10. Bay
11. V·A
12. Arithmetic expander
13. Systems block
14. 20 watts of direct current
15. Operating time of 4.0-4.5 microseconds, digit capacity of data: 8, 16 and 32
16. SM-3101 internal storage device

[Key continued on following page]

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Table 5.2. [Continued from preceding page]

Наименование	Конструктивное исполнение	Место установки	Количество стандартных мест	Нагрузка на ОШ, ед. н.	Потребление по переменному току	Основные технические характеристики
1	2	3	4	5	6	7
Устройство печати алфавитно-цифровое: (31) (32) контроллер СМ-6304 (консольное исполнение) DARO1156 СМ-6302	БЭ	АКБ (28) Консольное исполнение		1	250 В·А	(33) Скорость печати 100 символов/с, длина строки 132 символа, конструкция знака — мозаичная матрица 5×7 точек
(34) Устройство вывода на печать параллельное: контроллер СМ-6305 (35) АЦПУ СМ-6315	БЭ	АКБ Консольное исполнение		1	800 В·А	(36) Скорость печати 500—700 строк/с, количество знаков 64, 96
Алфавитно-цифровой терминал СМ-7204: (37)					(39)	(40)
БЭ 810М	БЭ	АКБ		1	450 Вт	Количество строк 24, размер строки 80, количество символов 96
БЭ 002 (38) ВТА-2000-2 (подставка)	БЭ Настольное	»				
Алфавитно-цифровой видеотерминал: (41)						(43)
УВИТ	БЭ	АКБ	—	1	400 В·А	На базе СМ-1800, возможна регенерация изображения, совместим с АЦ дисплеями и АЦПУ
УВКС	БЭ (42)	АКБ	—			
УВКФ подставка (44)	Настольное Напольное					
Алфавитно-цифровой терминал СМ-7205:		(46)			(47)	(48)
БЭ 810М	БЭ	БСИ		1	7 Вт; по постоянному току±5В 157 Вт	Максимальная скорость ввода-вывода 1000 зн./с, количество строк 16, количество знаков в строке 80
БЭ 811М	БЭ	БСИ				
Видеотон-340 (45)	Подставка					

Key [Continued from preceding page]

17. Capacity of 32K words, time of cycle 1.2 microseconds
18. SM-3100 ferrite memory block
19. SM-3102 internal storage device
20. Capacity of 16K words, time of cycle 1.2 microseconds
21. SM-6201 papertape input-output device: MI301 and MP51 dispatcher
22. Component block
23. Reading speed of 300 lines/second, printing speed of 50 lines/second
24. SM-6202 papertape input-output device
25. Dispatcher
26. Punch station
27. SM-6300 alphanumeric printer: DZM-180 dispatcher
28. Console version
29. 75 watts of direct current

[Key continued on following page]

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Table 5.2. [Continued from preceding page]

Наименование	Конструктивное исполнение	Место установки	Количество стандартных мест	Нагрузка на ОШ, ед. н.	Потребление по переменному току	Основные технические характеристики
1	2	3	4	5	6	7
Устройство отображения графической (49) информации СМ-7300: процессор дисплея (50) монитор графический с блоком питания БП 12? (51) устройство ввода клавишное (52)	АКБ Настольное	Стойка	5U	1	600 В·А	(53) Количество адресуемых точек 1024×1024, время построения векторов максимальной длины не более 30 мс, суммарная длина линии в кадре при 50 Гц не менее 120 м, число градаций яркости 8, число типов линий 4, 128 символов, 40 строк, 72 символа в строке
(54) Устройство внешней памяти на магнитных дисках: контроллер СМ-5102 (55) НМД СМ-5402 (57)	АКБ АКБ	» »	6U 6U	1 —	500 В·А	(56) Количество подключаемых накопителей от 1 до 4, емкость накопителя 2,4 Мслов×2, скорость передачи 150 кслов/с
Устройство внешней памяти на гибком магнитном диске СМ-5603: контроллер (58) НМД PLX-45	АКБ	Стойка	6U	1	900 В·А	(59) Скорость передачи данных 35 кбайт/с, емкость 0,5 Мбайт
Устройство внешней памяти на магнитных лентах: (60) контроллер СМ-5301 (61) НМЛ СМ-5300	АКБ Стойка	Стойка	6U	1 —	1 кВ·А	(64) Количество подключаемых накопителей 1—4, скорость обмена информацией 10 кбайт/с, носитель совместим с ЕС ЭВМ, объем 10 Мбайт
Устройство внешней памяти на магнитной (62) ленте (УВПМП) СМ-5322: контроллер накопитель (63)	АКБ	Стойка		2	625 В·А	(65) Скорость передачи 64—126 кбайт/с, объем 40 Мбайт, четыре НМЛ информационно совместимых с ЕС ЭВМ

Key [Continued from preceding page]

30. Printing speed of 180 characters per second, line size of 132 words
31. Alphanumeric printer
32. SM-6304 controller (console version)
33. Printing speed of 100 symbols per second, length of line 132 symbols, character structure--mosaic matrix of 5 X 7 points
34. Parallel printing device
35. SM-6305 dispatcher and SM-6315 alphanumeric printer
36. Printing speed of 500-700 lines per second, number of characters 64 and 96
37. SM-7204 alphanumeric terminal
38. Accessory
39. Watts

[Key continued on following page]

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Наименование	Конструктивное исполнение	Место установки	Количество стандартных мест	Нагрузка на ОШ, ед. н.	Потребление по переменному току	Основные технические характеристики
1	2	3	4	5	6	7
Устройство внешней (66) памяти на базе кассетного накопителя на магнитной ленте (УВПК): контроллер накопитель РК-1	АКБ	»	6U	1	150 В·А	(67) Объем 5,6 Мбит, скорость записи 4 кбит/с (68) Емкость кассеты 400 К байт, скорость передачи данных 0,5 кбайт/с
Широкоформатный графический экранный пульт проектировщика (ШГЭПП2): (69) контроллер дисплейный процессор (70) блок памяти (71) устройство индикации (72) блок клавиатуры (73)					(74)	Позволяет подключить два устройства, размер рабочего поля экрана 350×350 мм, количество адресуемых точек 2048×2048, объем буферной памяти 16К байт, время построения символа 35 мкс
Устройство преобразования (75) графической информации в цифровой код (УПГИ) А5122 контроллер УСГИ А5123	БЭ	(76) Консольное исполнение			300 В·А (77)	Размер рабочего поля планшета 850×600 мм, скорость в режиме дискретного преобразования 4800 точек/с, в режиме непрерывного преобразования 100 точек/с
(78) Блок расширения системный (БРС)			6U			
(79) Адаптер дистанционной связи (АДС)	(80) Кассета монтажная	АКБ	2U	2	—	(81) Выход на два канала передачи данных: модем — модем, модем — дисплей ВТ-340, модем — телетайп Т-63, скорость работы 50—9600 Бод.

Key [continued from preceding page]

40. Number of lines 24, line size 80, number of symbols 96
41. Alphanumeric video terminal
42. Desk
43. Based on SM-1800, image regeneration is possible, compatible with alphanumeric displays and alphanumeric printers
44. SM-7205 alphanumeric terminal
45. Vidioton-340
46. Systems interface block
47. ± 5 V direct current, 157 watts
48. Maximum input-output speed 1,000 characters per second, number of lines 16, number of characters per line 80

[Key continued on following page]

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Наименование	Конструктивное исполнение	Место установки	Количество стандартных мест	Нагрузка на ОШ, ед. н.	Потребление по переменному току	Основные технические характеристики
1	2	3	4	5	6	7
Переключатель шины СМ-4501 (82)	АКБ	Стойка	6U	1	500 В·А	(83) Задержка цикла передачи сигналов через ПШ 500 нс, нагрузка ПШ по входу 2 ед. н., по выходу 18 ед. н.
(84) Устройство ввода-вывода аналоговых сигналов (УВА)	АКБ	Стойка	8U	1	200 В·А	(85) Максимальное количество каналов 1024, скорость опроса контактных коммутаторов 200 каналов/с, бесконтактных коммутаторов 600 или 2000 каналов/с
(86) Устройство ввода-вывода дискретных сигналов (УВД)	АКБ	»	8U	1	200 В·А	(87) Максимальное количество каналов ввода-вывода — 3072, емкость счетчика — 16 разрядов
(88) Устройство ввода-вывода быстродействующее УВБ-200	АКБ	»	8U	1	200 В·А	(89) 48 дискретных сигналов ввода 48 дискретных сигналов вывода, 24 аналоговых сигнала ввода и 2 аналоговых сигнала вывода (200 кГц)
Крейт КАМАК: (90) крейт (91) контроллер крейта (92) модули (93)	Крейт КАМАК	Стойка	8U	1	900 В·А	(94) Содержит подсистемы ввода-вывода аналоговых и дискретных сигналов, ввода инициативных сигналов, генератор тактовых импульсов и констант

Key [Continued from preceding page]

49. SM-7300 graphical information display device
50. Display processor
51. Graphical monitor with DP122 power supply block
52. Keyboard input device
53. Number of addressable points 1,024 X 1,024, maximum-length vector plotting time no more than 30 milliseconds, total length of line per frame at 50 Hz not less than 120 meters, number of brightness gradations 8, number of types of lines 4, 128 symbols, 40 lines, 72 symbols per line

[Key continued on following page]

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Table 5.2. [Concluded]

Наименование	Конструктивное исполнение	Место установки	Количество стандартных м_ст	Нагрузка на ОШ, ед. н.	Потребление по переменному току	Основные технические характеристики
1	2	3	4	5	6	7
Расширитель интерфейса СМ-4101 БЭ9402 (два) (95)	Кассета монтажная	АКБ	1,5U	1,1	—	(96) Увеличение длины на 15 м, задержка чтения на 0,35 мс, задержка записи на 0,25 мс
Устройство согласования сопряжений УСС-ОШ12К: (97)						
блок управления (98)	АКБ	Стойка	4U	2	800 В·А (100)	Количество устройств 2К, подключаемых к программному каналу, 16; количество устройств 2К, подключаемых к двум каналам прямого доступа, 16; при использовании восьми расширителей возможно подключение до 120 устройств
блок интерфейсный (99)	АКБ	Стойка	6U			
Устройство сопряжения вычислительных машин (УСВМ) (101)						Расстояние между сопрягаемыми ЭВМ 50 м, скорость передачи данных в режиме прерывания 40 тыс. байт/с, в режиме прямого доступа — 800 тыс. байт/с
А71118:					500 В·А (105)	
блок интерфейсный (102)	АКБ (103)	Стойка (104)				
УСВМ	Тумба	Напольное				
Универсальный программируемый контроллер СМ-4301 (106)	Кассета монтажная	АКБ	6U	1	50 В·А (108)	Внутренняя тактовая частота 5—10 МГц, размер преобразуемого массива 4096, ширина полосы сигнала 500 кГц
Спецпроцессор быстрого преобразования Фурье СМ-5410 (107)	Стойка	Стойка	—	1	1 кВ·А (109)	

Key [Continued from preceding page]
54. Magnetic disk external storage device
55. SM-5102 dispatcher
56. Number of connected storage devices from 1 to 4, capacity of storage device 2.4 Mwords X 2, transmission speed of 150 Kwords per second
57. SM-5603 floppy magnetic disk external storage device
58. Dispatcher
[Key continued on following page]
59. Data transmission speed of 35 Kbytes/s, capacity of 0.5 Mbytes
60. Magnetic tape external storage device
61. SM-5301 dispatcher
62. SM-5322 magnetic tape external storage device (UVPMP)
63. Storage device

Key [Continued from preceding page]

64. Number of connected storage devices 1-4, information exchange rate 10 Kbytes/s, carrier compatible with YeS EVM, capacity of 10 Mbytes
65. Transmission speed of 64-126 Kbytes/s, capacity of 40 Mbytes, 4 magnetic tape stores informationally compatible with YeS EVM
66. Cassette magnetic tape external storage device (UVPK)
67. Capacity of 5.6 Mbits, recording speed of 4 kbits/s
68. Cassette capacity of 400 Kbytes, data transmission speed 0.5 Kbytes/s
69. Wide-format designer graphical screen console (ShGEPP2)
70. Display processor
71. Memory block
72. Display device
73. Keyboard block
74. Permits connection of two devices, size of operating field of screen 350 X X 350 mm, number of addressable points 2,048 X 2,048, capacity of buffer storage 16 Kbytes, time of symbol formation 35 microseconds
75. A5122 graphical information to digital code converter (UPGI)
76. Console version
77. Size of operating field of plotter 850 X 600 mm, speed in digital conversion mode 4,800 points/s, speed in analog conversion mode 100 points/s
78. Systems expansion block (BRS)
79. Remote communications adaptor (ADS)
80. Installation cassette
81. Output to two data transmission channels: modem-modem, modem-VT-340 display, modem-T-63 teletype, operating speed of 50-9,600 bauds
82. SM-4501 bus switch
83. Signal transmission cycle delay through PSh 500 ns, PSh load: two load units through input, 18 load units through output
84. Analog signal input-output device (UVA)
85. Maximum number of channels 1,024, contact commutator interrogation rate 200 channels per second, contactless commutator interrogation rate 600 or 2,000 channels per second
86. Digital signal input-output device (UVD)
87. Maximum number of input-output channels 3,072, counter capacity 16 digits
88. UVD-200 high-speed input-output device
89. 48 digital input signals, 48 digital output signals, 24 analog input signals and 2 analog output signals (200 kHz)
90. CAMAC crate
91. Crate
92. Crate controller
93. Modules
94. Contains analog and digital signal input-output subsystems, initiative signal input subsystem and timing pulse and constant generator subsystem
95. SM-4101 BE9402 interface expander (two)
96. Increase of length by 15 meters, readout delay by 0.35 ms, recording delay by 0.25 ms
97. USS-OSh12K integration matching device
98. Control block
99. Interface block

[Key continued on following page]

Key [Continued from preceding page]

100. Number of 2K devices connected to program channel 16, number of 2K devices connected to two direct access channels 16; connection to 120 devices is possible when using eight expanders
101. A71118 computer integration device (USVM)
102. Interface block
103. Pedestal
104. Floor
105. Distance between integrated computers 50 meters, data transmission speed in analog mode 40,000 bytes per second, data transmission speed in direct access mode 800,000 bytes per second
106. SM-4301 universal programmable dispatcher
107. SM-5410 fast Fourier transform special processor
108. kV·A
109. Internal timing frequency 5-10 MHz, size of transformable file 4,096, width of signal band 500 kHz.

USO Configuration Based on Devices Having 2K Junction Output

The presence of OSh interface and 2K-USS OSh/2K interface matching devices in the nomenclature of the SM-3 and SM-4 permits the use of all the nomenclature of devices and modules of the ASVT-M (M-400, M-6000, M-7000) and SM-1 and SM-2 having output to the 2K interface as object communications devices.

5.4. Operating Conditions of the Complex

Complexes configured from SM EVM hardware should be operated under conditions corresponding to GOST [State standard] 20397-74 for articles of group 3B having direct contact with the external medium.

The maximum operating conditions of the complex are the following:

Climatic Factors	Maximum Variations of Factors	
	Lower	Upper
Temperature, °C	+10	+35
Relative humidity at +30°C, percent	--	90
Atmospheric pressure, mm Hg	735	785

A single-phase alternating current industrial system (220 V, 50 $\pm$ 1 Hz) is used as the main primary power supply. Smooth and intermittent variations of voltage of +10 $\pm$ 15 percent from the nominal value are permitted.

The complexes should be installed in dry heated buildings. The height of ceilings in the building is not less than 3 meters. The ceiling and walls should be faced with sound-absorbing materials of light tones. A whitewash coating is not permitted.

Louvers or blinds should be provided in the window sills.

The use of fuel and flammable materials is not permitted during construction and finishing of buildings. Automatic fire signalling devices should be provided.

Lighting is fluorescent or incandescent lamps with diffusion device. Lighting is not less than 150 luxes at a height of 0.8 meter from the floor. The lighting of operators' positions and keyboards is 350-400 luxes. Emergency lighting from a separate power source must be provided.

An area of not less than 15 m^2 is required for arrangement of the SM-3 and SM-4 complexes and not less than 10 m^2 is required for the auxiliary equipment.

An insulated production floor which prevents accumulation of static electricity should be provided if possible. The degree of static charge capacity of the coating should provide a charge leakage time of not more than 30 seconds.

The production floor is designed for loads of not less than 300 kilograms per panel. The recommended size of the panel (nonmetal or metal) is 650 X 650 mm. The space between the production floor and the main floor is not less than 208-250 mm in height. If a production floor cannot be provided, cable channels protected on top by wooden shields must be provided.

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