STATUS REPORT

for period

1 September through 30 September 1970

U. S. GOVERNMENT

STAT

File No. 11038

STAT

This document is presented as the Monthly Status Report under Contract to the U. S. Government, [redacted]

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The report period represented herein covers the period 1 September through 30 September 1970.

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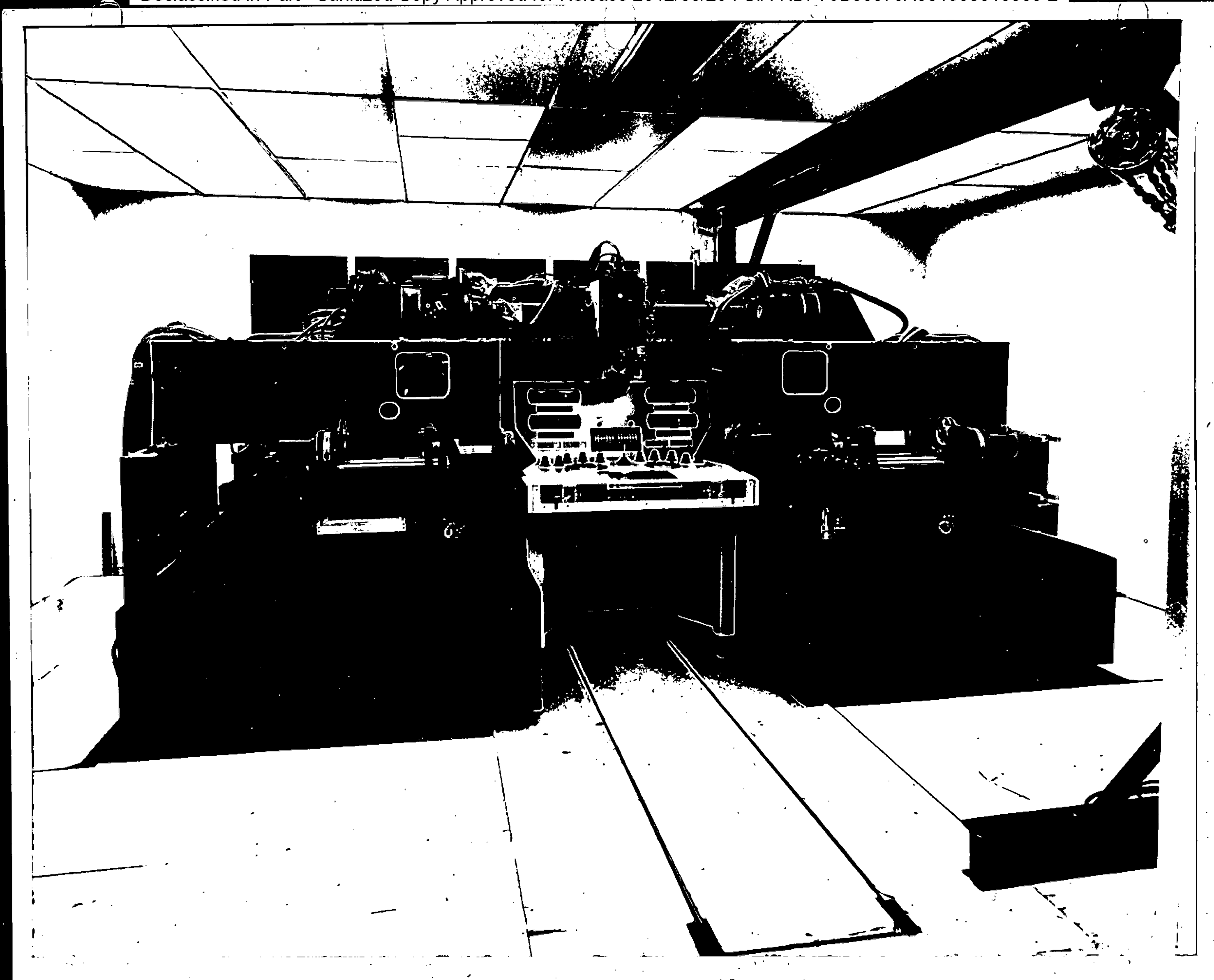

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INDEX

PROGRAM SUMMARY

Scheduled percentage of completion	98.5%
Actual percentage this date	94.5%

Two major subassemblies of the Stereocomparator have been found to be deficient in their performance, namely,

1) The Interferometer measuring system.
2) The stage position countdown registers.

These devices as they were originally designed were apparently satisfactory but under the stress of extensive usage problems have arisen which necessitate extensive rework.

Unfortunately the in-plant acceptance test requires all systems to be operative. Further, a minimum of three weeks is required to integrate the computer program with the revised subassemblies. As a consequence, the revised schedule shows that the in-plant acceptance test completion date is revised from November 20, 1970 to December 31, 1970.

There is a problem with this latter date in that it interferes with the holiday schedule. If it turns out not to be possible to shorten the schedule, it may have to be increased to perhaps January 15, 1971 to be more realistic.

On this basis, the completion of the on-site final acceptance test would be possibly May 7, 1971.

Task 2

SCHEDULING and PLANNING

Scheduled percentage of completion	100%
Actual percentage this date	99%

Because of additional work found necessary during checkout and test, the schedule has been revised to show a delivery eight weeks after the schedule made on June 15, 1970.

The new schedule indicates a final acceptance test completion date of May 7, 1971.

The schedule of October 5, 1970, is attached.

STEREOCOMPARATOR SCHEDULE October 5, 1970

		Completion Date
1.	Installation of revised interferometers and mirrors	October 30, 1970
2.	Installation of revised interferometer electronics	November 6, 1970
3.	Installation of revised counting logic	October 23, 1970
4.	Completion of vibration dampers	November 6, 1970
5.	Completion of Informatics computer program	November 27, 1970
6.	Acceptance test in-plant (Work to start December 11, 1970)	January 15, 1971
7.	Packing, shipping, and unpacking (Work to begin January 18, 1971)	February 12, 1971
8.	Assembly at site (Work to begin February 8, 1971)	March 26, 1971
9.	Preacceptance test	April 23, 1971
10.	Final acceptance test	May 7, 1971

Task 3

TEST and INSPECTION PROCEDURES

Scheduled percentage of completion	100%
Actual percentage this date	100%

Procedures for performing the Acceptance Tests for the Stereocomparator have been delivered to the customer.

These procedures cover the in-plant tests as well as the on-site final tests.

Various documents outlining the proposed tests have been submitted . The first submittal was on June 15, 1970.

These latest procedures show the up-date as of September 15, 1970. The latest specifications are included as of September 11, 1970.

Task 22

INTERFEROMETER ASSEMBLY

Scheduled percentage of completion	100%
Actual percentage this date	75%

Mechanical detail drawings of the interferometer have been completed and are presently being released to the shop for fabrication.

Details of parts to mount the Rochon prism and quarter and half wave plates are being held until those optical parts arrive. This is to make sure that data about mounting dimensions, etc. is correct.

Task 28

OUTPUT LOGIC and INTERFACES

Scheduled percentage of completion	100%
Actual percentage this date	100%

During this report period general logic testing and debugging has continued. A number of minor modifications have been incorporated into the logic circuitry to accommodate hardware/software interfacing. It is expected that this type of work will continue throughout the period of time during which software integration is in process.

The machine logic appears to be operating in a generally satisfactory manner with one exception, which is discussed in the following paragraphs. This exception is the forward-backward binary counters (23-bit) which are used in the stage servo countdown positioning systems and also as position reference accumulators for the computer system.

Throughout the construction and testing of the Stereocomparator machine, these particular counters have shown erratic performance. Various circuit modifications have been made which have improved operation, but the level of performance has not been brought to that which is considered satisfactory for use in the machine on a day-to-day basis.

During the last report period, a design review was undertaken to investigate the difficulties experienced, and it was decided that the best solution would be to change the counting logic. This can be done by designing special logic cards which are essentially interchangeable with the units presently installed in the machine. It was determined that this work could be done within the remaining time before delivery of the machine, and since the improvement in operation to be obtained is quite significant, this work has commenced. The action being taken and the results of the design review follow.

I. Results of Design Review

The binary counters presently in the machine have a tendency to suddenly become loaded with large numbers in an erratic fashion. The result of this is that the measuring stages suddenly have a large command loaded into the servo systems and the stages move away from their proper positions occasionally, usually in large amounts. When the

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machine is operating in its MANUAL (no computer) mode, the result is a loss of position; in the AUTOMATIC modes of operation, if the error occurs in the binary countdown register, no visible effect occurs since the computer will reload the proper number into the countdown register within 1/120 second, and the servo system cannot respond to the erroneous count within this time. If, however, the (separate) stage position register contains the erroneous number, the reference point for the coordinate measuring system used by the computer is lost, and a runaway condition occurs very similar to that in the MANUAL operating mode. Since the occurrence of either type of error is unsatisfactory, the purpose of the design review was to isolate and remedy the causes for this behavior of the systems.

A review of the circuitry involved showed the following conditions to be causing the erroneous counting. Each is discussed separately below.

1) Counting speed limitations imposed by cable loading on counter flip-flops.

2) Triggering of counter flip-flops by noise on output lines of flip-flops.

3) Noise on counter inputs which is non-synchronous with the counting pulses.

4) Error mechanism in synchronous counters.

Items 1) and 2) above are caused by having the counters drive long cables between electronics cabinets in the case of the countdown registers. The counters are located in Electronics Cabinet No. 3 and the lines are brought through cables to the 23-bit D/A converters in Electronics Cabinet No. 1. There is approximately 40 feet of cable between the chassis containing the circuits which are interconnected. These long cables present a heavy capacitance load to the counters, and the counting speeds are limited by the rate at which the counters can charge and discharge the cable capacitance. At present, the counters can operate to about 500KHz provided no reversing is required. Also, the long cables form a large antenna for noise pickup. The DTL circuits used in the flip-flops can be triggered at their outputs rather easily, since the line impedance of the "off" side of the flip-flop is at least 500 ohms. Thus, noise currents of only 2 to 3 mA can trigger the flip-flop, since the "off" side output is crossconnected to an input of the "on" side. The susceptibility of the counters to items 1) and 2) is greatly magnified by the fact that DTL synchronous circuits are used, as explained below.

Both of the problems 1) and 2) above can be solved by buffering the flip-flop outputs. In practice, only the countdown register is connected to long output lines; the stage position register outputs are tied to buffer registers immediately adjacent physically to the counters, so that conditions 1) and 2) apply only to the countdown registers.

Item 3), non-synchronous noise on the counter inputs, has been dealt with extensively in the machine circuitry. In order to minimize problems in this area, a large amount of circuitry has been added to provide:

a) hysteresis (anti-dither circuit).

b) digital averaging (irregularly-spaced interferometer pulses are processed through variable delay circuitry so that at high speeds the pulses are spaced to allow carry ripple-outs.

c) elaborate pulse-dodging circuits to prevent simultaneous inputs of interferometer pulses, trackball pulses (MANUAL mode only) and jam-transfers from the joystick (MANUAL mode only) or computer (AUTOMATIC modes).

All of the above measures improved counter operation; however, an occasional stray pulse still gets in, and the effects noted occur. The problem of input noise triggering is magnified by the fact that the counters are synchronous circuits, and any non-synchronous imputs produce indeterminate counter contents. In order to illustrate this phenomenon, it is necessary to examine the operation of both synchronous and asynchronous forward-backward counting logic.

A synchronous counter circuit of the type used in the machine is shown in Figure T28-A. It consists of J-K flip-flops and 2-NAND gates for carry and borrow pulses. The 2-NAND gates monitor the states of a given flip-flop and the forward-reverse count lines and enable or inhibit toggling of the next stage, depending on whether a carry occurs. For example, assume that the counter shown contains all zeros (0000). With the Reverse Inhibit line at Logic "1", the first clock pulse will merely toggle the first flip-flop in the string, giving a count of 0001. The next clock pulse will reset the first flip-flop on the trailing edge of the pulse. Meanwhile, however, since the first flip-flop is at a logic "1", the second flip-flop is enabled to toggle as well by the 2-NAND gates. Thus, at the end of the clock period, the counter contains the number 0010 (binary 2). This sequence continues for every count, with the rule being that if a given flip-flop is at the "1" state and the Reverse Inhibit line is at Logic "1" (or, more importantly, the Forward Inhibit line is at Logic "0"), then the succeeding stage is allowed to toggle also. A similar sequence occurs during reverse counting. Notice, however, that the clock line is connected to all flip-flops in the string in parallel. This common clock line is the salient feature of every synchronous counter, although various ways exist to develop the carry signals, etc.

Now, in operation, it may be seen that in between clock pulses, the carry signals are developed for the next count. Examination of the logic diagram for the counter shows, however, that the carry signals are propagated through two NAND gates per stage of the counter. Thus the propagation through a 23-bit counter is approximately 1.5 microsecond, maximum.

Now, since the state of any given flip-flop is determined by the state of the carry gates at clock time, it can be seen that if another clock pulse occurs before the carry signals have fully propagated, then incorrect results will be obtained. And since the carry signals propagate from least significant to most significant place in the counter, it can be seen that <u>any errors generated will be large ones</u>. Thus, if a counter is going from 0000... to 11111... (zero to -1) and a pulse or noise occurs on the clock line at the time that the carry signal has propagated to (say) bit 16, then <u>all</u> higher order bits will be clocked to the incorrect state, and a very large error results; this error mechanism has been the source of much of the unsatisfactory performance in the counters.

An asynchronous counter is diagrammed in Figure T28-B. In many respects the counters look very similar, the main difference between synchronous and asynchronous counters being the manner in which carry signals and clock signals are generated.

It will be noticed that the J-K flip-flop inputs are not used in this system; only the toggle (clock) input is required. Examination of the gating structure shows that the rule, for clocking any given flip-flop is, "if the preceding stage is at a Logic 1 and an "up" count comes into the system such as to toggle the preceding stage, then toggle this stage also." Thus, it may be seen that operation of any given flip-flop is dependent only on the state of the two previous flip-flops. The input of the counter has no direct access to the higher order bits, since the clock signal for each stage of the counter is determined by the previous stage. It is thus impossible for the clock to get out of synchronism with the carry signals, since both the carry and clock signals are one and the same. Thus, in order for a noise pulse to affect bit 16 of an asynchronous counter, it would be the 16,384th mistake on the input - a highly unlikely situation. The important advantage of this type of counter is that the effect of an erroneous noise pulse is to make the counter wrong by 1 count only. Also, since the counter can have inputs applied only at the input end of the clocking string, the speed at which the counter can operate is the speed of a single stage. It is even possible to have two counts propagating simultaneously through the counter with no bad effects! It is true that if one attempts to read out the contents of the counter before the carries have all rippled out, an erroneous reading will be obtained, but in our application we have buffers in the circuitry to eliminate this problem entirely. Any mistakes made are thus small (low-order) ones.

In conclusion, the asynchronous counter logic should be highly advantageous in solving the foregoing problems. The use of buffered asynchronous counter logic is thus indicated since it will provide:

a) greater tolerance for clock pulse characteristics with respect to timing considerations.

b) the error mechanism of the counter is such that if a mistake is made, it is simply a 1 count error.

II. <u>Action being taken with respect to Results of Design Review</u>.

In order to incorporate the improved counting logic within the Stereocomparator machine with a minimum of changes to the hardware, a new counter card is being designed which will be a plug-in replacement for the synchronous counter cards in the machine. Some slight modifications to the pulse-steering circuitry will be performed in order to accommodate the different input clocking arrangement for the asynchronous counters.

These new boards will be fabricated and installed in the countdown registers during the next report period. Tests will then be run to determine whether the new counter logic is also required for the 23-bit stage position registers. This latter requirement is somewhat doubtful, due to the fact that the stage position registers do not suffer from the heavy cable loading that the countdown registers have. Also, there are fewer inputs, since the countdown registers must also accommodate the manual trackball and joystick inputs as well as automatic computer jam-transfers in automatic operation. The stage position register merely follows the interferometer inputs, with a computer-ordered dump into a buffer in automatic modes of operation, so it does not have the confusion factors existing in the countdown registers.

However, the stage position register is the only reference for the systems under computer control, and mistakes are not permissible without loss of the coordinate references; therefore, if tests show that the stage position register exhibits an excessive error rate with present circuitry, then the improved asynchronous counter logic will be used here also. This work can probably be done within the next report period.

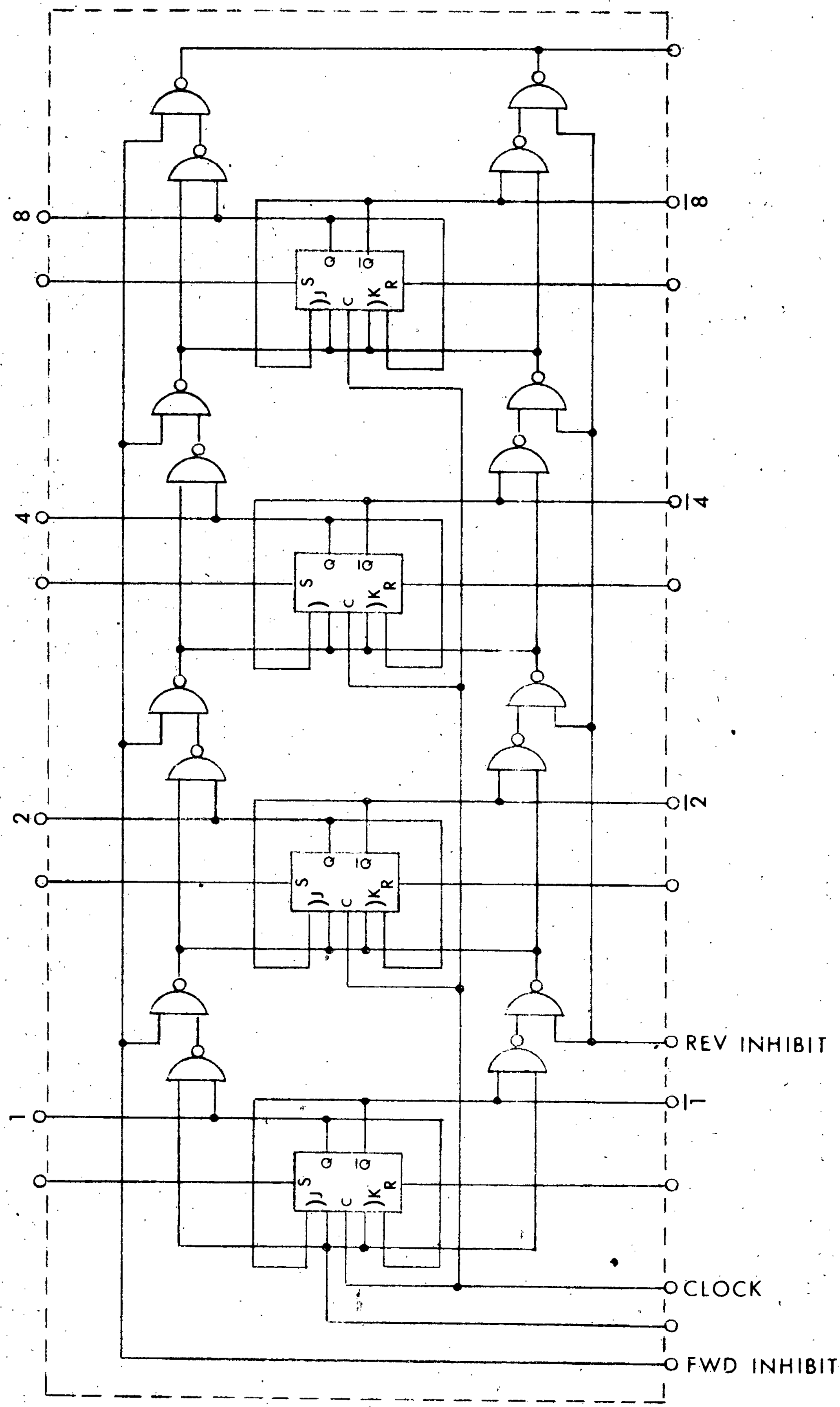

FIG T28-A SYNCHRONOUS COUNTER

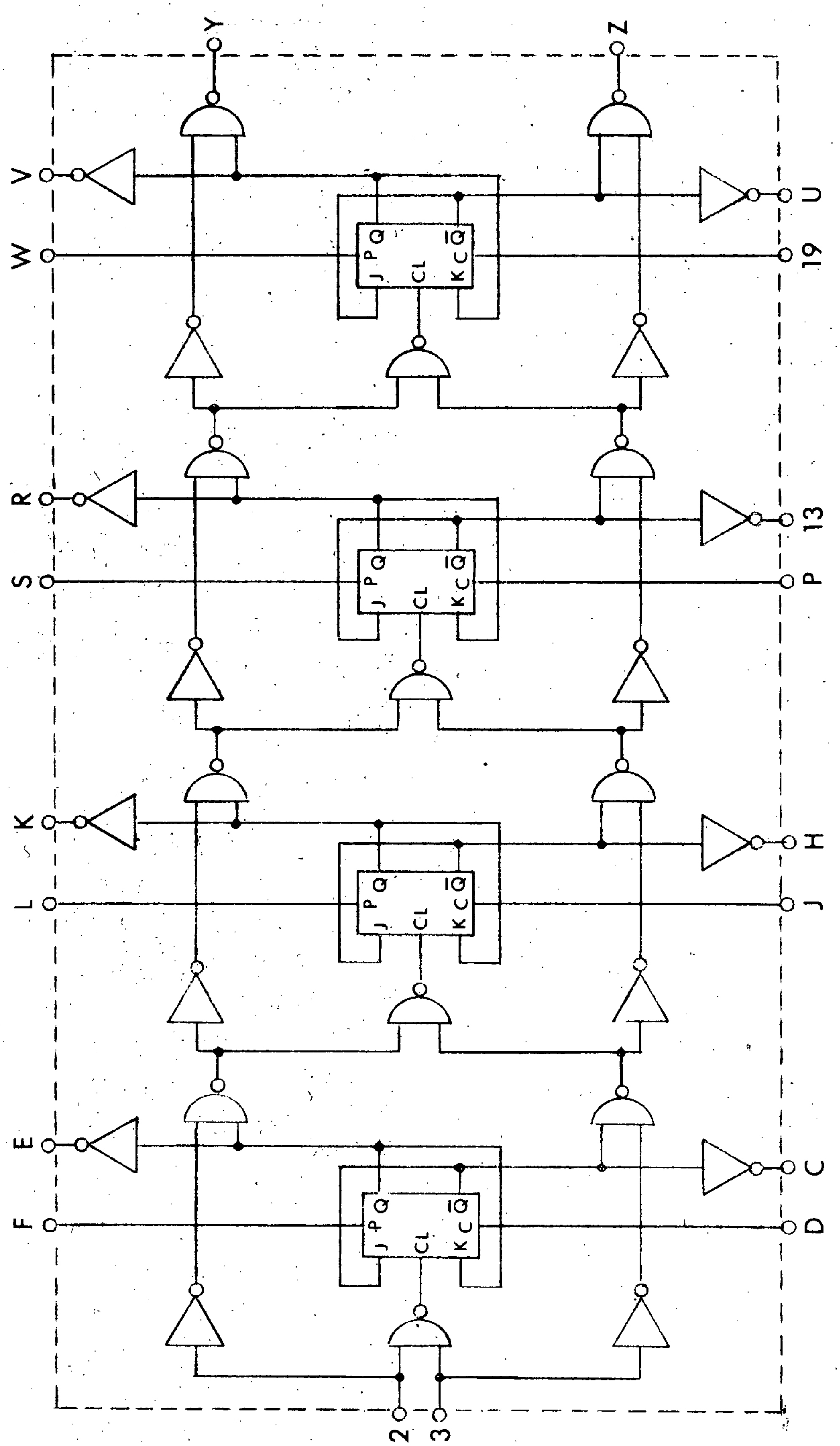

FIG T28-B ASYNCHRONOUS COUNTER

Task 35

VIBRATION ABSORPTION and LEVELING

Scheduled percentage of completion	100%
Actual percentage this date	90%

The dash pot layout has been completed and a new envelope drawing submitted to the customer.

The dash pot uses 25 pairs of plates 12" OD and 5" ID. The moveable plates are cantilevered from the granite on the fore and aft centerline. The fixed plates are mounted through a welded steel bracket to the floor. Different mountings are required [redacted] and at the customer's facility. The dash pot will use a silicone oil of 10,000cs, such as Viscasil.

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Task 36

OVERALL ASSEMBLY

Scheduled percentage of completion	100%
Actual percentage this date	90%

The overall assembly of the Stereocomparator is progressing as follows:

Optical Assembly:

The optical elements are aligned to produce above specification resolutions and image wander. Optimizing of the alignment is still proceeding.

Image Dissector and Light Level:

Light-tight housings for the image dissector and light level tubes are being fabricated and installed on the Stereocomparator.

Interferometer:

The rework of the interferometer assembly is progressing. To facilitate programming, encoders have been mounted on the X and Y axes of both stages temporarily in lieu of the interferometers.

Task 43

COMPUTER PROGRAMMING and SERVICES

Scheduled percentage of completion	100%
Actual percentage this date	94%

The [redacted] report on the status of the computer program effort for the Stereocomparator is included on the following page.

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INFORMATICS INC.

MONTHLY PROGRESS REPORT

August, 1970

This technical report is for the month of August, 1970. The report is prepared according to [redacted] STAT specifications DB1001 (as modified).

1. During August the accommodation of the software to the 16K core expansion was completed as planned. Final integration of the Stereocomparator program was begun; however, hardware problems have hindered progress on the software.

2. During September Informatics personnel will continue final integration [redacted] STAT If hardware problems delay software tasks (example - computer was out of order for 10 days), work will be done on peripheral tasks, off the main line of work. Also work will be done on the calibration/checkout program as time permits.

3. At this time there exist no pending unresolved technical problems.

The programming for Project 342 is 90% complete.