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PHASE I REPORT

on

THE KEYER MEMORY

November 30, 1960

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KEYER MEMORY

Weight and Power

Total Weight Less Batteries	3.8 lbs.
Case Weight	2.7 lbs.
Net Weight	1.1 lbs.
Equivalent Case Weight in Aluminum	0.9 lbs.
Net Weight	1.1 lbs.
Theoretical Total Weight	2.0 lbs.

Battery Drain

Function Switch Position	D-C Current Milliampers	Power Milliwatts
Standby (S)	218	544
Receive (R)	238	595
Idle (I)	230	575
Transmit (X) Standby	270	675
Transmit (X) Operating	240	600

Battery Source - Sonotone nickel cadium size D rechargeable

cells - terminal voltage 1.25 volts each.

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SECTION I

INTRODUCTION

The Northville program covers the design, development, and fabrication of a Keyer Memory unit which provides non-volatile storage of approximately 100 words of 6 characters each. The Keyer Memory is implemented through the use of low-cost, solid-state circuits and a coincident-current, ferrite-core memory packaged within the minimum volume practicable. Desired size of the unit is 6 inches x 1-1/2 inches x 2-1/2 inches for a total volume of 31.5 cubic inches. The above effort constitutes Phase One of the program and is to culminate in the delivery of a Keyer Memory unit for test and evaluation by the customer. Dependent on the results of the evaluation a Phase II is planned to provide four additional units for service tests.

The original specification called for an 1800-bit buffer memory using the twistor technique for storage. The disadvantages of larger volume, longer development time, and higher cost of the twistor memory were outlined in a proposal submitted by Burroughs. The additional possibility of increasing the capacity to 2500 bits in the same volume with a ferrite-core, coincident-current memory resulted in a decision to delete the twistor requirement when the program was funded.

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The program was modified during the latter part of 1959 to provide for an integrated Keyer Memory. Significant advantages in cost and volume were possible, primarily through the elimination of duplicate circuit functions, power supplies, and structural elements.

The Keyer Memory unit is a completely self-contained device permitting the manual insertion of 2560 bits stored in a ferrite core memory. The information is stored 4 bits at a time by depressing any one of 12 keys on a keyboard integral to the Keyer Memory. Through the incoming information has a character format identical to the 5-unit start/stop teletype code, only 4 units need to be stored to provide for the 12 characters used. The start baud is used only for control and the fifth and stop bauds are not used. This gives a total character storage of 640 and a 6-character-per-word storage of 106 2/3 words. Once the memory has had any number of words inserted up to the maximum capacity, the entire contents can be read out of the Keyer Memory at a nominal rate of 60 words per minute.

The read-out cycle, once initiated by the operator, is automatic and nondestructive. As each character is transmitted to the external receiving device, the same character is re-inserted into the memory. The entire memory can be completely cleared by properly actuating three switch controls. The controls are electrically interlocked to minimize accidental clearing.

The Keyer Memory (figure 1) measures 8 inches by 4 inches by 1-5/8 inches for a volume of 52 cubic inches without batteries. The prototype weighs   pounds including 2.7 pounds for the brass case and cover. (The use of heavy material for the enclosure

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Table I. Keyer Memory Specifications

	Volume	Component Count	Component Density
KE-9 and Buffer Memory	6 in x 1.5 in x 3.5 in = 31.5 in^{3*}	——	——
KE-9	3 5/16 in x 2 1/8 in x 7/8 in = 6.2 in^3	97	$\frac{97}{6.2}$ = 15.5 per in^3
Keyer Memory	8 in x 1 5/8 in x 4 in = 52 in^3	4058	$\frac{4058}{52}$ = 78 components/in^3
Keyer Memory Less KE-9	31.5 in^{3*} – 6.2 in^3 = 25.3 in^3	3961	$\frac{3961}{25.3}$ = 157 components/in^3

*Original Specification

is discussed in the mechanical design section.) The average power dissipation is 600 milliwatts supplied by two D-size, Nicad batteries.

In table I the volumes, component counts, and component densities are tabulated for various conditions. The specification furnished before the program was initiated requested a volume of 31.5 cubic inches. Though this volume included both the buffer memory and the KE-9 Keyer, the proposal submitted by [   ] assumed that the 25X1 31.5 figure applied to the buffer memory only. The proposal included a design goal of 100 components per cubic inch. The actual overall density came out to 78 components per cubic inch and a total volume of 52 cubic inches. The volume of the memory proper was originally estimated at 2 cubic inches and the actual volume is 1.4 cubic inches.

The inability to meet the desired volume can be attributed largely to the extreme temperature limits specified. The normal range with worst-case design of a ferrite core memory is 55°C. The specification calls for a temperature range of minus 50°C to $+50^{\circ}$C. Relaxing the worst case designs and changing the lower limit to minus 40°C kept the problem realistic but still made for difficult packaging. The temperature range and high component density required considerably more component evaluation than originally anticipated. Even the use of factory adjustments to remove initial component tolerances did not provide sufficient relief to ease the packaging problems. An Appendix on Circuit Design Criteria is included in this report. Certain schematic diagrams referred to in the following sections are provided under seperate cover.

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SECTION II

CIRCUITS AND LOGICAL OPERATION

The Keyer Memory is designed to provide a system with simplicity, small physical volume, low cost, and operation from low power. Information can be written into the memory at random with the manual keys of the keyer and stored until required. When memory information is required it can be transmitted sequentially at teletype speed. Logic symbols used in the [   ] program are described in figure 25X1 and the logic diagram is shown in figure 3.

MAJOR UNITS

The Keyer Memory is comprised of nine major units. The function of these units is as follows:

1. Power Supply. The power supply is capable of converting either the voltage of two series-connected dry cell batteries (3 volts) or the voltage of two series-connected Nicad batteries (2.5 volts) to four regulated and two unregulated voltages. Although designed for this capability, the prototype Keyer Memory is set internally to operate only from Nicad batteries.

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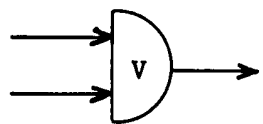
Symbol	Name	Description
OR gate symbol (V)	OR Gate	Output is -2V with 1 or more inputs at -2V. OR gates have 2 to 4 inputs.
AND gate symbol (•)	AND Gate	Output is -2V when all inputs are -2V. No output when all inputs are not at -2V. AND gates have 2 to 5 inputs.
Box with 1 / 0	Set-Reset Flip-Flop	A -2V input to either side will produce a -2V output at the same side. A -2V input to the other side will then reverse the state of the flip-flop.
Box with 0 / 1	Complementing Flip-Flop	A +2V complement input reverses the state of the flip-flop. The ZERO input is the reset input.
INV circle	Inverter	Output is the complement of the input. -2V input = 0V output. 0V input = -2V output.
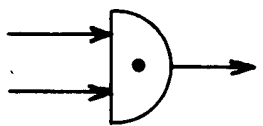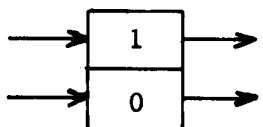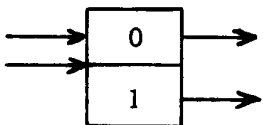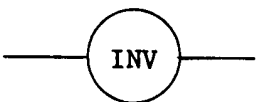
Figure 2. [   ] Logic

25X1

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2. Mode Selector Switch. This switch selects the desired mode of operation and connects the logic biases for the specific mode.

3. Keyer. The keyer consists of 12 manual keys and a decoder. In the RECEIVE (R) mode of operation the keyer is used to write information into the memory; each key selects specific fixed information.

4. Logic Circuits. These circuits perform the required logical functions for the selected mode of operation.

5. Address Circuits. The address circuits are a system of counters used to address the memory to read and write memory information sequentially.

6. Drivers. Driver circuits generate the currents necessary for switching the memory cores and, when properly addressed, deliver these currents to the selected memory word.

7. Memory. The memory consists of 2560 ferrite cores (one core per word) and associated selection diodes; each core stores 1 bit of information.

8. Sense Amplifier. The sense amplifier detects the core outputs when the memory is interrogated and amplifies these outputs to a usable level.

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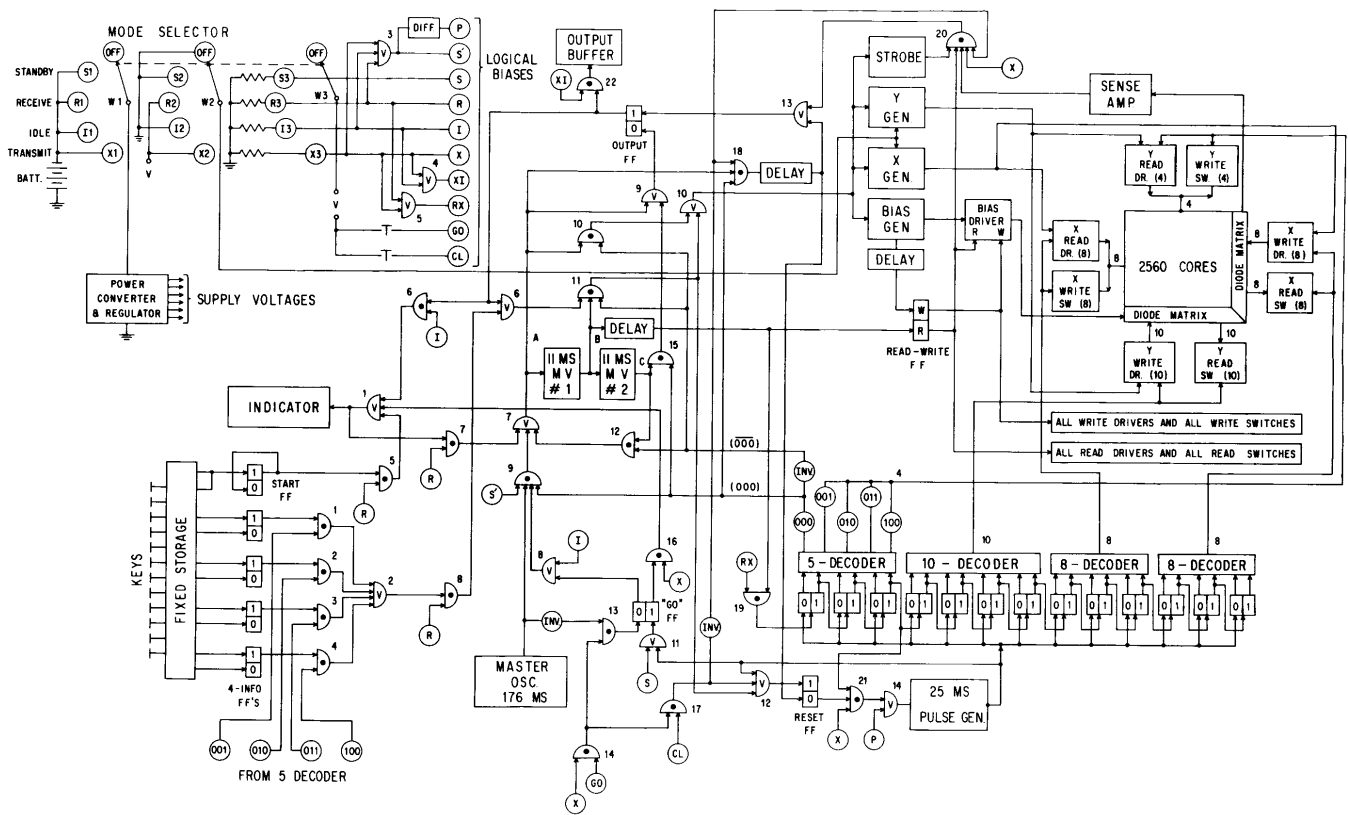
Figure 3. Keyer Memory Logic Diagram

9. Output Buffer and Indicator. The output buffer provides buffered output information to other equipment used with the Keyer Memory. The indicator circuit, using an incandescent bulb, indicates when contact has been made in depressing a key of the keyer, provides a rough indication of proper operation during IDLE (I), and indicates the end of the message during the TRANSMIT (X) mode of operation.

MODES OF OPERATION

Four modes of operation are used. The desired mode is selected by a 5- position mode selector switch; the fifth position is OFF. Operation in each of these modes is as follows:

1. STANDBY. Power converter on with biases applied to prepare the equipment for operation.

2. RECEIVE. For writing information into the memory.

3. IDLE. Idling characters are generated (one START baud followed by all marks).

4. TRANSMIT. This position permits reading information from and restoring information to the memory, and the clearing of the memory.

CIRCUIT DESIGN

Circuits of the Keyer Memory were selected from existing proven circuitry and adapted to fill the requirements of the program. These circuits will operate within

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a temperature range of minus 40 degrees Centigrade to plus 50 degrees Centigrade.
Satisfactory operation can be obtained when using as a primary source of power two
series-connected dry cells or two series-connected Nicad batteries, although the
prototype will use only Nicad batteries. End-of-life voltage for the series-connected
dry cells is 2.2 volts; end-of-life voltage for the series-connected Nicad batteries is
1.8 volts. The indicator lamp, which is connected across half of the battery voltage,
will function until the voltage across it falls below approximately 1.2 volts. The in-
formation baud length at the output is 22 milliseconds, plus or minus 3 percent; the
STOP baud length at the output is 28 milliseconds, minimum.

A description of the selection of circuit design criteria is included as Appendix I to
this report.

Modified Coincident-Current Memory

In a conventional coincident-current memory three half-select currents are utilized;
an X current, Y current, and Inhibit current, each of which are half the value of
nominal switching currents. Reading is accomplished by the coincidence of X and Y
to give a full switching current at the X-Y intersection. Writing a ONE is accomplished
by the coincidence of negative X and Y currents. Writing a ZERO (not writing a ONE)
is accomplished by the triple coincidence of X, Y, and Inhibit currents.

If I_{th} is defined as the maximum current which will guarantee no core switching and
I_s is defined as the minimum current to ensure complete core switching, then the
memory current equations which must be satisfied are:

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$$I_x \leq I_{th} \text{ (unselected cores)}$$

$$I_y \leq I_{th} \text{ (unselected cores)}$$

$$I_{inh} \leq I_{th} \text{ (unselected cores)}$$

$$I_x + I_y - I_{inh} \leq I_{th} \text{ (writing a ZERO in the selected core), and}$$

$$I_x + I_y \geq I_s \text{ (reading, or writing a ONE in the selected core).}$$

The best switching-to-no-switching current (neglecting current tolerances) is therefore 2 to 1.

This use of a 1-bit word permits modification of these equations to obtain a 3-to-1 ration. Because of the 1-bit per word, there is no ONE and ZERO combination which must be written at the same time; only a ONE or a ZERO. This permits X and Y currents to be 2/3 switching currents, and the inhibit current (referred to as the bias current) to be a negative 1/3 switching current. Therefore, during read,

$$I_x - I_{bias} \leq I_{th} \text{ (unselected cores)}$$

$$I_y - I_{bias} \leq I_{th} \text{ (unselected cores)}$$

$$I_x + I_y - I_{bias} \geq I_s \text{ (selected core)}$$

The above equations are applied to negative currents during the writing of a ONE. When writing a ZERO no currents are turned on, thereby eliminating the need for

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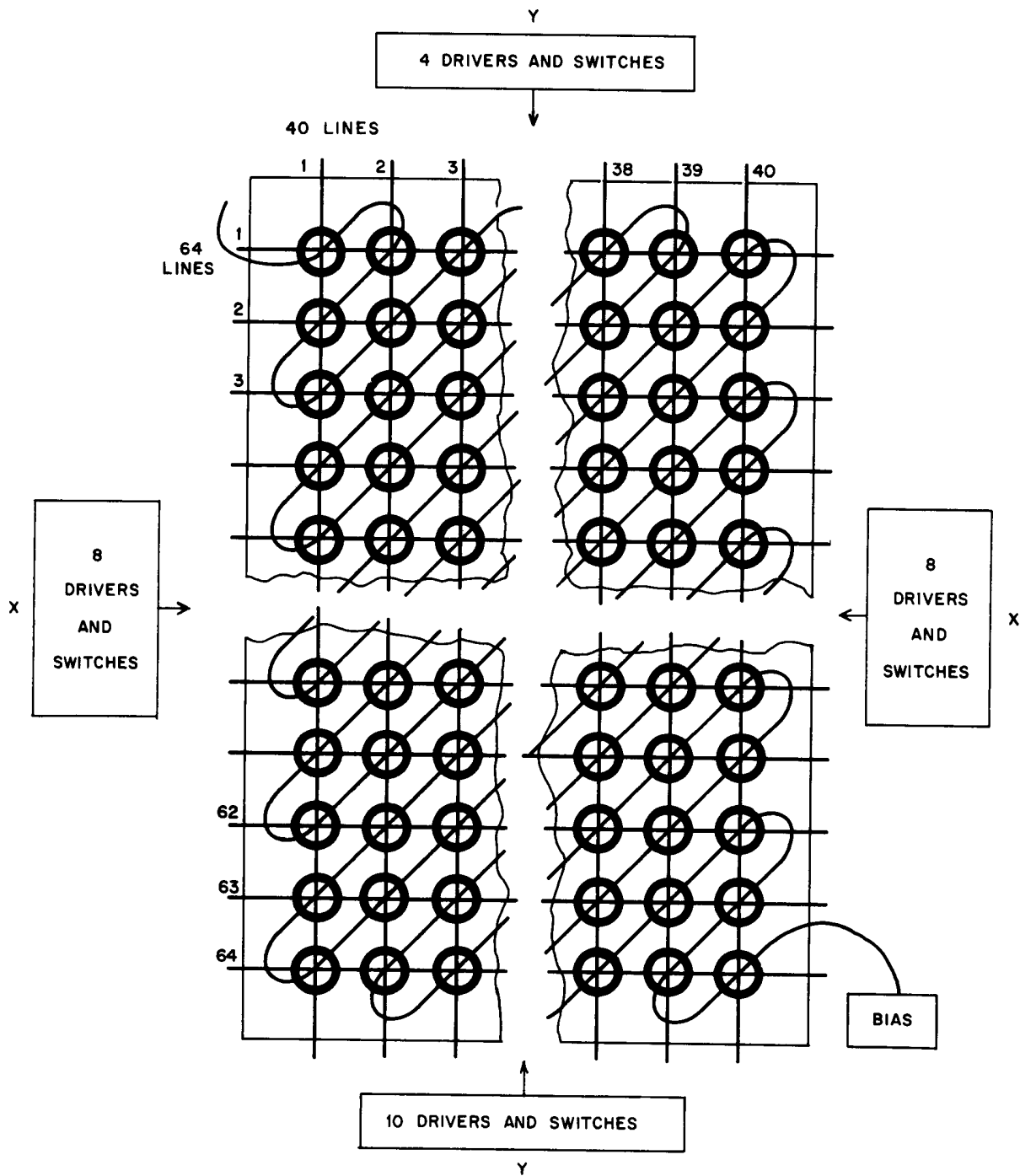
Figure 4. Memory Configuration

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an equation for this function. The 1/3 and 2/3 read currents as specified are sub-

stituted, resulting in:

$$2/3 - 1/3 = 1/3 \text{ (no-switching current)}$$

$$2/3 - 1/3 = 1/3 \text{ (no-switching current)}$$

$$2/3 + 2/3 - 1/3 = 1 \text{ (switching current)},$$

which gives the 3 to 1 ratio.

The configuration for this modified coincident-current memory is shown in figure 4.
The ferrite cores are arranged in a 64-by-40 matrix. An 8-by-8 driver switch de-
livers the X currents and a 4-by-10 driver switch delivers the Y currents. Bias
current is carried by a single line threaded through all the cores of the matrix.

Memory Selection. The memory selection scheme representation is shown in the
upper right in figure 3. The following description is of the Y drivers and switches,
since operation of the X drivers and switches is identical. For a particular address
in the address counters, one of the four outputs from the 5-DECODER will select
one of four Y-read drivers and the corresponding Y-write switch. One of the outputs
of the 10-DECODER will select one of the ten Y-write drivers and the corresponding
Y-read switch. The total number of lines that can be selected is therefore 10 times
4, or 40 lines. The Y-line current, (from the Y-current generator) is delivered to
the selected line. The drivers and switches are further selected by the output of the
output of the read-write flip-flop. When the flip-flop is in the READ (R) state, the
read drivers and read switches are selected. When the flip-flop is in the WRITE
(W) state, the write drivers and write switches are selected.

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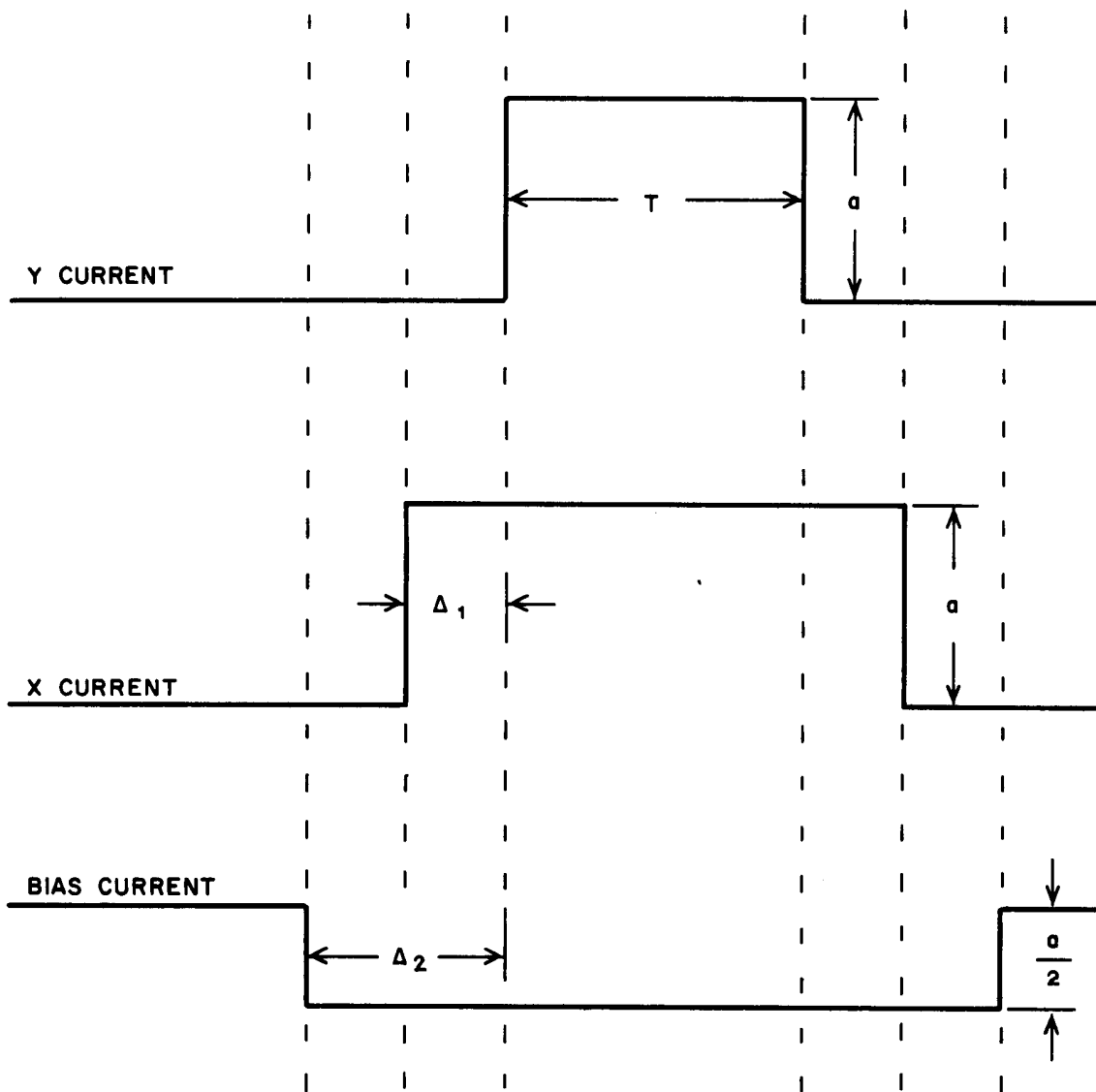
Figure 5. Current Time Relationships

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Memory Operation. Beginning with the read cycle, the read-write flip-flop is in the READ state, and the address counters are set to a particular count. Therefore, one read driver and one read switch are energized in both the X and Y directions. Since the bias driver is associated with all words, it is addressed only by the read-write flip-flop; it also is set when the read-write flip-flop is in the READ state. An input pulse, applied simultaneously to the X, Y, and bias-current generators, produces three current pulses. The time relationship of these current pulses is shown in figure 5.

If the Y pulse is of amplitude, a, and duration, T, then the X pulse is of amplitude, a, and duration $T + \Delta_1$, and the bias pulse is of negative amplitude $a/2$ and duration $T + \Delta_2$. If $a/2$ is approximately $1/3$ switching current, then with the bias pulse turning on first, there is a negative $1/3$ noise current in all cores. When the X pulse is turned on, a $2/3 - 1/3 = +1/3$ noise current is delivered to the selected X line. When the Y pulse is turned on a $2/3 - 1/3 = +1/3$ noise current is delivered to all cores in the selected Y line except one, which is the core in coincidence with X and Y. This core receives $2/3 + 2/3 - 1/3 = +1$ (full switching current). If the core was in the ONE state it is now switched to the ZERO state and the core output produced is sensed by the sense amplifier. Turnoff of the bias generator triggers the read-write flip-flop to the WRITE state but the address counters remain at the same count.

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During the write cycle, two conditions can occur. If a ZERO is to be written, the input pulse is inhibited and no currents are generated. Since the core went to the ZERO state during the read cycle, no currents are required during the write cycle. In writing a ONE the same sequence is used as in the read cycle except that the write drivers and switches are energized, delivering negative currents to the cores. The currents produced, in the order of current generator turnon, are:

1. Bias. Plus 1/3 noise current in all cores

2. X Generator. Minus $2/3 + 1/3 = -1/3$ noise current in the X line

3. Y Generator. Minus $2/3 + 1/3 = -1/3$ noise current in the Y line, and

4. Minus $2/3 - 2/3 + 1/3 = 1$ (full current) in the selected core. This core is then switched to the ONE state.

In summarizing the operation, read current always exists, switching the selected core to the ZERO state. Write current flows in the same addressed lines as read current if a ONE is to be written. If a ZERO is to be written, turn on of all three current generators is prevented.

Power Supply

The power supply is comprised of a dc-to-dc converter and four transistor regulators and provides six rectified output voltages. The dc-to-dc converter consists of a free-running multivibrator transformer coupled to the rectifier circuits. Power to operate

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the converter is supplied by batteries. Four of the six rectified output voltages are regulated by the transistor regulators; the other two voltages (plus 7 volts and minus 7 volts) are filtered but not regulated.

The outputs of the four regulated voltages (plus 2 volts, minus 2 volts, plus 5 volts, and minus 5 volts) are controlled by Zener diodes. The output of a regulated voltage is therefore $V_{out} = V_{diode} - V_{be}$.

The frequency of the power supply oscillator is 30 kilocycles, plus or minus 10 kilocycles. For the remaining power supply specifications refer to table II. Drawing 4093-1004, contains the power supply circuit diagram.

Mode Selector Switch Circuit

The switch circuit consists of the mode-selector switch, ganged 5-position switches and the gating necessary to provide the logical bias outputs (figure 3). Switch deck 1 (with shorting contacts) is used to connect power to the converter in all positions except OFF. Switch deck 2 is used to apply either ground or plus 5 volts to the current generators. Since the current generators are used only during the receive and transmit modes the plus 5-volt supply is applied only in these positions. Switch deck 3 connects the logical biases and the P pulse. The diode gates are all OR gates which provide an output of minus 2 volts if only one input (minus 2 volts) is present. When the switch is changed from one position to another a negative pulse is applied to a

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Table II. Power Supply Specifications

VOLTAGE	TOLERANCE (volts)	MAXIMUM LOAD (ma.)
+ 2.0 V*	± 0.15	10.0
- 2.0 V*	± 0.15	10.0
+ 5.0 V*	± 0.2	10.0
- 5.0 V*	± 0.2	25.0
+ 7.0 V	± 1.0	2.0
- 7.0 V	± 1.0	2.0

*Regulated

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one-shot multivibrator, producing a single output pulse P of approximately 35 micro-
seconds. Drawings 4093-1004 and 4093-1005 contain the Mode Selector Switch
Circuit Diagram.

Keyer

The keyer consists of 12 manual keys and a wired-core decoder. The decoder is
comprised of four flip-flops, a one-shot multivibrator, and gating. The keyer cir-
cuit diagram is contained in drawing 4093-1001.

Depressing a key causes a pulse of current to be sent through a particular wire (of
the wired core decoder) which passes through some combination of the core trans-
formers. Outputs of the core transformers are used to set the four information flip-
flops. The states of these four information flip-flops are then sensed serially by
their associated AND gates and the address inputs. The keyer information output
therefore is the serial output of the four information flip-flops.

All of the wires pass through the core transformer associated with the one-shot
multivibrator so that whenever a key is depressed, a keyer START pulse is generated.
The keyer START output is a negative pulse which goes from minus 0.1 volt (plus or
minus 0.1 volt) to minus 2.2 volts (plus or minus 0.3 volt). The pulse duration is
35 milliseconds, plus or minus 25 milliseconds.

Since the current pulse delivered to the wired-core decoder is the result of the
charge on a capacitor, a definite time must be allowed between breaking the contact

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of one key and depression of the next key. If five time constants are allowed to permit the capacitor to fully charge, the time separation is:

$$5 \times 100 \times 10^{3} \times 10^{-6} = 0.25 \text{ seconds.}$$

Pulse Generators

The plus 5-volt input from the mode-selector switch is present only during the RECEIVE (R) and TRANSMIT (X) modes of operation. In other modes, this input is at ground potential, preventing any transient from generating a current-pulse output (figure 3). Drawing 4093-1039 contains the Pulse Generator circuit diagram.

The input to the pulse generators (from the logic circuits) is a negative pulse of approximately 25 microseconds duration. This pulse is applied simultaneously to the X-, Y-, and bias-pulse generators. Each pulse generator consists of two delay multivibrators in tandem followed by two stages of current amplification. The bias pulse generator has a 3.5-microsecond delay multivibrator followed by a 7.5-microsecond delay multivibrator. The 7.5-microsecond delay multivibrator generates the current pulse which is amplified to full bias current.

The delays of the multivibrators associated with the X-pulse generator are 4.5 microseconds and 5.5 microseconds; delays of the multivibrators associated with the Y-pulse generator are 5.5 microseconds and 3.5 microseconds. An input pulse to the pulse generators therefore turns on all three generators, but not simultaneously. The bias generator turns on first and turns off last. The X-pulse generator output is within

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the bias-pulse time, and the Y-pulse generator output is within the X-pulse time. The leading edge of the Y generator pulse is used to generate a strobe pulse for the sense amplifier output. For specifications of the pulse generator refer to table III.

Driver and Switch Circuits

The purpose of the driver and switch circuits is to steer the current pulses of the X and Y current generators through the proper X and Y memory-core lines in the proper direction, and to steer the bias current in the proper direction through the bias winding (figure 3). Drawing 4093-1007 contains the schematic for this circuit.

Considering first the X and Y drivers and switches, each driver and switch consists of a current-steering transistor and a 2-input AND gate. The two inputs are the address and the output of the read-write flip-flop. If both inputs are negative, the base of the current-steering transistor is negative and the pulse current can pass through this transistor. Because of the long delay (11 milliseconds) permitted to set up these drivers and switches, a large capacitor is connected to the base of the current-steering transistor. When current passes through the transistor, the base voltage changes very little. Use of this capacitor minimizes the power required to energize the drivers and switches. All of the driver circuits are clamped at minus 2 volts while the switches are not clamped. The gate inputs go from zero volts to minus 5 volts. This places the base of the energized driver at minus 2 volts and the base of the energized driver at minus 2 volts and the base of the energized switch at minus 5 volts which puts a 3-volt drop across the selected line of cores through which

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Table III. Pulse Generator Specifications

GENERATOR	INITIAL DELAY	PULSE DURATION	OUTPUT CURRENT (25°C)	RISE TIME	FALL TIME
Y	5.5(± 0.4) μsec.	3.5(± 0.4) μsec.	118 ma. (±9%)	0.2(± 0.1) μsec.	0.6 sec. max.
X	4.5(± 0.4) μsec.	5.5(± 0.4) μsec.	118 ma. (± 9%)	0.2(± 0.1) μsec.	0.6 sec. max.
Bias	3.5(± 0.4) μsec.	7.5(± 0.4) μsec.	68 ma. (± 9%)	0.2(± 0.1) μsec.	0.6 sec. max.

Note: The output current should have a temperature coefficient of approximately
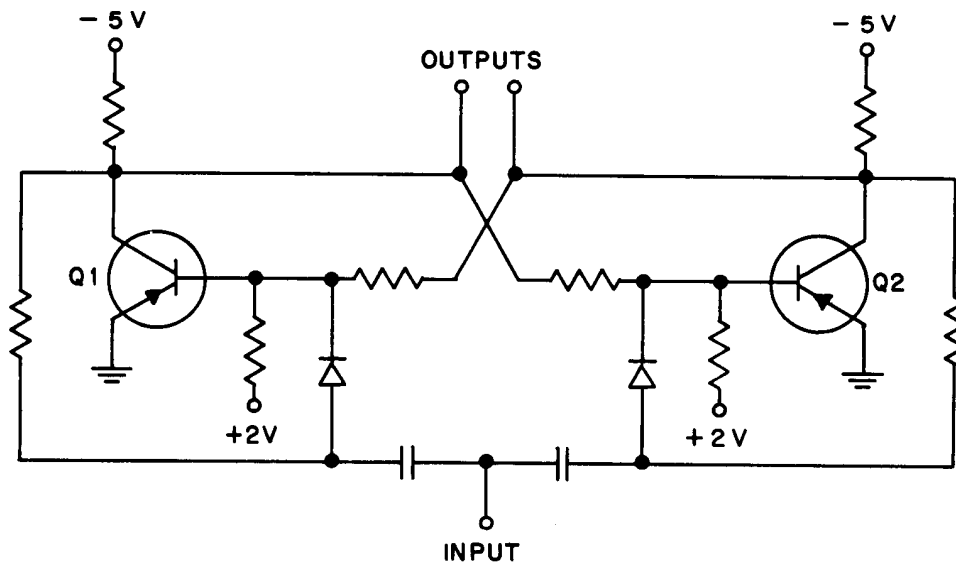   minus 0.45 percent per degree Centigrade.

Figure 6. Complementing Flip-Flop

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the pulse current passes. For this reason the address and read-write flip-flop outputs are zero to minus 5 volts. All other signal voltages in the system are from zero to minus 2 volts.

Operation of the bias drivers and switches is similar to the X and Y drivers and switches with one exception. There is only one bias line, and current passes through this line independent of the address. There is, therefore, no address input to the bias drivers and switches.

Output current of the X and Y drivers at $25^{\circ}C$ is 118 milliamperes, plus or minus 9 percent. Output current of the bias driver at $25^{\circ}C$ is 64 milliamperes, plus or minus 9 percent. The base voltage rise during a current pulse is 1.0 volt, maximum.

Address Circuits

The addressing circuits consist of 13 complementing flip-flops in tandem (figure 3). Drawing 4093-1006 contains the schematic for the address circuits. The basic circuit of a complementing flip-flop is shown in figure 6.

A positive input pulse will reverse the state of the flip-flop. If transistor Q1 is on and Q2 is off, the collector of Q2 is at minus 5 volts. The anode of the steering diodes associated with Q2 will also be minus 5 volts. The collector of Q1 will be near ground potential as well the anode of its associated steering diode. A positive pulse input will have no effect on Q2 provided the pulse is less than 5 volts but it will

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turn off Q1 which in turn turns on Q2. Conditions will then reverse and the next positive input pulse will turn off Q2, and so on.

The first three flip-flops in the address counter are used to count five pulses and then reset to the starting position although they are capable of counting to 8 (2^3). When the fifth count is reached, a diode decoder sends a negative output to circuit A, (drawing 4093-1006) which resets the three flip-flops to the starting condition. The next four flip-flops, although capable of a count of 16 (2^4), are used to count 10. A similar circuit (A) is used here to reset these four flip-flops after 10 counts. The next 3 flip-flops count 8 (2^3), and the last three flip-flops also count 8. No internal resetting is required as these flip-flops are used to their full counting capability.

The diode decoders associated with the address flip-flops are used to produce, for a given address:

1. One negative and four positive outputs from the first three flip-flops (5-DECODER).

2. One negative and nine positive outputs from the next four flip-flops (10-DECODER).

3. One negative and seven positive outputs from the next three flip-flops (8-DECODER).

4. One negative and seven positive outputs from the next three flip-flops (8-DECODER).

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Sense Amplifier

The sense amplifier consists of two stages of differential amplification followed by single-ended output (figure 3). Drawing 4093-1005 contains the schematic for this circuit. The purpose of the differential stages is to reject common mode noise. For gain stabilization a considerable amount of degeneration is used in the first two stages. This amplifier will give a negative output for either positive or negative input signal.

Also associated with the sense amplifier is a 1-transistor multivibrator which generates the strobe pulse, and a 5-input AND gate which controls the sense amplifier output so that it is fed to other circuitry only at the proper times.

Indicator

The indicator circuit consists of a combination of AND and OR gates followed by a buffer stage which activates the indicator light. When activated, the light is connected across one of the two batteries used for primary power (figure 3). Drawing 4093-1005 contains the schematic for the indicator circuit.

One-Shot Multivibrator

The input to the standard one-shot circuit is a negative pulse, the duration of which need only be sufficient to permit feedback action (figure 7). The duration of the negative-going output pulse is dependent on the RC time constant.

The one-transistor multivibrator requires a positive input pulse (negative for an NPN transistor), the duration of which must be longer than that of the output pulse.

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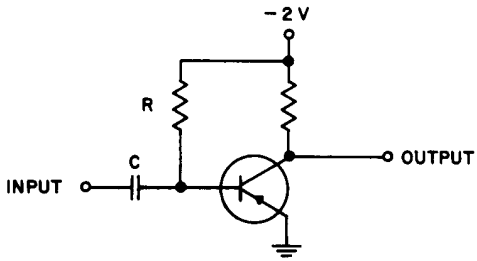
a. One-Transistor One-Shot
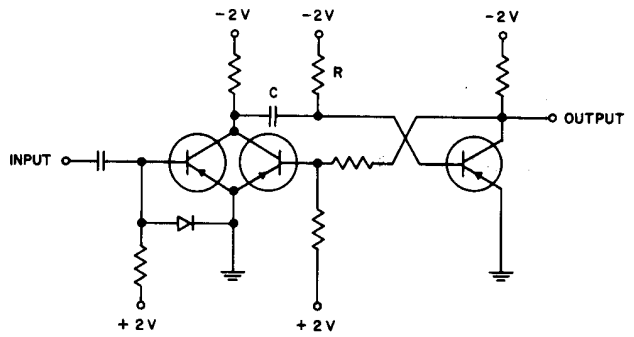
b. Standard One-Shot

Figure 7. One-Shot Multivibrator

Figure 9. Transistor OR Gate

Figure 8. AND Gate

28
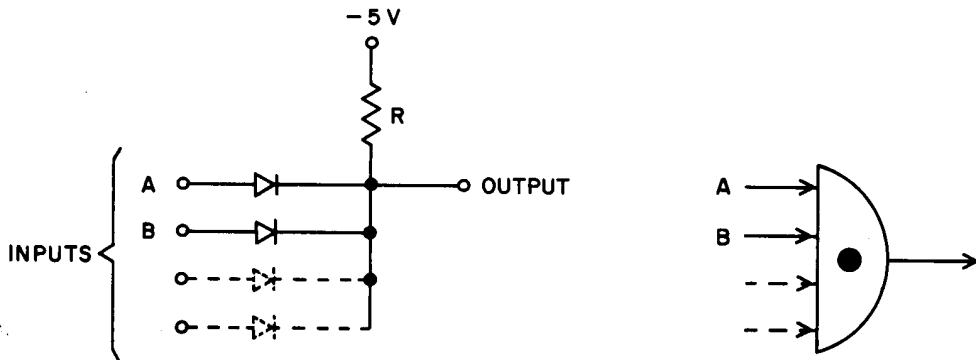
(The output pulse is a function of the RC time constant.) If the input pulse is shorter than the calculated RC output pulse, the output will be of the same duration as the input pulse; it can never be longer than the input pulse.

Logic Circuits

This section describes the operation of circuits which comprise the logical elements. Logic circuit specifications are given in figure 2.

AND Gate. A negative output (figure 8) of minus 2 volts is obtained only if all inputs are at minus 2 volts. If one or more inputs are at zero volts, the output will be zero volts.
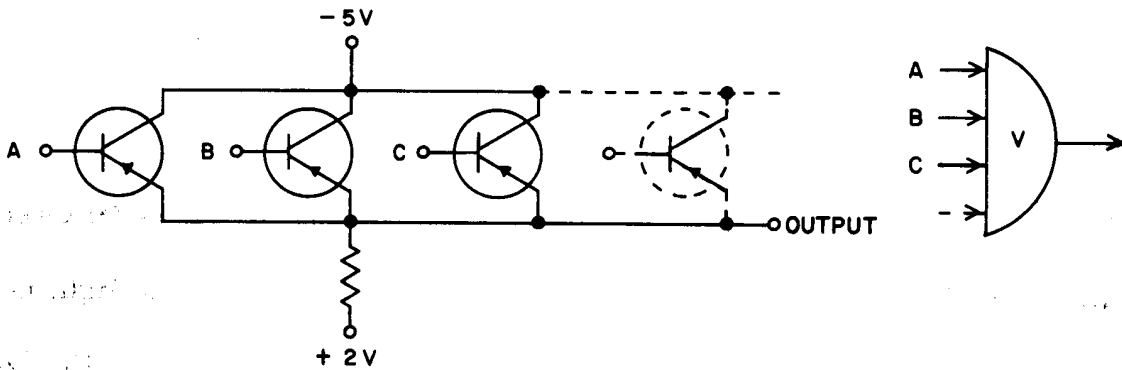
OR Gates. If one or more inputs (A, B, or C) are at minus 2 volts the output will be minus 2 volts. If all inputs are at zero volts the output will be at zero volts, figure 9 illustrates a transistor OR gate and figure 10, a diode OR gate.

Set-Reset Flip-Flop. A negative input at A of sufficient length to permit regeneration will set the flip-flop to the ONE state (figure 11). A negative input is required at B to reset the flip-flop to the ZERO state.

Complementing Flip-Flop. Complementing flip-flops are used in the address circuits. The circuit (figure 6) and description are covered under Address Circuits in this chapter.

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Figure 10. Diode OR Gate
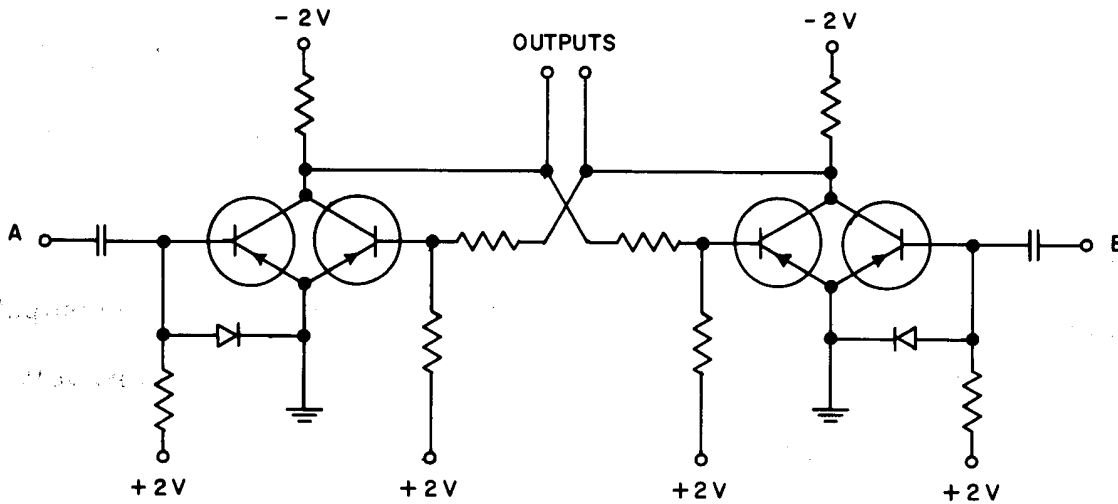
Figure 11. Set, Reset Flip-Flop
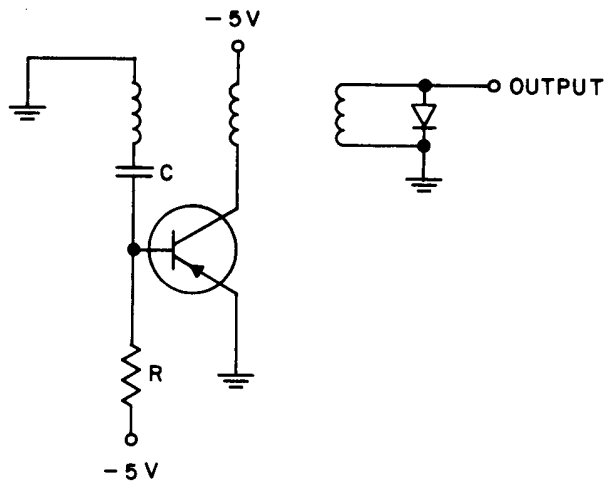
Figure 12. Master Oscillator

30

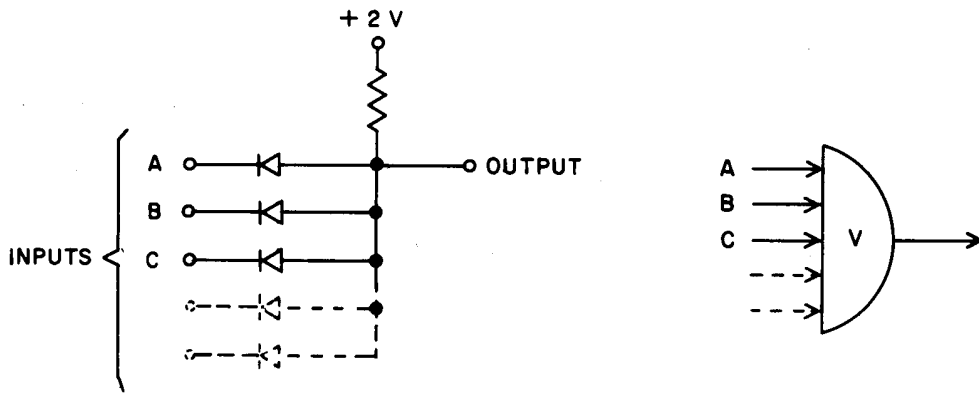**Master Oscillator.** The master oscillator is a free-running pulse oscillator (figure 12). The output pulse duration is proportional to $\frac{N\Phi}{E}$ (the number of turns in the collector winding times the magnetic flux divided by the voltage across the winding); the pulse repetition rate is proportional to the base-circuit RC time constant. A 50-microsecond pulse is produced every 176 milliseconds. An additional output winding (not shown here) is shown in the logic diagram as an inverter between the master oscillator and AND gate 13. For pulse specifications refer to table IV.

Output Buffer. The output buffer circuit consists of an integrator and three stages of current amplification. The integrator removes the short duration pulses which exist between each baud as produced by the output flip-flop. The X1 logic bias input to the output buffer (figure 3) prevents turnon of the last two stages except in the TRANSMIT and IDLE modes of operation. Drawing 4093-1005 contains the schematic of the Output Buffer.

TRANSMITTED CODE UNITS

Two types of transmission are provided, frequency shift keying (FSK) and continuous wave (CW). The type keying to be used determines the selection of adapter cords but does not otherwise affect operating procedures of the Keyer Memory itself.

Frequency Shift Keying

Spaces appear at the higher of the two carrier frequencies and marks at the lower frequency.

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Table IV. Circuit Specifications

CIRCUIT	OUTPUT PULSE	PULSE DURATION	MISC.
Oscillator[1]	2.1 V $\pm$ 0.25 V	50 μsec. $\pm$ 20 μsec.	Rep. Rate 176 msec. $\pm$ 30 msec.
11 - Msec Multivibrator	- 2.1 V $\pm$ 0.2 V	11.0 msec. $\pm$ 3.0 msec.	-
Start Buffer	- 2.0 V $\pm$ 0.2 V	50 μsec. $\pm$ 10 μsec.	-
One-Transistor One-Shot Multivibrator[2]	- 2.1 V $\pm$ 0.2 V	25 μsec. $\pm$ 5 μsec.	-
25 - Msec Multivibrator	- 4.0 V $\pm$ 0.3 V	15 msec. minimum	-
Read-Write Counter, Input Buffers	Note 3	Note 3	-
End-Around Buffer	- 2.0 V $\pm$ 0.2 V	15 μsec. $\pm$ 5 μsec.	-
Address Flip-Flop	- 0.3 V, $\pm$ 0.2 V or - 5.2 V, $\pm$ 0.3 V	-	-
Address Circuit "A"	+ 3.5 V $\pm$ 0.4 V	300 μsec. $\pm$100 μsec.	-
Sense Amplifier[4] (Input 40 to 150 mv)	- 2.0 V $\pm$ 0.2 V	1.5 μsec. $\pm$0.5 μsec.	Strobe Output -2.0 V, $\pm$ 0.2 V 2.5 μsec. $\pm$0.5 μsec.
Indicator[5]	Visual Indication	-	-
Output Buffer	50 ma. (to load RT-6)	-	-

Notes:
1. One positive and one negative output pulse.

2. This circuit follows the 11-msec. multivibrator.

3. Inversions of the output of the one-shot multivibrator which follows the first 11-msec. multivibrator.

4. Maximum input noise (for no output) is 24.0 mv. Minimum input signal required is 40.0 mv.

5. Requires input of -2.0V, 10 msec. minimum. Minimum voltage required across indicator light is 1.1 volt.

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Figure 13 shows the frequency-shift characteristics of CR-18 and CR-27 crystals. Although the amount of shift varies between different units cut to the same frequency, a given crystal can be expected to retain a given approximate shift permanently. Number CR-18 or CR-27 crystals have been encountered which display frequency shift of too small a value for reception on standard equipment. When doubling or tripling in the transmitter the frequency shift transmitter will be correspondingly doubled or tripled and shifts as great as 3000 cps could result. One method for receiving shifts greater than 1000 cps is to zero-beat the receiver BFO on the "mark" carrier frequency and treat the result as if it were CW keying. Another method is to set receiver selectivity to minimum value and tune in on the mark carrier. Perhaps the best practice is to pre-check the desired crystals for shift, and if doubling or tripling would cause shifts greater than 1000 cps, use the CW Adapter Cord for transmitting. Use of CW keying would not provide the 3 db advantage of FSK.

The frequency shift of the transmitting crystal does not vary with the battery voltage of the Keyer Memory, but ±10 percent voltage fluctuations of the transmitting power source may cause variations of ±2 percent.

CW Keying

The transmitter is keyed off only during spaces and remains on during marks.

Adapter Cord Operation

Both the FSK and CW adapter cords contain semiconducter circuits within the black plastic encapsulation and should be regarded as parts of the Keyer Memory.

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CRYSTAL FREQUENCY (MEGACYCLES)

SHIFT (CYCLES)
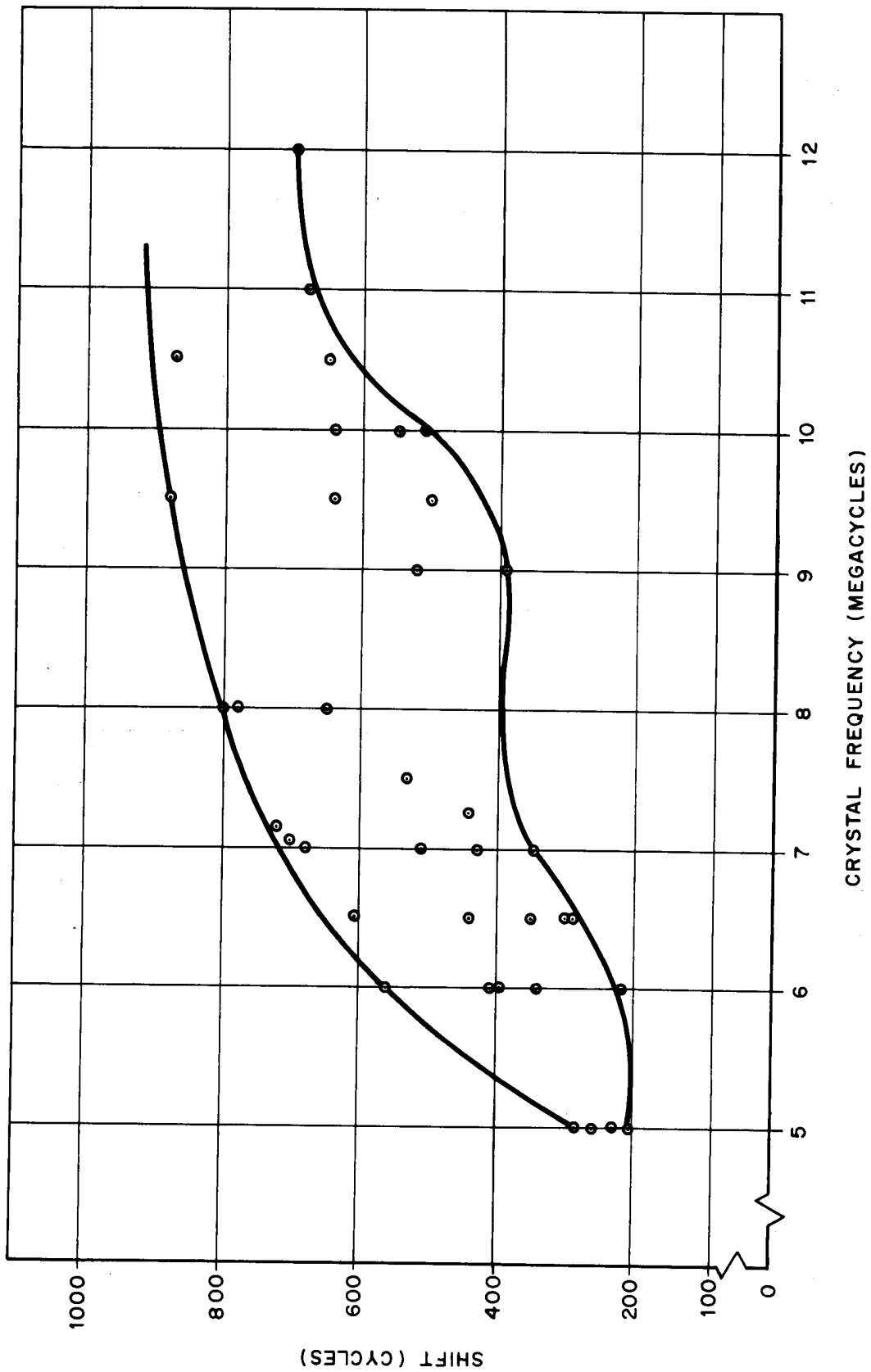
Figure 13. Frequency Shift Characteristics

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FSK Adapter Core. A Varicap semiconducter diode is paralleled through a small capacitor with the transmitting crystal (figure 14). During transmission of a space, a d-c voltage, obtained from rectification of rf by the Varicap itself is permitted to appear across the Varicap. This voltage, whose magnitude is limited to about 10 volts by a resistor, causes the Varicap to assume minimum capacitance. During a mark, the output amplifier shorts the d-c voltage through an r-f choke, thereby increasing the varicap capacitance and dropping the crystal frequency.

CW Adapter Cord. When the CW adapter plug is inserted in the KEY JACK of the transmitter, certain cathode returns in the transmitter are broken and placed in series with the silicon power transistor in the adapter plug (figure 15). During a mark, this transistor is saturated by current from the output amplifier, keying the carrier on. During a space, the transistor is cut off. This interrupts the cathode returns in the transmitter, keying the carrier off.

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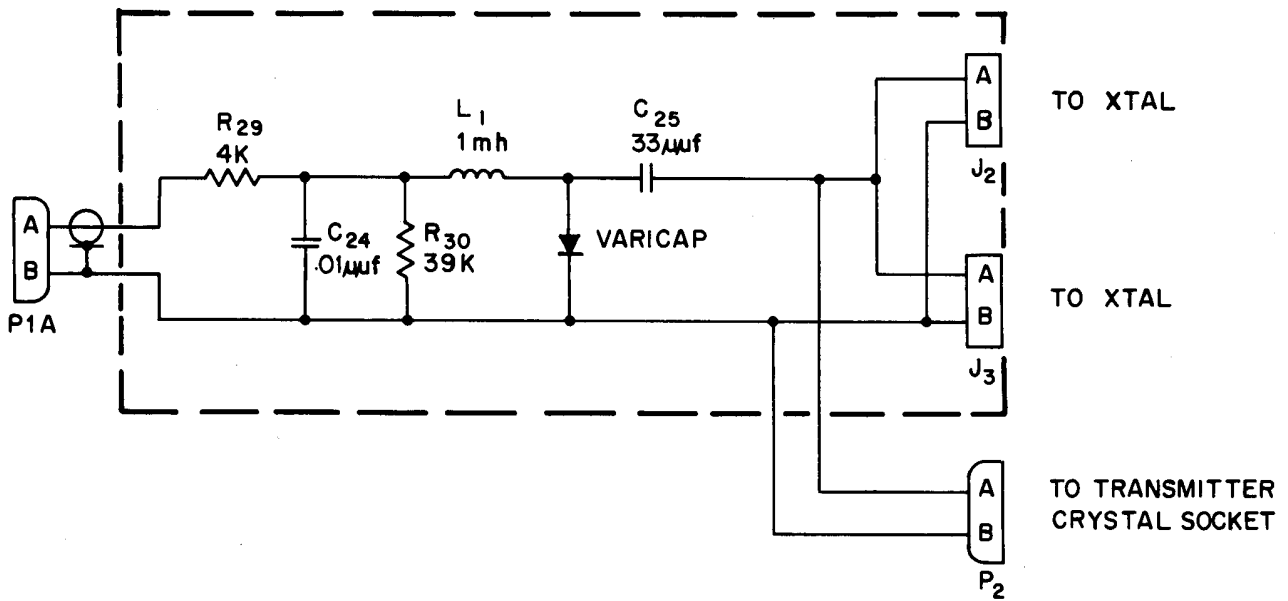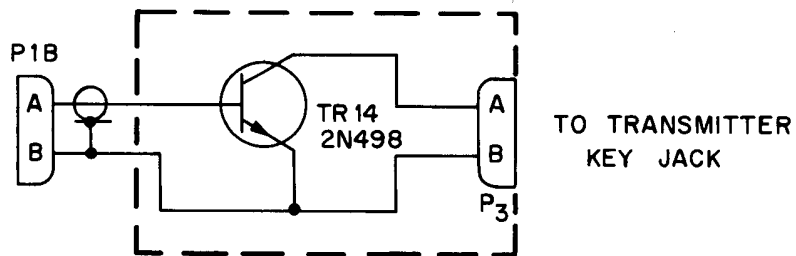Figure 14. FSK Adapter Cord Circuit

NOTE: P_3 IS A MODIFIED PL-55 TYPE PLUG

A = TIP, B = SLEEVE

Figure 15. CW Adapter Cord Circuit

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SECTION III

MECHANICAL DESIGN

The entire Keyer Memory is contained within a single metal case (figure 1). All operating necessities are mounted on the cover and are secured to the underside of the cover with the exception of the cable plug receptacle which is secured to the side of the cover, and the battery mount which is secured to the top of the cover.

DESIGN CONSIDERATIONS

The Keyer Memory was made to the present mechanical configuration for the reasons following. When the packaging design was initiated late in 1959 the circuitry had not been entirely defined in terms of components and component values. The smallest commercially available components and special mechanical parts, printed circuit, and memory and interconnecting wires were used so that characteristics of these components could be evaluated. It was considered desirable to arrange circuitry on printed circuit boards in organized groups closely related to one another, but not to develop many small modules which would entail excessive interconnecting circuitry. To attain desirable packaging density the decision was made to stack components on each printed circuit board to a depth equal to the thickness of the largest single component (approximately 0.1875 inch). In planning component locations on a board, consideration was given to sufficient space for the use of heat-sink tweezers and thin soldering-

37
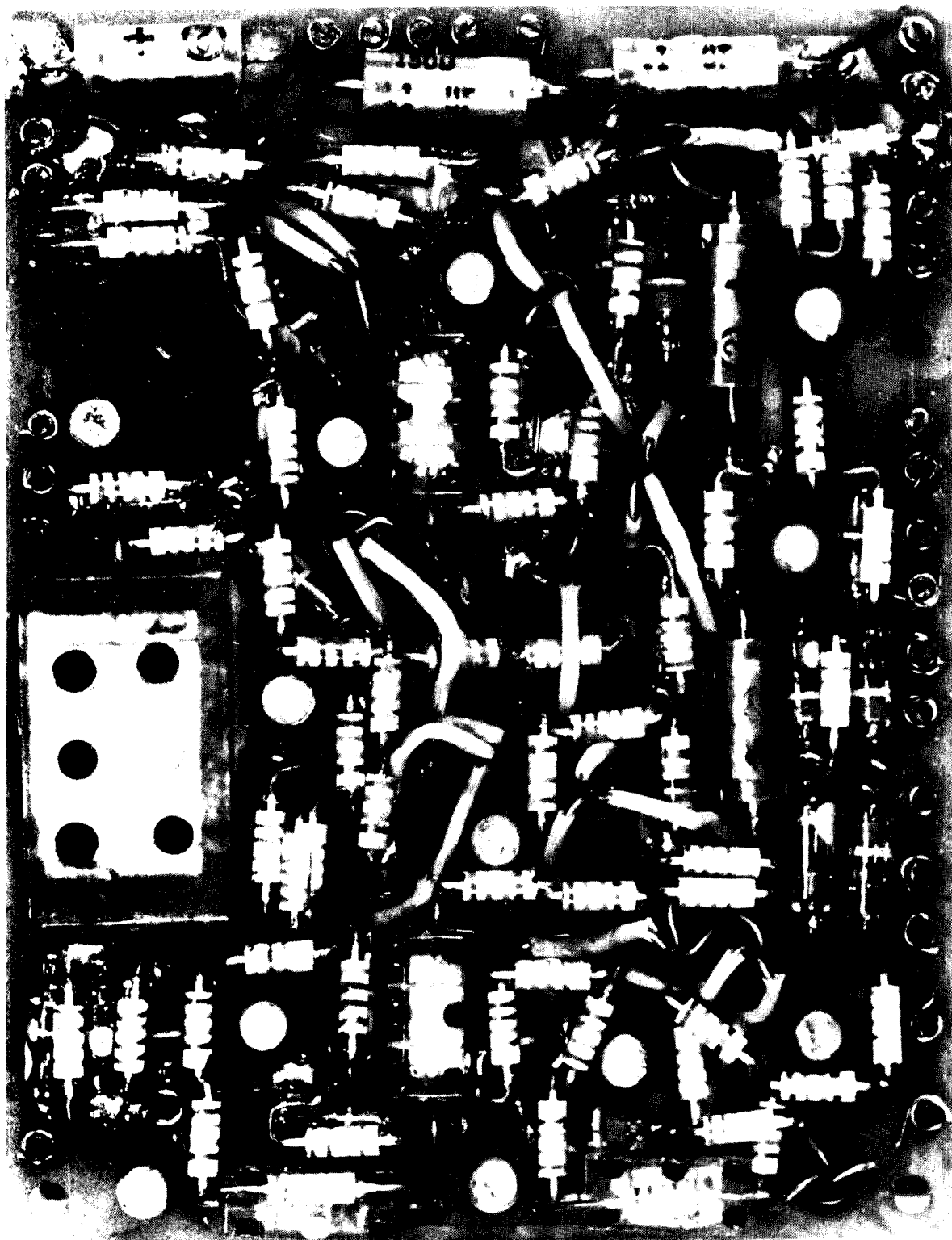
Figure 16. Keyer Memory Printed Circuit Card

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iron tips during assembly. Printed circuit boards were planned as large as practicable to reduce the number of boards and the number of interconnections between boards.

The present form of the Keyer Memory may be described as a hybrid, semi-modular, organized-circuit design. Random interconnections were provided between the distant points of circuitry. Component boards were originally to be 0.031-inch thick to conserve space but warpage during soldering was sufficient to defeat this purpose. Therefore, boards made after 1 May 1960 are 0.062-inch thick: figure 16 shows the high package density of a printed circuit board.

COVER

The cover can be removed from the case by removing the retaining screws and lifting the cover off. The following items are attached to the cover and can be seen when the cover is removed:

1. Mode selector switch assembly.

2. Cable-plug receptacle, with case grounding lug.

3. Indicator light assembly.

4. Keyer assembly.

5. GO and CLEAR pushbutton assemblies.

6. Power supply oscillator board.

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Battery Mount

The battery mount, located on top of the cover, has been designed to fold flat against the cover when the batteries are removed; the ends of the mount (when folded) should be locked in place with the slides provided for the purpose. Battery polarity is inscribed on the battery mount.

Mode Selector Switch

This switch was designed as a flat, 5-position slide switch to save space. Careful consideration was given to selection of contact material to ensure a reasonable long operating life. The moveable portion of the switch is a notched shaft or stem, which is pushed into or pulled out of the Keyer Memory to select the desired mode of operation. Contact fingers attached to the shaft make connection with contacts on the printed circuit portion of the switch. These contacts are rhodium plated, contact fingers on the shaft are gold plated. Markings on the shaft indicate the mode position.

Cable Plug Receptacle

The plug receptacle used with the Keyer Memory is a duplicate of the model furnished by the customer and is located on the side of the cover. The plug can be inserted only in a manner ensuring proper polarity.

Indicator

The indicator consists of a miniature incandescent low-voltage lamp housed within a plexiglass body. The plexiglass body has been designed to provide maximum illumination through the convex lens on top.

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Keyer

Keyer switches used were furnished by the customer and are recessed in the cover. Conservation of space, ease of operation, and accessibility for wiring were factors determining their location on the cover.

Go and Clear Switches

These are miniature pushbutton switches. To avoid projection above the top surface of the Keyer Memory, these switches have been recessed in the cover.

CASE

The remaining assemblies of the Keyer Memory are contained within the case. Because of machineability, ease of soldering, and ability to take a good finish coating, brass was selected as the case material. Assemblies within the case are shown in figure 17 and consist of:

1. Sense amplifier and associated circuit board.

2. Memory assembly.

3. Address boards assembly.

4. Power supply board.

5. Logic boards assembly.

All of the assemblies are fastened either to one another or to the case and are interconnected in a manner permitting limited disassembly for test purposes. Where necessary, either mylar or silicon-rubber sheets have been positioned between assemblies to prevent possible short circuits. Where required, sensitive circuits

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MEMORY BLOCK CONTAINING:

3 — DIODE MATRIX BOARDS

3 — SWITCH AND DRIVER
        BOARDS

1 — PULSE GENERATOR &
        KEYER BOARD

1 — CORE MATRIX ASSEMBLY

2 — LOGIC CIRCUIT BOARDS

SENSE AMPLIFIER
OUTPUT BUFFER
INDICATOR

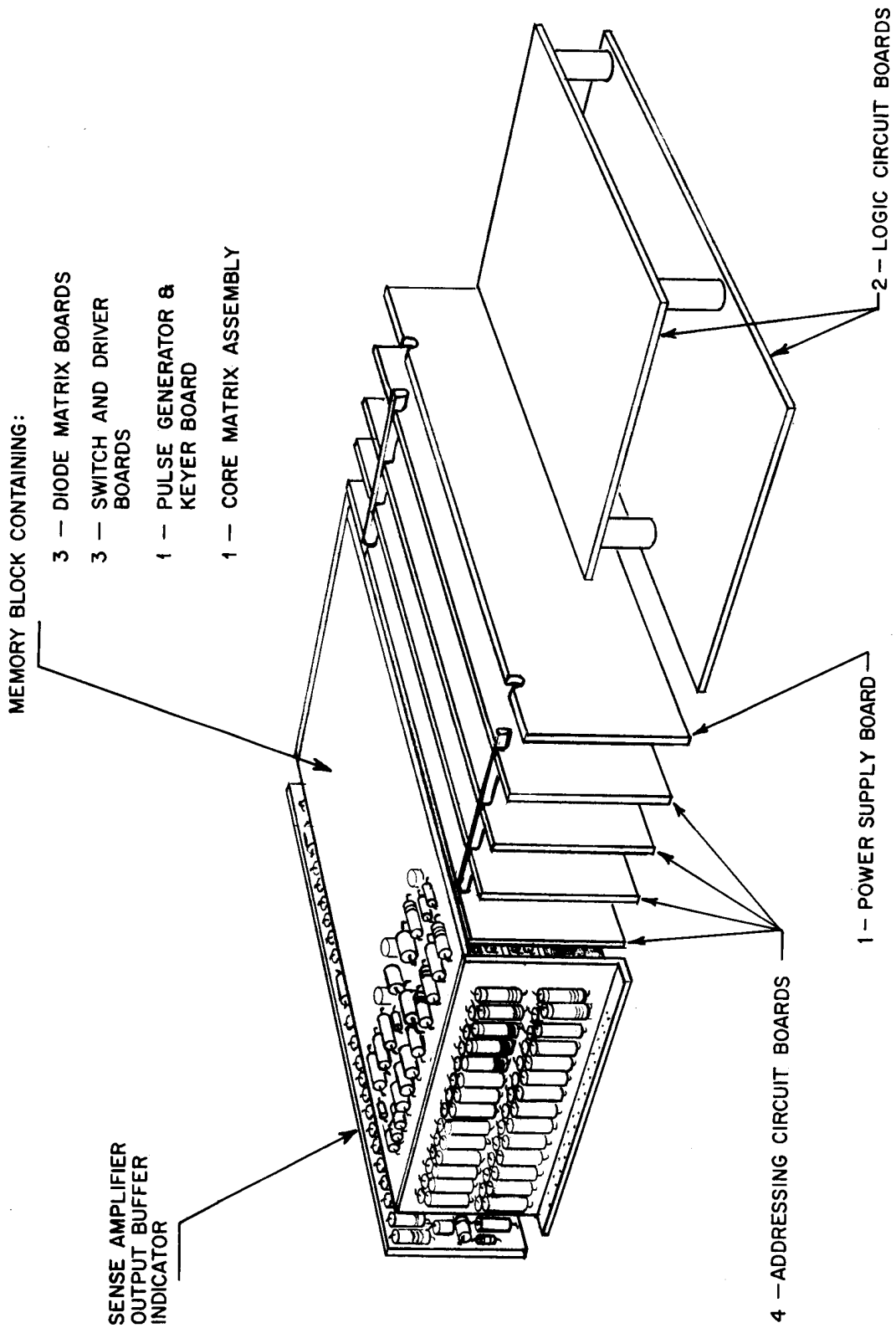1 — POWER SUPPLY BOARD

4 — ADDRESSING CIRCUIT BOARDS

Figure 17. Arrangement of Printed Circuit Cards

42

have been shielded by thin foils of special metal to prevent magnetic noise or high-frequency radiation which might affect performance. Connections between assemblies are made with insulated wire. The function and operation of the circuits of these assemblies are described under CIRCUIT DESIGN.

The memory assembly consists of the memory matrix, the board containing the Y switches and drivers, the two boards containing the X switches and drivers, and the board containing the pulse generators and keyer circuits is located on the top of the assembly. Figure 18 shows the configuration of the memory and its connections to the printed circuit boards and figure 19 shows a wired memory stick.
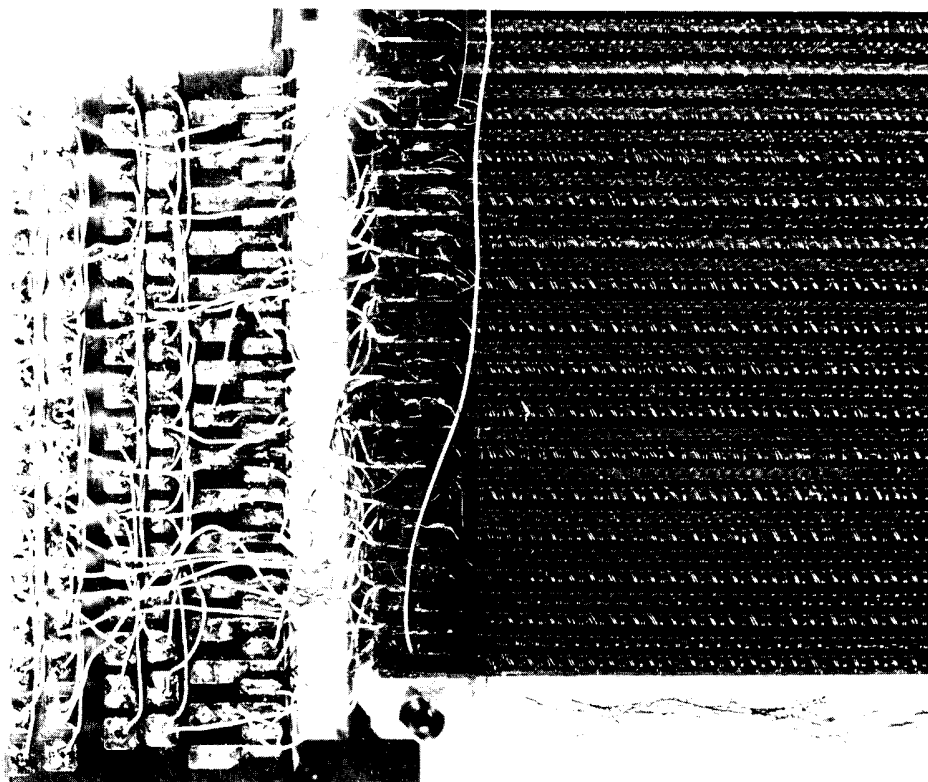
43

Figure 18. Assembled Memory with Connections to Printed Circuit Boards

Figure 19. Wired Memory Stick

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SECTION IV

CONCLUSIONS AND RECOMMENDATIONS

The Keyer Memory was designed as a working prototype, around components and circuitry of known reliability. While not fabricated to pass any stringent MIL tests, it was designed with MIL specifications in mind, especially in choice of components. Continued satisfactory operation is expected within the temperature range specified under CIRCUIT DESIGN.

Last-minute changes, dictated by improvements made in circuit design, caused excessive component density in the areas of the sense amplifier circuit board and the circuit board containing the pulse generators. Packaging in these areas should be improved.

Recommendations made in the following discussions should result in a Keyer Memory which is even more compact, reliable, and rugged. Time and funds did not permit incorporation of these improvements into the prototype Keyer Memory. Recommendations should be evaluated on the basis of the number of additional units required and conditions under which the units will be operated.

45

BATTERY MOUNT

The battery mount is of conventional design and involves the use of individually installed, loose batteries. These loose batteries could deteriorate before being put into use. It is recommended that a special plastic case be provided which can be opened for recharging and inspection and which can be plugged, as a unit, into a connector on the cover. This would permit a more dust-proof and water-tight construction.

MEMORY

The memory matrix should be redesigned to provide a simpler and less costly method of assembling cores into strips. Redesign should also include more rugged core windings, connections to core windings which are more readily accessible and easily soldered, and a more positive method of assembling core strips into a matrix.

CIRCUITS

The use of more silicon transistors, although expensive, would result in a reduction in leakage current. This would in turn result in a reduction in the number of clamping diodes required. The net result would be reduction of over-all current requirements, a reduction in the component count, and simplification of some of the circuitry. Miniature flexible circuitry could be used between individual assemblies for increased reliability.

Redesign might include development of a number of modular subassemblies to be used for individual circuits which are repeated a sufficient number of times to make modularization economical.

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It is recommended that circuits be physically revised to reduce connections and thereby reduce joint failures during assembly and operation. All printed circuit boards should be of 0.062-inch-thick laminated material for increased rigidity. Printed circuit board assemblies should be revised to take advantage of physically smaller components which are becoming commercially available. Diode boards, for example, could be redesigned to take advantage of microdiodes and simplify the complex wiring connections. Revision of board assemblies would result in considerable reduction of board area without an increase in assembly cost or a loss in reliability. An alternate approach to revision could be utilization of Bimag[*] (magnetic core) circuits which would simplify circuit design, increase reliability and possibly result in a reduction of volume.

If the unit is to be capable of satisfactory operation under adverse field conditions, ultimate redesign should be combined with an extensive test program. This would ensure that each component, circuit, assembly or module, and the entire unit is capable of meeting applicable MIL specifications.

CASE

The case for the first unit was made of brass to permit last minute modifications. These modifications were unavoidable because of the limited design time allotted to the entire project. The case was large for the same reason. Cases of future units

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[*]A Burroughs-developed bistable magnetic-core technique

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can be made smaller and of aluminum or another lighter material. If results of r-f radiation studies permit, the case may be made of a suitable plastic. Redesign will include consideration of molding or diecasting. Preliminary studies of redesign of the memory and diode matrix for greater reliability and ease of assembly and test, and of address and logic circuits for Bimag (magnetic core) application, indicate the possibility of at least 12.5-percent reduction in case volume.

COVER AND KEYER

The present layout of the cover indicates the availability of space for a larger keyboard (which would undoubtedly be easier to operate). The keyboard, as furnished by the customer, is too compact to permit satisfactory manipulation of keys and it is neither dust nor moisture proof. No provisions have been made for attachment of the keyboard to the case as an assembled unit. It must be disassembled and attached to the case piece by piece. This creates difficulty in making the necessary alignment and in ensuring proper tension of each contact spring.

Tests of the keyer contact assembly disclosed a great degree of unreliability caused by ganging of weak contacts in close proximity on a common plate which is easily affected by changes in tension of mounting screws. Contact springs are too weak to properly support and return the keys. Spring strength decreases rapidly, resulting in a change in length of the operating stroke. In addition, the bodies of the keys are too short for the travel required to operate most of the contact springs. It is recommended that the keyboard be redesigned for more satisfactory operation, greater reliability, and consideration of human factors principles.

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5-POSITION SWITCH

Design criteria for this switch is based on the utilization of the small volume available for the switch within the present case. The present switch is neither dust nor moisture proof and its reliability has not been determined. Because of the importance of this switch to the overall operation it should be redesigned for reliability and ease of use.

GO AND CLEAR MOMENTARY CONTACT SWITCHES

These switches were obtained through commercial channels and were selected for their small size and reliability. Some thought should be given to a selection of more rugged switches, because of the importance of these switches to the performance of the Keyer Memory.

PLUG RECEPTACLE

This device is basically the same as that used in the customer's sample and was used without modification because it must be mated with the customer's plug. It should be redesigned to provide a dust and moisture proof connection.

INDICATOR

At present, there is no means for indicating when the memory is full or nearly so. With some redesign and the addition of several components (dependent upon the desired stopping place) a steady light indication could be provided at any character, for example character 635. This would inform the operator that he was close to filling the memory and would aid in preventing overfilling of the memory.

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An additional bulb, paralleled with the present bulb, would have two advantages. First, more light would be provided which would alleviate the present situation where indications may be missed due to insufficient light. Second, a fail-safe would be provided if one bulb failed. The use of an additional bulb would require some redesign and would be an additional drain on the power supply.

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APPENDIX I

DESIGN CRITERIA

Design criteria presented here covers core-switching currents, temperature compensation, drive line voltages, and logic circuits. Logic circuit design criteria applies to the switching amplifier and timing circuit.

CORE SWITCHING CURRENTS

In establishing criteria for core switching currents it was first necessary to make certain assumptions. The basic circuit used in establishing criteria is shown in figure I-1. Assumptions made were:

1. Initial adjustment of R_e with respect to the plus 5-volt supply will give a total error of plus or minus 2 percent.

2. Parameters V_{be2} and V_{ce1} vary oppositely with temperature changes. The difference between these parameters can be incorporated in calculation of the temperature coefficient of R_e but can be disregarded when considering design tolerances.

Based on these assumptions

$$I_{c2} = \frac{(5v - V_{be2} - V_{ce1})\alpha2}{R_e} \tag{1}$$

I-1

and load current

$$I_L = I_{c2} \, \alpha 3 \qquad\qquad (2)$$

Using

$$\delta \, (V_{be2} \text{ and } V_{ce1} = \pm \, 3 \text{ percent}$$

$$\delta \, \alpha 2 = \pm \, 2 \text{ percent}$$

$$\delta \, \alpha 3 = \pm \, 2 \text{ percent}$$

$$\text{initial adjustment of } R_e = \underline{\pm \, 2 \text{ percent}}$$

the total $\delta \, I_L$ will be $\qquad \pm \, 9$ percent.

If in design the maximum noise currents are equal, and if

$$I_X = I_y = I_2$$

and

$$I_{bias} = I_1 \qquad\qquad (3)$$

then

$$\overline{I}_1 = \overline{I}_2 - \underline{I}_1$$

shown mathematically as

$$I_1(1.09) = I_2(1.09) - I_1(0.91)$$

$$2I_1 = 1.09 \, I_2$$

$$I_1 = \frac{1.09 \, I_2}{2}$$

$$= 0.545 \, I_2.$$

I-2

Minimum signal current therefore, is

$$I_s = 2 \times I_2 - \overline{I}_1$$

$$I_s = 2(0.91\ I_2) - 1.09\ (\frac{1.09}{2})\ I_2) = 1.226\ I_2, \tag{4}$$

maximum noise current is

$$\overline{I}_n = \frac{1.09}{2}\ (1.09\ I_2) = 0.595\ I_2, \tag{5}$$

and the worst-case signal-to-noise current ratio is

$$\gamma = \frac{1.226\ I_2}{0.596\ I_2} = 2.06 \tag{6}$$

TEMPERATURE COMPENSATION

To maintain a constant core output over the temperature range of minus 40 degrees Centigrade to plus 50 degrees Centigrade, the drive currents are required to have a temperature coefficient of minus 0.45 percent per degree Centigrade.

The change in drive current caused by the effect of temperature variation on V_{be} (figure I-1) is 0.045 percent per degree Centigrade. The change in drive current caused by the effect of temperature variations on the plus 5-volt supply is minus 0.022 percent per degree Centigrade. Therefore R_e must have a temperature co-efficient of $- 0.45 + 0.045 - 0.022 = 0.022 = - 0.473$ percent per degree Centigrade. Assuming R_1 in parallel with it has a temperature coefficient of zero, then
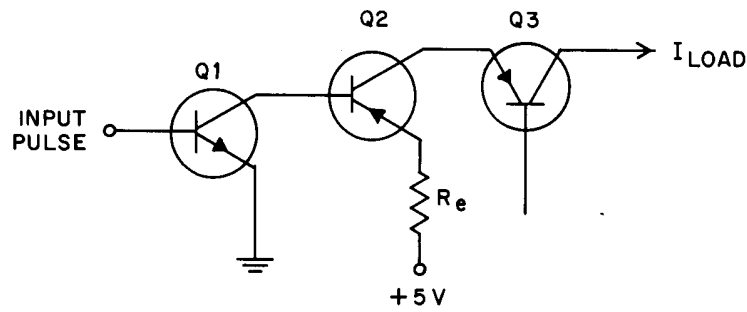
I-3
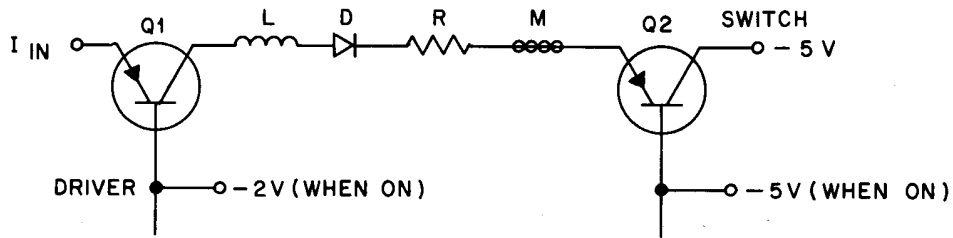
Figure I-1. Switching Current Analysis Circuit

Figure I-2. Drive Voltage Analysis Circuit

$$\frac{R_1 R_2}{R_1 + R_2} \div R_2 = \frac{0.473}{0.545} \tag{7}$$

making

$$R_1 = 6.57 \ R_2$$

If R_2 is two 68-ohm sensistors in parallel (34 ohms), than

$$R_1 = 6.57 \times 34 = 220 \text{ ohms}$$

DRIVE VOLTAGES

Drive voltage criteria is based on the circuit configuration of figure I-2. This cir-cuit is representative of a word line of the memory.

Drive lines can be defined as having:

line inductance, $L = 0.75$ microhenries

series resistance, $R = 2.0$ ohms

core voltage per line $V_M = 0.465$ volts

diode voltage, $V_D = 0.8$ volt during steady-state conduction and

$= 1.0$ volt transient

V_{be} of transistor $Q_2 = 0.7$ volt during steady-state conduction and

$= 1.0$ volt transient.

With a load current, I_L, of 150 milliamperes with a 0.15-microsecond rise time

$$V_L = 0.75 \times 10^{-6} \times \frac{150 \times 10^{-3}}{0.15 \times 10^{-6}}$$

$$= 0.75 \text{ volt}$$

and

$$V_R = 0.3 \text{ volt.}$$

Under transient conditions the voltage drop across the word line is

$$V_{drop} = V_{be(tran)} + L \frac{di}{dt} + V_{0(tran)}$$

(8)

$$V_{drop} = 1.0 + 0.75 + 1.0 = 2.75 \text{ volts,}$$

and steady-state voltage drop across the word line is

$$V_{drop} = I_R + V_M + V_D + V_{BK}$$

$$V_{drop} = 0.3 + 0.465 + 0.8 + 0.7 = 2.3 \text{ volts.}$$

Therefore, the use of minus 2 volts on the driver and minus 5 volts on the switch results in a worst-case driver line voltage (allowing for tolerances) of

$$4.8 - 2.1 = 2.7 \text{ volts.}$$

This is an acceptable value.

LOGIC CIRCUITS

Logic circuit criteria explained here applies to the switching amplifier and timing circuit. These are basic building blocks for the logic circuits covered in other chapters of this report.

I-6

Switching Amplifier

The basic switching amplifier circuit is shown in figure I-3. In this circuit, where load current always flows out of the amplifier, R_c is required only to absorb transistor I_{co}.

The value of R_c is calculated under conditions when the transistor is off, as

$$R_c = 3v \div I_{co}.$$

When the transistor is on load current can be calculated as

$$\overline{I}_{load} = 5v \div R_c + I_{s(diode)} + \frac{5v}{R_{load}} \tag{10}$$

Minimum base current is then calculated as

$$\underline{I}_b = \overline{I}_L \div \underline{\beta} \tag{11}$$

The value of the base biasing resistor (R) is calculated to be capable of supplying maximum I_{co} from base to collector when the transistor is off.

Timing Circuit

The basic timing circuit is shown in figure I-4. This is the basic building block around which the logic timing circuits were designed.

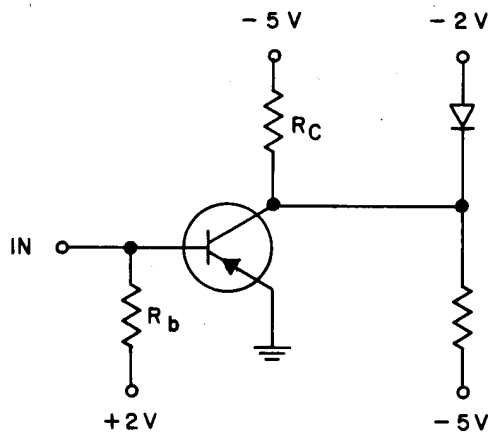With load current equal to

$$\overline{I}_L = 5v \div \underline{R}_L$$

I-7

CONFIDENTIAL

Figure I-3. Switching Amplifier
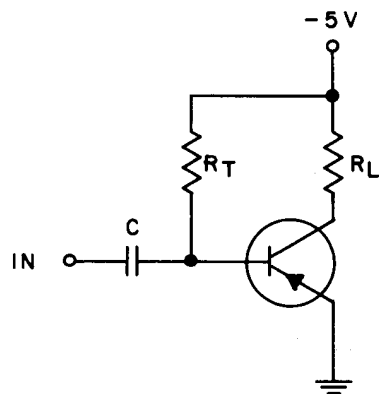
Figure I-4. Timing Circuit

I-8

CONFIDENTIAL

CONFIDENTIAL

Base current

$$I_b = I_L \div \underline{\beta}$$

then

$$\overline{R}_T = 5v \div \overline{I}_b. \tag{12}$$

For a given input voltage (V_{in}) and neglecting the base-to-emitter diode drop of the transistor

$$V_{in} = (5 + V_{in})(1 - e^{\frac{t}{R_T C}}) \tag{13}$$

$$e^{\frac{t}{R_T C}} = \frac{5 + V_{in}}{5}$$

and

$$t = R_T C \, \ell n \, \frac{5 + V_{in}}{5} \tag{14}$$

Since the leakage (base to collector) is relatively high in germanium transistors, silicon transistors are used where accurate timing is required. Where timing accuracy is not as critical, germanium transistors are used and the base current is set to at least four to five times greater than I_{co} so that variations in this current do not adversely affect the timing.

CONFIDENTIAL

I-9