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Third Bimonthly Report on the RT-21 Transmitter Development

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I. Purpose

See Bimonthly Report No. 1.

II. Abstract

In this report an account is given of a brief investigation which was carried out to determine whether, by utilizing the avalanche breakdown phenomenon in transistors, it would be possible to obtain relatively high output powers at high frequencies from low frequency transistors.

During the past reporting period work has been continued in the areas of antenna matching and automatic tuning of the transmitter. The former activity has been largely of an analytical nature directed towards determining the suitability of various transformation networks for this application. Efforts have been made to devise impedance transformation methods which do not either lead to impractically large maximum to minimum capacitor ratios, impractically small or large values of inductance or capacitance, or inherent circuit losses comparable to the loss which would be experienced if no attempt was made to match the transmitter to the antenna. Several configurations have been studied, all except one of which have been found unacceptable. In this report a description of the various configurations is given as well as the reasons which make them unacceptable. A variable transformer method is described which appears, at the present time, to lead to a far more practical solution than the other approaches.

Towards the end of this reporting period a visit from the customer revealed a change in antenna matching requirements. The new requirements change the problem materially; however, at the time of writing, the full significance had not been determined.

Associated with the matching network is the sensing circuitry which is required in order to indicate when a properly matched condition exists. This report includes a description of the work which has been done in the area of both magnitude and phase sensing circuitry.

The transmitter tuning problem has been described in earlier reports. In this report a description is given of the steps which have been taken in order to insure that the range of frequencies over which the electrical tuning system operates corresponds to the maximum that the voltage variable capacitors are capable of providing. It is clear that small improvements in available electrically variable capacitors will not alter the picture sufficiently to permit the whole range from 3 mc. to 15 mc. to be covered in one band. An electronic switch has consequently been developed which will permit taps to be moved electrically making possible automatic tuning over the whole range using presently available voltage variable capacitors.

During the past month several high power-high frequency transistors have become available. In particular, the Texas Instrument 2N1141 shows considerable potentialities. This transistor does not approach the output stage requirements for the RT21 transmitter but makes possible the design of a relatively high power oscillator stage. If the output transistors which are ultimately used have a reasonable power gain, the 2N1141 would probably be suitable as a driver stage. Using these transistors, the crystal oscillator has been redesigned to provide a higher output than was possible using 2N247 transistors. By increasing the oscillator output level, the total number of stages can be reduced with a consequent reduction in the number of tuned circuits with their associated control circuitry.

A circuit has been designed which enables the band from 3-15 mc. to be swept in three ranges with automatic switching of coil taps for each range. The 15-30 mc. range is covered without the necessity for switching coil taps, representing a maximum to minimum frequency ratio within a range of only 2:1. The switching circuit has been built in preliminary form and operated successfully. At the conclusion of the present reporting period it had not been integrated with the remainder of the transmitter circuitry.

III. Factual Data

1. Power Output

(a) Introduction

The problem of obtaining 10 watts of R.F. power from a transistor circuit is a function of the transistor device itself. The transistor device art is slowly moving to high power R.F. units. However, a technique has been devised that utilizes the avalanche multiplication effect of low frequency transistors to produce high frequency-high current pulses. Avalanche multiplication in transistors is analogous to a gas discharge tube where charge carriers are accelerated in a high electric field to a high speed. When they collide with other molecules, more carriers are produced in the collision.[1,2] This phenomena has been utilized to produce very narrow pulses (approximately 1 m μs wide) with an amplitude of about one ampere.

The formation of a very narrow pulse is dependent upon the switching time of a device. It has been shown that a transistor operated in the avalanche mode can be used to discharge a capacitor in a very short time. If it is possible to produce these pulses at a repetition rate of 30 mc., a suitable power

amplifier can be produced.

(b) Circuit[3]

As a voltage V_{cc} is applied to the circuit shown in Figure 1, capacitor C will charge through R_L to a value approaching V_{cc}. If $I_b R_b < V_{bb}$, the circuit will be stable with $I_b = I_c$ and $I_E = 0$. If the base is then triggered with a negative pulse, the emitter to base diode will be forward conducting and C will discharge through the nominally zero impedance transistor to ground. This pulse of current flowing out of C can then be coupled to a load through some appropriate coupling network.

The maximum repetition rate of the avalanche mode is limited by the average collector dissipation of the transistor. The capacitor is charged to a voltage V_B, equal to the avalanche potential of the transistor, and the power dissipated is P_d. Since the discharge time is negligible compared to the charging time of C through R_L, the transistor dissipates energy during a time, T, that can be calculated as follows:

$$V_{cc} = V_B \left(1 - e^{-\frac{T}{R_L C}}\right)$$

$$\text{or} \qquad T = CR_L \ln \frac{V_{cc}}{V_{cc} - V_B}$$

The average power dissipation over one cycle is:

$$P_d = \frac{CV_B^2}{2T}$$

$$= \frac{V_B^2}{2R_L} \cdot \frac{1}{\ln \frac{V_{cc}}{V_{cc} - V_B}}$$

During the non-conducting quiescent state a collector current, I_c, will flow

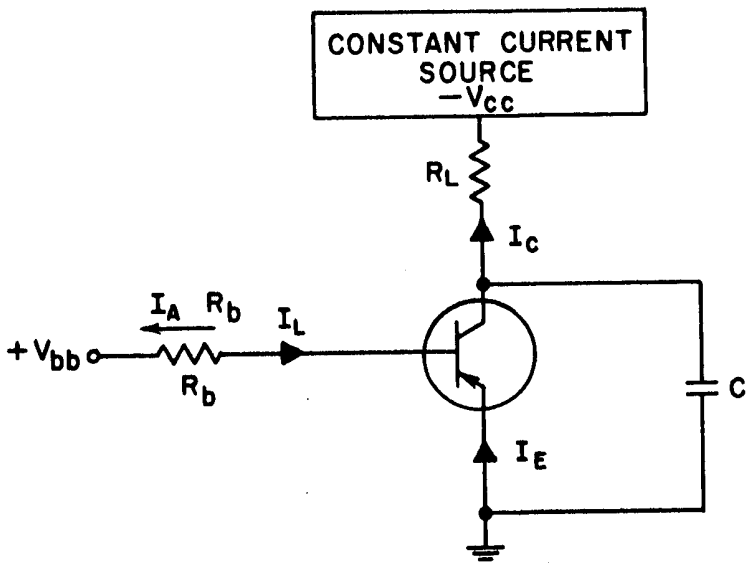


FIGURE 1

which is:

$$I_c = \frac{V_{cc} - V_B}{R_L}$$

The dissipation during this time is P_q which is:

$$P_q = I_c V_c = I_c V_B = \frac{V_B (V_{cc} - V_B)}{R_L} = \frac{V_B^2}{R_L} \left(\frac{V_{cc}}{V_B} - 1\right)$$

Hence,

$$\frac{P_q}{P_d} = 2(r-1) \ln \frac{r}{r-1}$$

where $$r = \frac{V_{cc}}{V_B}$$

This equation represents the compromise between battery voltage and collector dissipation that must be realized.

From a consideration of the average power the maximum repetition rate, f_{max}, can be determined.

$$f_{max} = \frac{1}{T_{min}} = \frac{2P_d}{CV_B^2}$$

If we assume that the current pulse is in the form of a half sine wave the peak current flowing can be calculated from:

$$\frac{2}{\pi} I_{peak} \, t = CV_B$$

(c) Numerical Application

If a 10 ohm load were placed in series with the capacitor C and

we wished to dissipate 10 watts in this load, a current of 1 A_{rms} or 1.4 A_{peak} must flow. Experiments with germanium transistors indicate that the avalanche potential, V_B, is about 50 volts. Using the equation

$$\frac{2}{\pi} I_{peak}\, t = CV_B$$

and assuming $t = \frac{1}{40 \text{ mc.}} = \frac{10^{-6}}{40}$

$$C = \frac{2}{\pi} \frac{I_{peak}\, t}{V_B}$$

$$C = 450 \text{ } \mu\mu f$$

Using this value of C and a $f_{max} = 40$ mc.

$$P_{max} = \frac{CV_B^2}{2T}$$

$$= \frac{(450)(10^{-12})(50)^2(40)}{(2)(10^{-6})}$$

$$P_{max} = 22.5 \text{ W}$$

The value of R_L can now be computed from

$$R_L = \frac{V_B^2}{2P_d} \frac{1}{\ln \frac{V_{cc}}{V_{cc}-V_B}}$$

$$= \frac{(50)^2}{2\,(22.5)} \frac{1}{\ln \frac{105}{105-50}}$$

$$= 99.4 \text{ ohm}$$

$$R_L \cong 100 \text{ ohms}$$

These results can be summarized:

R_L = 100 ohm

C = 450 $\mu\mu$f

V_{cc} = 105 Volts

V_B = 50 Volts

P_d = 22.5 Watts

Hence, for the circuit to function as described, a transistor must be found that exhibits avalanche breakdown and has a collector dissipation of at least 22.5 watts.

Several high power audio transistors, e.g., 2N174, 2N441, were examined for avalanche characteristics without success. Since the testing for avalanche is potentially destructive to the transistor, these tests were discontinued after several attempts to find an avalanche transistor failed. Further work in this area was discontinued due to the high mortality rate of transistors.

2. Impedance Matching

(a) Introduction

The original specifications on impedance matching stated that the load presented to the transmitter would fall within the area bounded by R = 25 to 1300 ohm and X = $\not<$ j1000 ohms over the entire frequency range of 3 to 30 mc. However, in a recent conference with the customer this specification has been changed such that the load impedance is a function of frequency. This function is a spiral in the R-X plane.

The problem involved in the original specification consisted of synthesizing a network where the resistive part of the load varied by a factor of 52

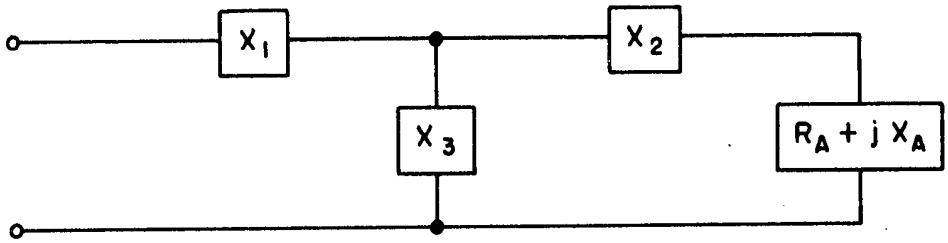
over a frequency variation of 10:1. This is an extremely large impedance transformation ratio. The Second Bimonthly Report described "L" and "Pi" networks which are theoretically possible but physically unrealizable because of the extremely large variations in capacity that are required.

When a matching network is placed between the source and the load a certain amount of insertion loss must be expected. However, the gain and power output of an amplifier are functions of the transistor and its associated load. Since the particular transistor has not been specified for the output stage of the RT21 transmitter and there is no information concerning a suitable unit, a "typical" transistor has been assumed. Under these circumstances, a variation in load resistance of 52:1 which is approximately 25:1 about the center point would lead to a 7 db. loss[4] in gain for a common emitter configuration. Since the problem is to deliver 10 watts of power into the load a loss of power by a factor of 5 because of mismatching is considered to be intolerable and a matching network must be used. However, if the insertion loss of the matching network exceeds 7 db., there would be no purpose in having the network present.

During the last period considerable work was done on the original specifications; i.e., 25 to 1300 ohms. A T_{ee} ladder lattice and variable transformer network were studied to see if they offered a solution to this problem.

(b) Tee Network

In terms of the network shown in Figure 2, (where x_1, x_2 and x_3 represent the reactance in the elements of the T-network, while $R_A \neq j\, x_A$ represents the antenna impedance), the input impedance, Z_{in}, will be a pure resistance of magnitude R_0 provided



IMPEDANCE MATCHING T NETWORK

FIGURE 2

$$-x_2 = x_A \neq x_3 \mp \sqrt{\frac{R_A}{R_O}\ (x_3^2 - R_A R_O)}$$

and

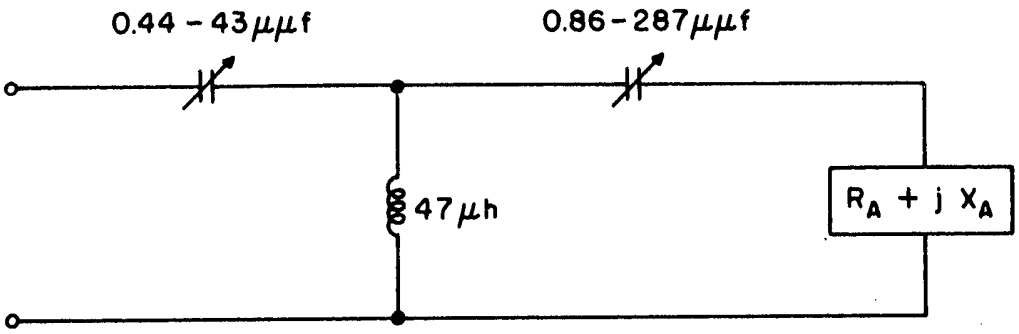
$$-x_1 = x_3 \mp \sqrt{\frac{R_O}{R_A}\ (x_3^2 - R_A R_O)}$$

Since x_1 and x_2 must be real numbers, it is apparent that $x_3^2 \geq R_A R_O$. Requiring this inequality to hold for all antenna impedances over the specified frequency band, again, as in the Pi-network, leads to unrealistic elements. The T-network for the 3-15 mc. band is shown in Figure 3. Not only is the ratio of maximum to minimum capacitance very large (335:1), but also the low value of the minimum capacity creates additional problems. Thus, a simple T-network does not appear to be a suitable solution to the problem.

A modification of the T-network appears, at first glance, to present a more attractive solution to the problem. If a parallel L-C combination is substituted for the capacitors in the arms of the T-network, the circuit shown in Figure 4 results. A network of this type contains elements whose size and range appear reasonable. However, as in the case of the modified Pi-network, the coil losses are excessive. If the equivalent shunt resistance of the coil is included, the parallel L-C may be represented at a specified frequency as a series R-C. Even with coils having a Q of 250, the R component of the R-C representation is so large that most of the power is absorbed in the matching network. This fact eliminates the modified T-network as a practical solution to the problem.

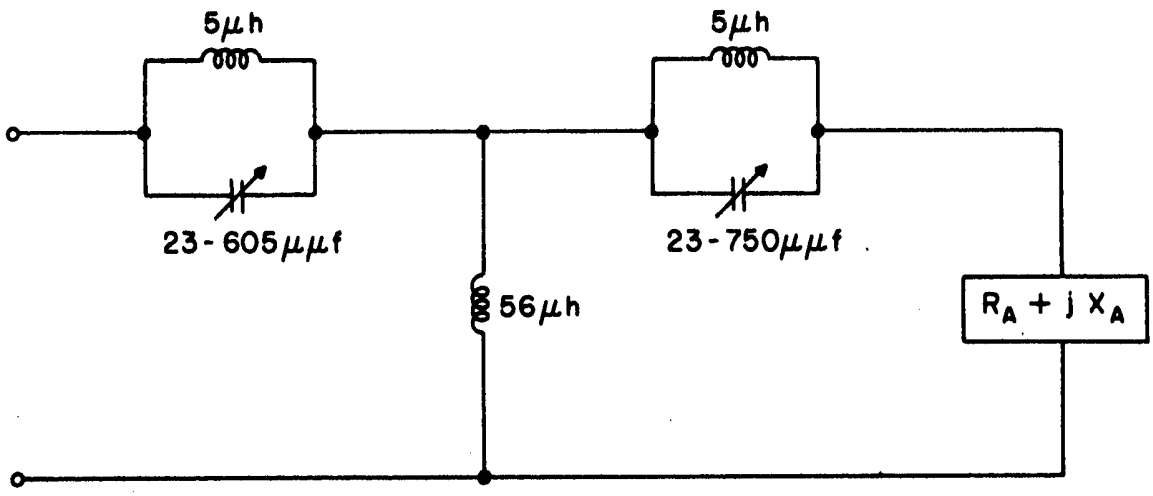
(c) Ladder Network

Impedance matching properties of a three-rung ladder (shown in



T - NETWORK FOR ANTENNA MATCHING
IN THE 3-15 MC BAND

FIGURE 3



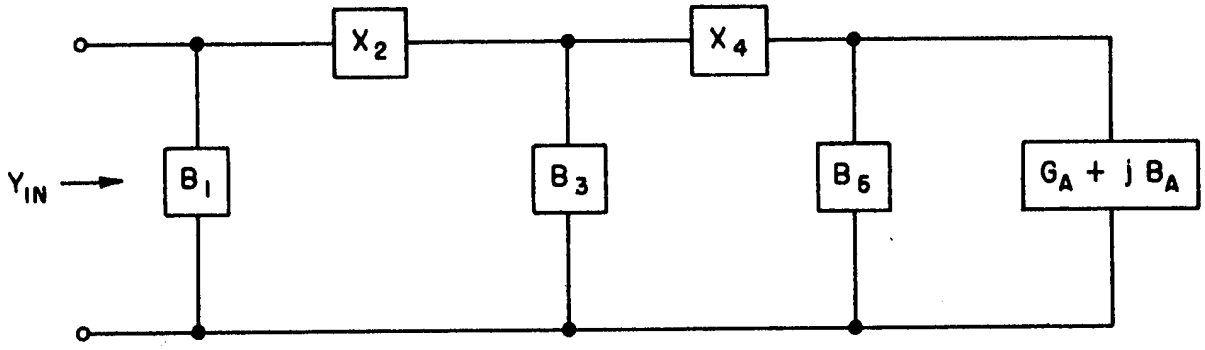
A MODIFIED T-NETWORK FOR ANTENNA MATCHING IN THE 3-15 MC BAND

FIGURE 4

Figure 5) were also investigated. Analysis of a network having this degree of complexity becomes extremely complicated. Since the control system under consideration provides for only two variable factors (impedance magnitude and phase), it was decided to simplify the analysis by considering x_2 and x_4 as fixed inductors and B_3 and B_5 as identical capacitors driven from a common shaft. With these constraints, B_3 and B_5 would then control impedance magnitude while B_1 controls impedance phase. The input admittance will be adjusted to a pure conductance of magnitude G_0 provided B_1 and B_3 are simultaneous solutions of two fourth-order algebraic equations. Since these equations do not lend themselves to a general solution, the problem was simulated on a digital computer. An exhaustive study of the network did not seem desirable at this time, but it appears that the necessary tuning ranges are approximately as shown in Figure 6. This network still requires a variable capacitor having a rather large value of maximum capacitance. A further investigation of this network has been postponed until other less complicated schemes have been definitely eliminated.

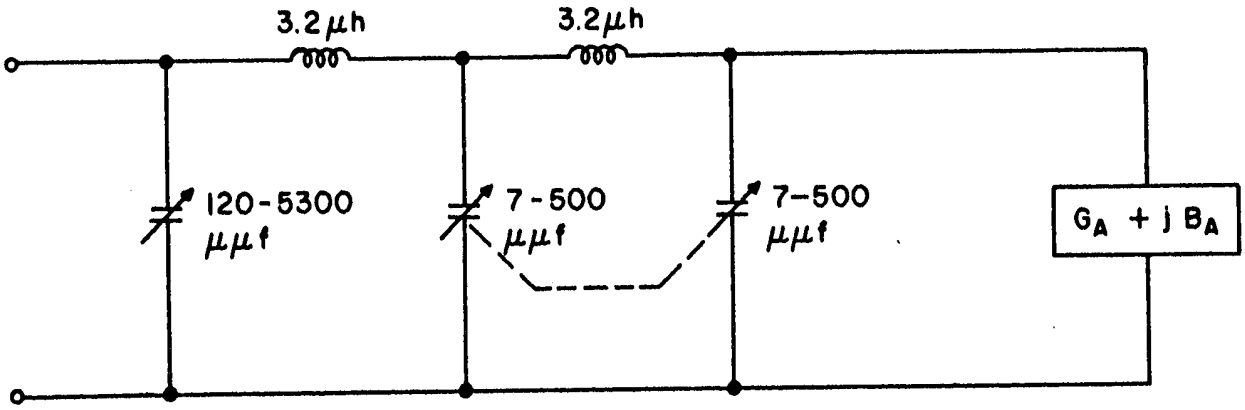
(d) Lattice Network

The problem of analyzing the lattice was placed on an analogue computer. In order to instrument the computer, values for the arms of the lattice had to be chosen. The choice of components was restrained to variable capacitors with a 100:1 ratio of maximum to minimum capacitance and inductors that would have small losses over the frequency spectrum being considered. Such a network is shown in Figure 7. Although a 100:1 ratio of capacitance is optimistic, it was felt that if the network was successful, an effort to reduce this ratio would be made in the future.



IMPEDANCE MATCHING THREE RUNG LADDER NETWORK

FIGURE 5



LADDER NETWORK FOR IMPEDANCE MATCHING IN THE 3-15 MC BAND

FIGURE 6

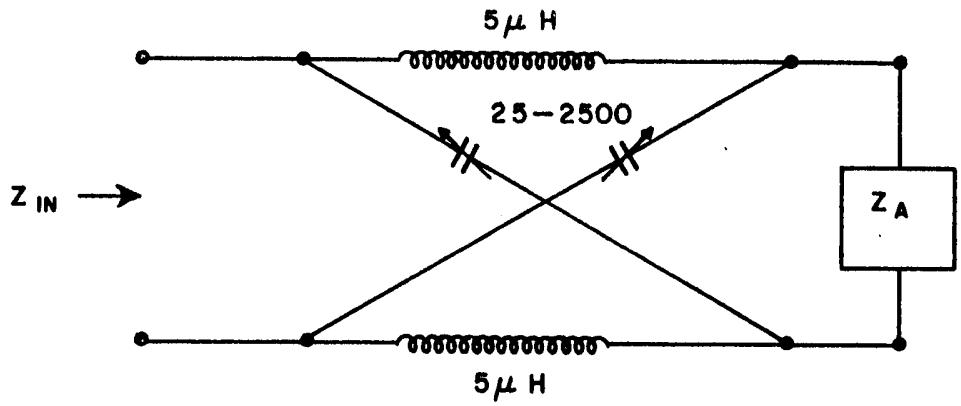


FIGURE 7

However, results from the computer indicate that the input impedance to the network cannot be made a pure resistance within the constraints that were placed on the components. Further work on this type of network has been postponed indefinitely.

(e) Variable Transformer Network

Another approach to this problem is a variable transformer shown in Figure 8. This circuit is a single tuned transformer with a variable tap on the primary side. This circuit has been analyzed from the viewpoint of an untuned transformer to which a tunable capacitor C is added, in order to make the input impedance to the transformer a pure resistance, and a variable tap is added to "tap down" this pure resistance to 500 ohms. Consider the circuit shown in Figure 9 where r_p and r_s are the resistance of the primary and secondary respectively. It may be shown that

$$Z = Z_p + \frac{Z_M^2}{Z_S + Z_L}$$

where $Z_p = r_p + j\omega L_p$ is the primary impedance

$Z_S = r_s + j\omega L_S$ is the secondary impedance

$Z_M = j\omega M$ is the mutual impedance

$Z_L = R_L + jX_L$ is the load impedance

Furthermore, by choosing the values of the circuit elements appropriately, it may be shown that Z is always inductive for all values of Z_L specified, i.e.,

$$Z = R + jX \text{ (inductive)}$$

If a capacitor, C, whose magnitude is

$$C = \frac{X}{R^2 + X^2} = \frac{X}{|Z|^2}$$

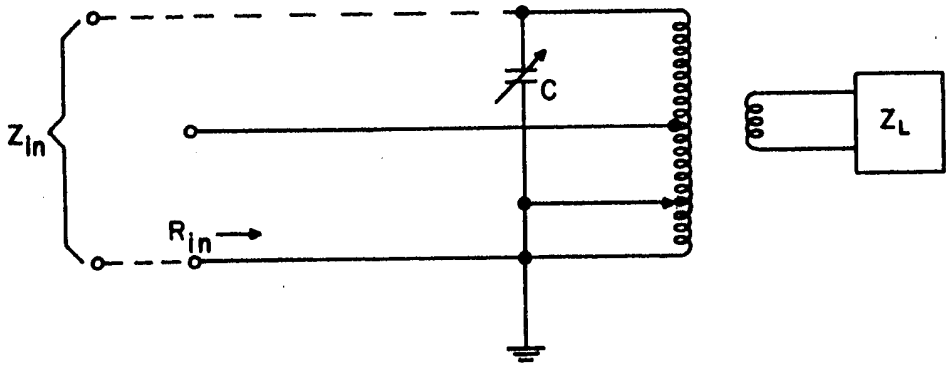


FIGURE 8

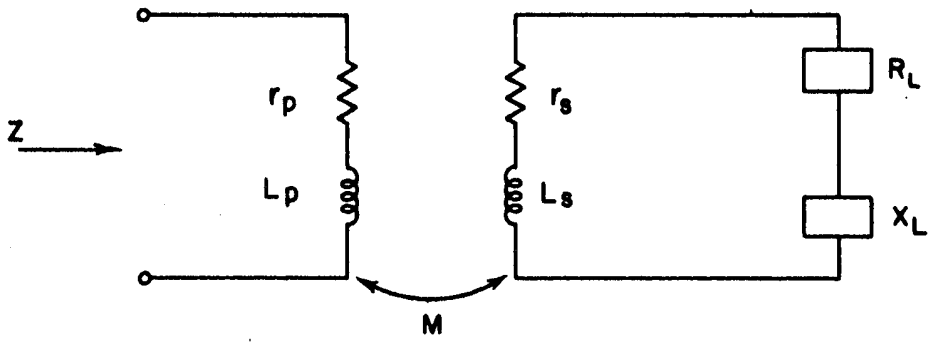


FIGURE 9

is placed in shunt with Z, Z will be a pure resistance whose magnitude can be calculated from:

$$R = r_p + \frac{\omega^2 M^2 (r_s + R_L)}{(r_s + R_L)^2 + (X_L + \omega L_S)^2}$$

This value of R appears across the entire coil and we can tap down to a 500 ohm level by using the variable tap on the coil. It is seen that R is a complex function of frequency and a large range of tap values must be allowed.

Preliminary laboratory experiments with this scheme indicate that the entire range of load impedances, over a frequency variation of 3 to 15 mc., can be transformed into an impedance of 500 + j0. This involved an insertion loss of about 0.2 db. at 10 mc. However, this was done with a modified variable inductor (Johnson 229-203) whose dimensions are 6½" x 3" x 3". Work is currently in the model shop to reduce the size of the coil to 5" x 1½" x 1-3/4". Future work on this scheme is pending completion of this device.

(f) Spiral Load

The advent of a new specification for the load impedance may make the work on the original specification, described above, obsolete. However, since these new specifications were received only recently it would be premature to say that they simplify the problem. In fact, they may make the problem more difficult since the dynamic range of resistance is increased from 52:1 to 120:1. On the other hand, the load is a function of frequency which may reduce some of the difficulties first encountered.

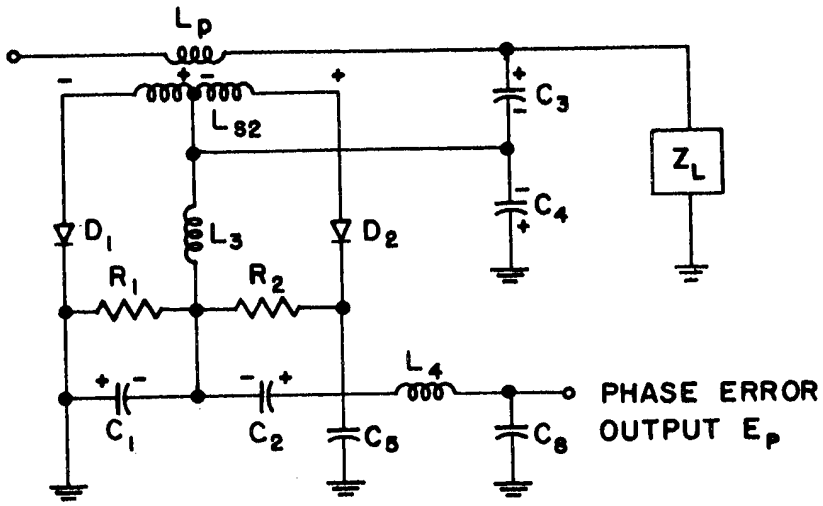
It is expected that more concrete information will be available during the next period.

3. Impedance Detector

The function of the impedance detector is to produce control signals which indicate the type of impedance produced by the antenna matching network. These control signals will then be applied to a servo system which varies the magnitude of the elements in the matching network until a resistive input impedance of the desired magnitude has been achieved.

Two D.C. output signals are derived from the impedance detector. The polarity of the first indicates whether the load impedance is inductive or capacitive, with zero output occurring when the load is purely resistive. The polarity of the second indicates whether the impedance is larger or smaller than a specified magnitude, with zero output occurring when the impedance magnitude is equal to the specified magnitude.

The theory on which the operation of the two components of the impedance detector is based is presented as follows. The phase detector, which indicates whether the load is inductive, capacitive or resistive, is shown in Figure 10. The output of the phase detector is the sum of the voltages developed across C_1 and C_2. This sum indicates the phase of the impedance because of the following facts. A fraction of the line voltage (determined by the divider C_3 and C_4) is applied to the center tap of the secondary. Since the voltage induced in the secondary winding of the transformer is 90^o out of phase with the line current, the voltage at one end of the secondary represents the vector sum of a fraction of the line voltage plus a voltage which leads the line current by 90^o. The voltage at the other end of the secondary is the vector sum of a fraction of the line voltage plus a voltage which lags the line current by 90^o. To make the mathematics more explicit, the line current is represented in phasor



IMPEDANCE PHASE DETECTOR

FIGURE 10

notation as

$$I_L = k_0 V_L (1 + ja),$$

where k_0 is a normalizing factor which depends on the magnitude of the load impedance. The quantity "a" will be positive for capacitive loading, negative for inductive loading and zero for purely resistive loading. The voltage induced across L_{S2} is then

$$V_{LS2} = j\omega M k_0 V_L (1 + ja),$$

and from the indicated polarity, also

$$V_{LS1} = j\omega M k_0 V_L (1 + ja),$$

where M is the mutual inductance of half the secondary. The action of D_1 is then to allow C_1 (and also C_4) to charge to a voltage

$$V_{C1} = \left| \frac{C_3}{C_3 + C_4} V_L - j\omega M k_0 V_L (1 + ja) \right|$$

The action of D_2 allows C_2 to charge to a voltage

$$V_{C2} = \left| \frac{C_3}{C_3 + C_4} V_L + j\omega M k_0 V_L (1 + ja) \right|.$$

The error output voltage, E_p, is then

$$E_p = V_{C2} - V_{C1},$$

which, after algebraic manipulation, becomes

$$E_p = V_L \left\{ \sqrt{\left[\frac{C_3}{C_3 + C_4}\right]^2 + k_0^2 \omega^2 M^2 (1 + a^2) + 2ak_0 \omega M \frac{C_3}{C_3 + C_4}} - \sqrt{\left[\frac{C_3}{C_3 + C_4}\right]^2 + k_0^2 \omega^2 M^2 (1 + a^2) - 2ak_0 \omega M \frac{C_3}{C_3 + C_4}} \right. \quad (1)$$

Eq. (1) indicates the polarity and magnitude of E_p is determined by "a", the

factor which is a measure of the amount by which the line current either leads or lags the line voltage.

With regard to the function of the other elements in the phase detector, L_3 provides a D.C. path for the capacitor charging currents while isolating the R.F. line voltage from the rest of the circuit. C_5, L_4 and C_6 provide additional RF filtering.

The magnitude detector, which indicates whether the load impedance is less than, greater than, or equal to a specified value is shown in Figure 11. The operation of the magnitude detector is based upon a comparison of the D.C. voltage across C_1 to the D.C. voltage across C_3. Assuming all impedances shunting the load are much greater than the load impedance, the action of D_1 is to allow C_1 to charge to

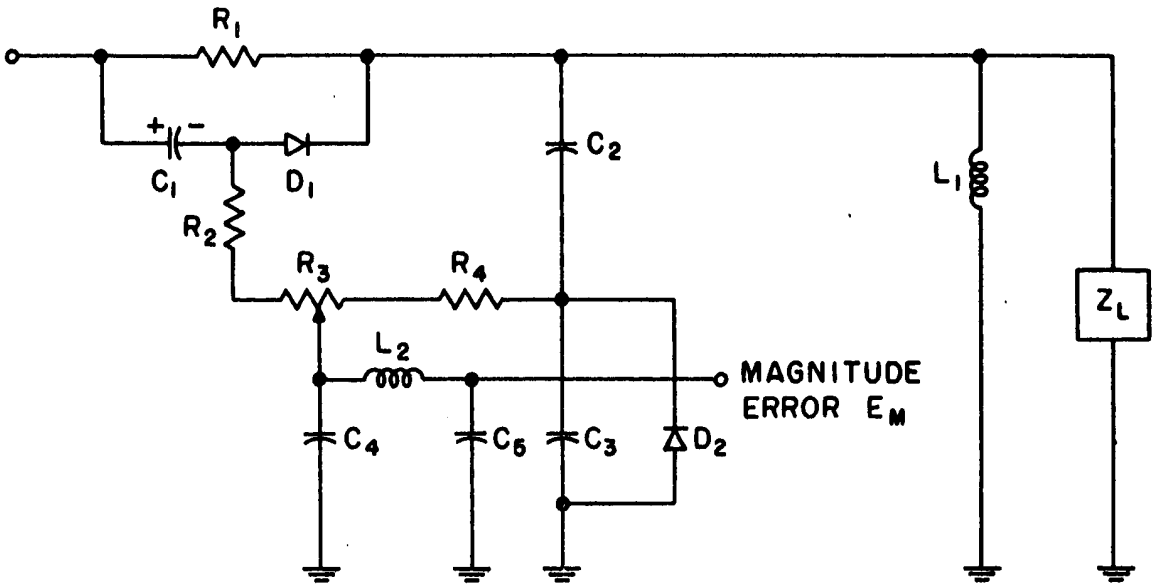
$$V_{C1} = \frac{R_1}{|R_1 + Z_L|} V_L \qquad (2)$$

Due to the clamping action of D_2, C_3 charges to a voltage

$$V_{C3} = \frac{C_2}{C_2 + C_3} V_L \qquad (3)$$

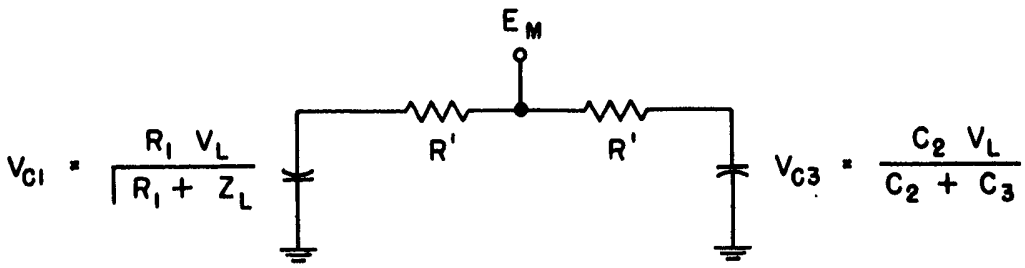
Since L_1 provides a D.C. ground, the significant part of the magnitude detector may then be represented as shown in Figure 12. In this circuit, R_1 and the DC resistance of the coil have been considered negligible in comparison to the other resistance in the circuit. The charged capacitors have been represented by D.C. batteries; and R_2, R_3 and R_4 have been lumped into a series connection of two resistors, each designated by R'. The magnitude error voltage, E_M, may be written as

$$E_M \cong V_{C3} - \left[\frac{V_{C3} + V_{C1}}{2R'}\right] R'$$



IMPEDANCE MAGNITUDE DETECTOR

FIGURE II



EQUIVALENT REPRESENTATION OF THE IMPEDANCE MAGNITUDE DETECTOR

FIGURE 12

$$\cong V_{C3} - \frac{V_{C3} + V_{C1}}{2} \qquad (4)$$

Since $R_1 \ll |Z_L|$, substituting Eq. (2) and Eq. (3) into Eq. (4) results in

$$E_M \cong \frac{V_L}{2}\left[\frac{C_2}{C_2 + C_3} - \frac{R_1}{Z_L}\right]$$

In order to obtain zero output when $|Z_L| = R_0$ (the desired impedance magnitude), the parameters must be chosen so that

$$\frac{R_1}{R_0} = \frac{C_2}{C_2 + C_3}$$

then

$$E_M \cong \frac{R_1 V_L}{2}\left[\frac{1}{R_0} - \frac{1}{|Z_L|}\right] \qquad (5)$$

Eq. (5) shows that the magnitude and polarity of E_M is determined by the manner in which Z_L differs from R_0.

With regard to the function of the other components of the magnitude detector, L_2, C_4 and C_5 provide RF filtering. The pot (R3) allows for compensation of slight circuit unbalance.

Work is in progress to evaluate and refine the operation of the impedance detector. The degree of accuracy with which the phase detector indicates a resistive termination has been investigated at several frequencies within the 3-30 mc. band. Since stray capacitance exists in the detector circuits, zero output from the phase detector actually occurs with an input impedance which is slightly capacitive. However, this effect is small enough that it does not pose a serious problem. In view of the work to date on the impedance detector, its operation appears to be in accordance with theory. It is anticipated that more explicit

results will be available for inclusion in the next report.

4. Automatic Tuning Program

(a) Voltage Variable Capacitors

Investigations showed that in the automatic tuning system, the full, useful range of capacitance variation of the tuning diodes was not being realized. The reduced maximum to minimum ratio came about because the voltage could not be brought as close to zero as was desired. When the modulator was balanced, it was found that a second harmonic of the subcarrier appeared at the output. The second harmonic could not be nulled and the use of traps proved ineffective. It was consequently necessary to reduce the input to the modulator. While this removed the second harmonic, it introduced several other problems. As a result of the reduced input, the maximum output obtainable was also reduced. This situation could be improved by increasing the step-up ratio of the transformer feeding the rectifier (T_2 Figure 3, Bimonthly Report No. 1).

Difficulty was still experienced in trying to tune the capacitors over the full range. "Lock on" was unreliable at the low frequency (maximum capacity) end of the bands. The trouble was attributed to the long time constant of the rectifier circuitry supplying the dc control voltage. If the sweeping voltage overshot, even though the modulator output passed through zero, the long time constant prevented charge from leaking off the capacitor fast enough to allow the system to reach equilibrium at the desired point. Instead, the voltage would continue to sweep to the high end of the band.

In order to provide a shorter time constant, the output to the storage capacitor is being supplied at a lower impedance level. This has called for a redesign of the amplifier and a special miniature output transformer. A diagram

of this portion of the circuitry is shown in Figure 13. The transformer for this application had not, at the time of writing, been received.

During the past report period, the Texas Instrument 2N1141 transistor became available. This transistor is quoted as operable at 750 mc. and has a dissipation rating of 750 mw. It was felt that the use of this transistor in the crystal oscillator stage would result in a considerable reduction in the total number of stages in the transmitter. This is particularly desirable because of a consequent reduction in the automatic tuning circuitry.

Due to the radically different characteristics of the 2N1141, it was not possible to make a direct substitution for the 2N247. The original circuit is shown in Figure 14. This circuit has the ability to produce an output at the second harmonic of the crystal. This output is produced by amplifying the second harmonic distortion of the fundamental crystal frequency and is not the result of a mechanical mode of the crystal. The output level is relatively low, necessitating an additional stage of amplification. Several attempts were made to duplicate this type of operation using the 2N1141 transistor. In order to avoid loading the crystal too heavily with the lower impedances associated with the new transistors, a Darlington configuration was investigated using the circuit shown in Figure 15. The results were not satisfactory. The modification shown in Figure 16 was also tried but operation at the second harmonic could not be obtained. Furthermore, replacing the crystal with a small capacitor, oscillation was obtained.

The Pierce oscillator, as shown in Figure 17, was investigated with very encouraging results. The following performance characteristics were observed.

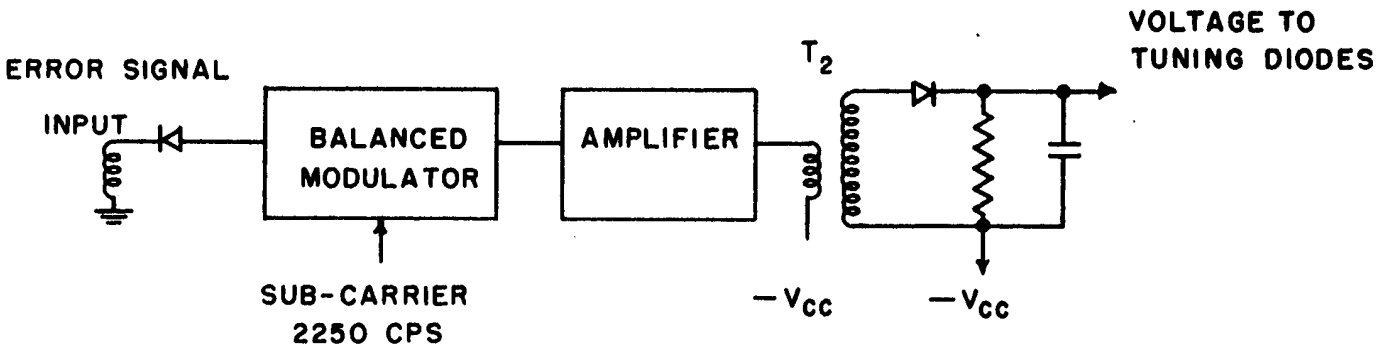
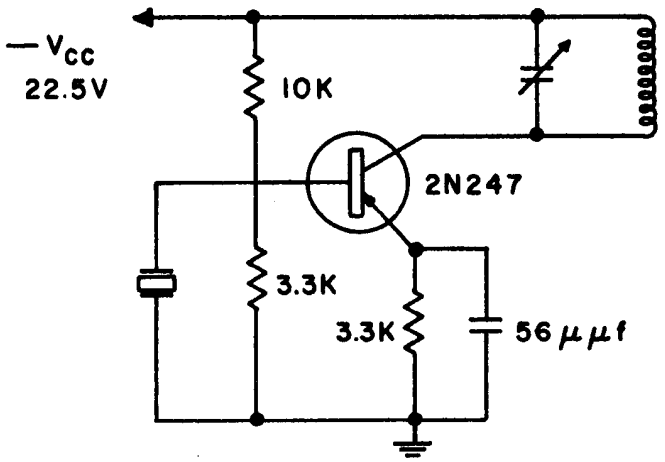


FIGURE 13



ORIGINAL OSCILLATOR CIRCUIT

FIGURE 14

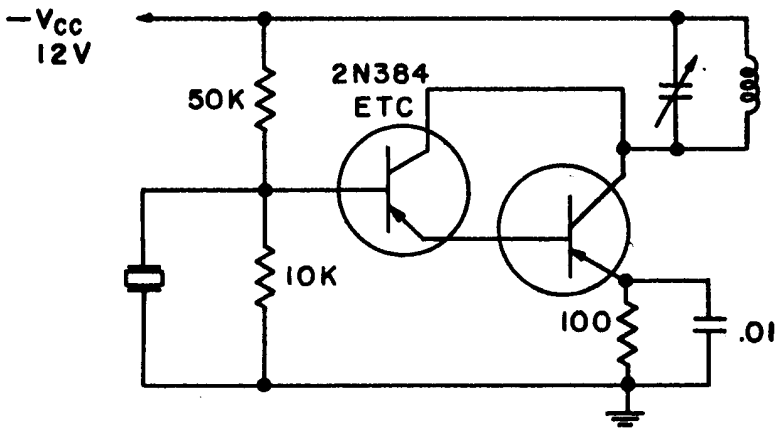


FIGURE 15

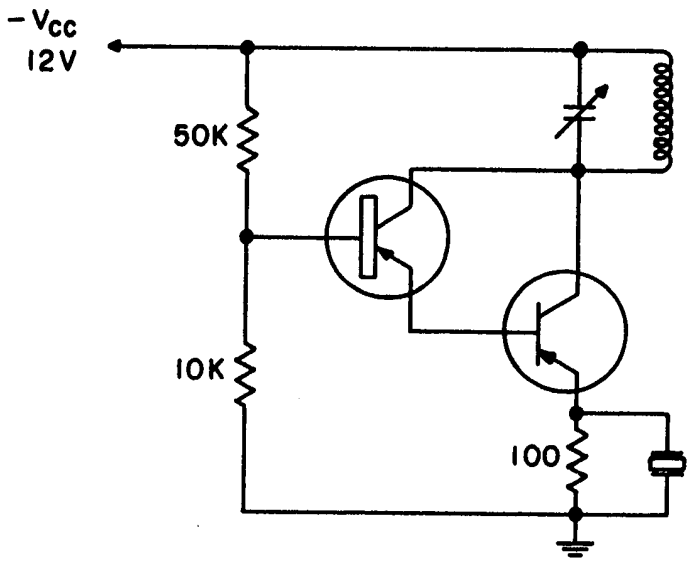
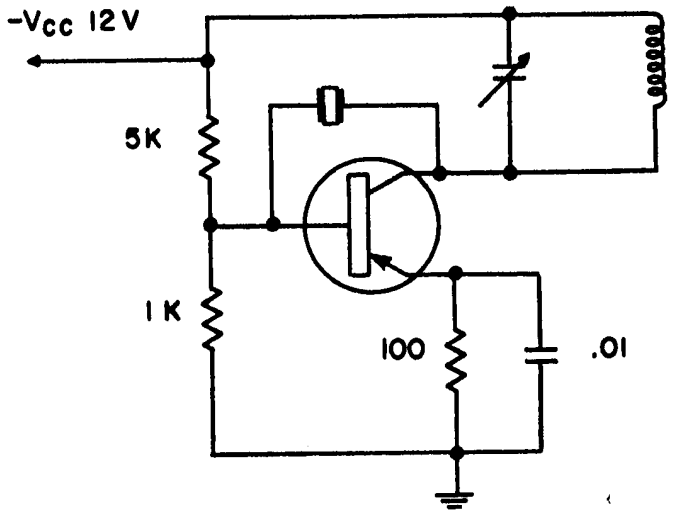


FIGURE 16



PIERCE OSCILLATOR

FIGURE 17

(a) No oscillation could be obtained without the crystal in place.

(b) An increase in output power by a factor of eight was obtained compared with that available from a 2N247 oscillator plus a 2N247 amplifier in cascade.

(c) No output is available until the output tank is accurately tuned to the correct frequency.

(d) Requires no change in the emitter capacitance with frequency.

(e) No second harmonic output is available. However, an output is obtained on the third mode (shear mode) of the crystal.

(f) There is no reduction of output power when operating on the third mode. The same output can be obtained at 15 mc. whether a 5 mc. or a 15 mc. crystal is used.

(g) No output at the third mode is available unless the tank is tuned correctly.

(h) Tuning is sharp, thereby increasing the reliability of the lock on system.

(i) The output impedance is low, reducing the tuning range. This can be overcome by tapping the collector down on the tank circuit. A somewhat similar transistor, the XT-517 manufactured by Pacific Semiconductors, being a higher impedance device, may remove the necessity for tapping the coil. An order of these transistors has not yet been received.

If third mode operation is acceptable to the customer, use of this configuration will result in a considerable simplification of the transmitter.

(b) Electrical Control of Coil Taps

To tune the tank circuit to the crystal in use, two things are necessary:

(i) for a fixed inductance of the tank circuit, (L_1, L_2 or L_3), to allow the voltage $V_{control}$ over the voltage controlled capacitors to rise from about .2 Volts to about 25 Volts (thereby sweeping through the diodes' capacity range) and then reset to .2 Volts,

(ii) at the end of the first sweep to reduce the inductance from L_1 to L_2, at the end of the second sweep to reduce the inductance from L_2 to L_3, and finally after the third sweep to reset from L_3 to L_1 and then repeat the three-step cycle.

The three sweeps will cover about 3-5 Mcps, 5-9 Mcps, and 9-15 Mcps. The range 15-30 Mcps is covered by a separate coil L_4, which is connected when the manual switch is thrown to the "15-30 Mcps" position.

The method used to meet the two demands is as follows (see Figure 3, page 6B, "First Bimonthly Report"):

(i) The charging and discharging of the capacitor C_1, the voltage of which is $V_{control}$, is made to cycle between .2 Volts and 25 Volts. For $V_{control}$ = 25 Volts, a flip-flop circuit is actuated, making a transistor (in parallel with the lower 2N123, on the figure) saturate and thereby suppress the subcarrier voltage supplied to transformer T_2. When $V_{control}$ has dropped to .2 Volts, a new signal resets the flip-flop. The subcarrier is turned on and the capacitor C_1 will charge. Independently of the tank circuit inductance, the capacitor C_1 will charge and discharge until its voltage level has been determined by resonance.

(ii) $V_{control}$ will therefore vary with time as indicated in Figure 18. To operate the switches that change the tank inductance from L_1-L_2-L_3-L_1, etc., a system of flip-flops is used. The flip-flop shown in Figure 19 has a control-transistor T_{cn} in one leg. When T_{cn} is reversed-biased, the flip-flop has only one stable position. When T_{cn} is forward-biased, the flip-flop will remain in the stable position. If the point D is pulled sufficiently below ground, the flip-flop is actuated. As long as no impulse is applied to E and T_{cn} remains forward-biased, the transistor will remain in this new stable position. What has been said about the circuit in Figure 19 holds true for the circuit in Figure 20, where 3 p-n-p transistors have been used instead of the 3 n-p-n transistors shown in Figure 19. It will be noticed that the components and wiring are identical on the 2 flip-flops, but that the voltage connections have been reversed. The p-n-p and the n-p-n transistors used have similar characteristics.

The 3.9 K and 1.6 K resistors have been chosen so that the voltage of point H (Figure 20) is between the two possible voltages of D, (Figure 19), and consequently the voltage of point B (Figure 19) is between the two possible voltages of point G. If we connect the base of a controlling T_{cn} transistor to G, the state of the p-n-p flip-flop determines whether the n-p-n flip-flop is bistable or not. If we connect the base of a controlling T_{cp} to D, the state of the n-p-n flip-flop determines whether the p-n-p circuit is bistable or not.

Figure 21 shows these flip-flops connected, n-p-n's and p-n-p's alternately. All T_{cn} and T_{cp} are reverse-biased when voltage is applied, the initial condition of all flip-flops is thus defined. During the first charging

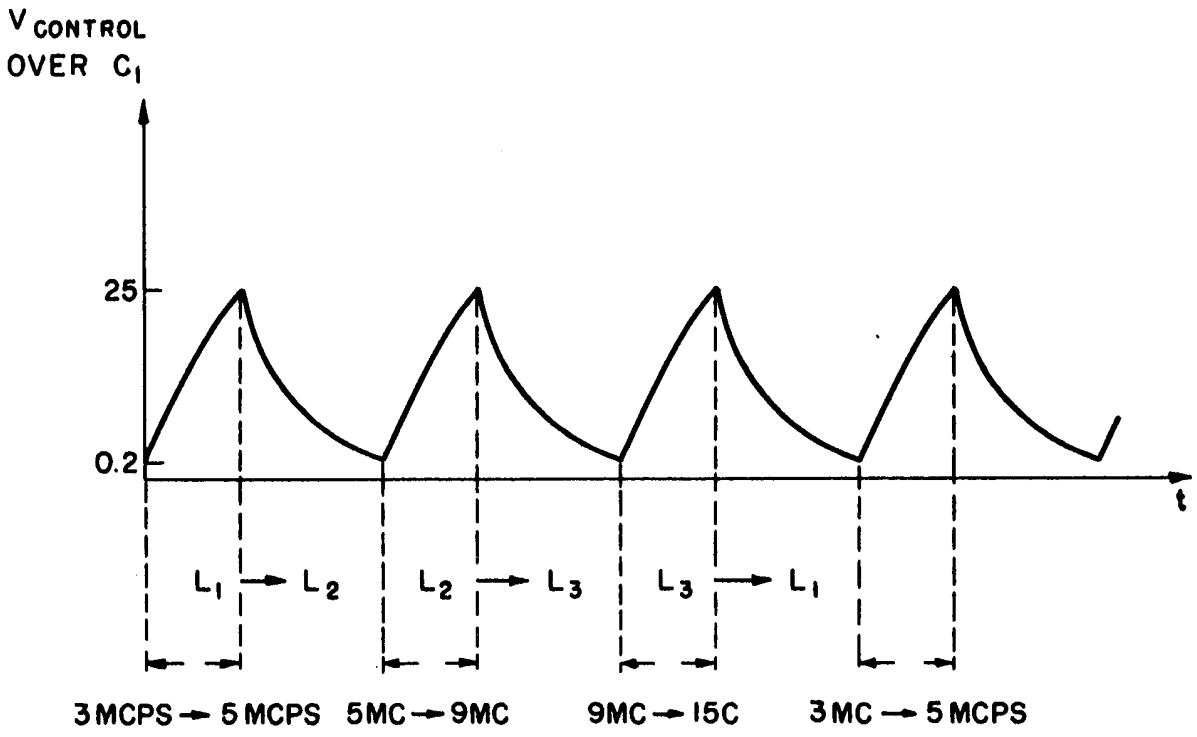


FIGURE 18

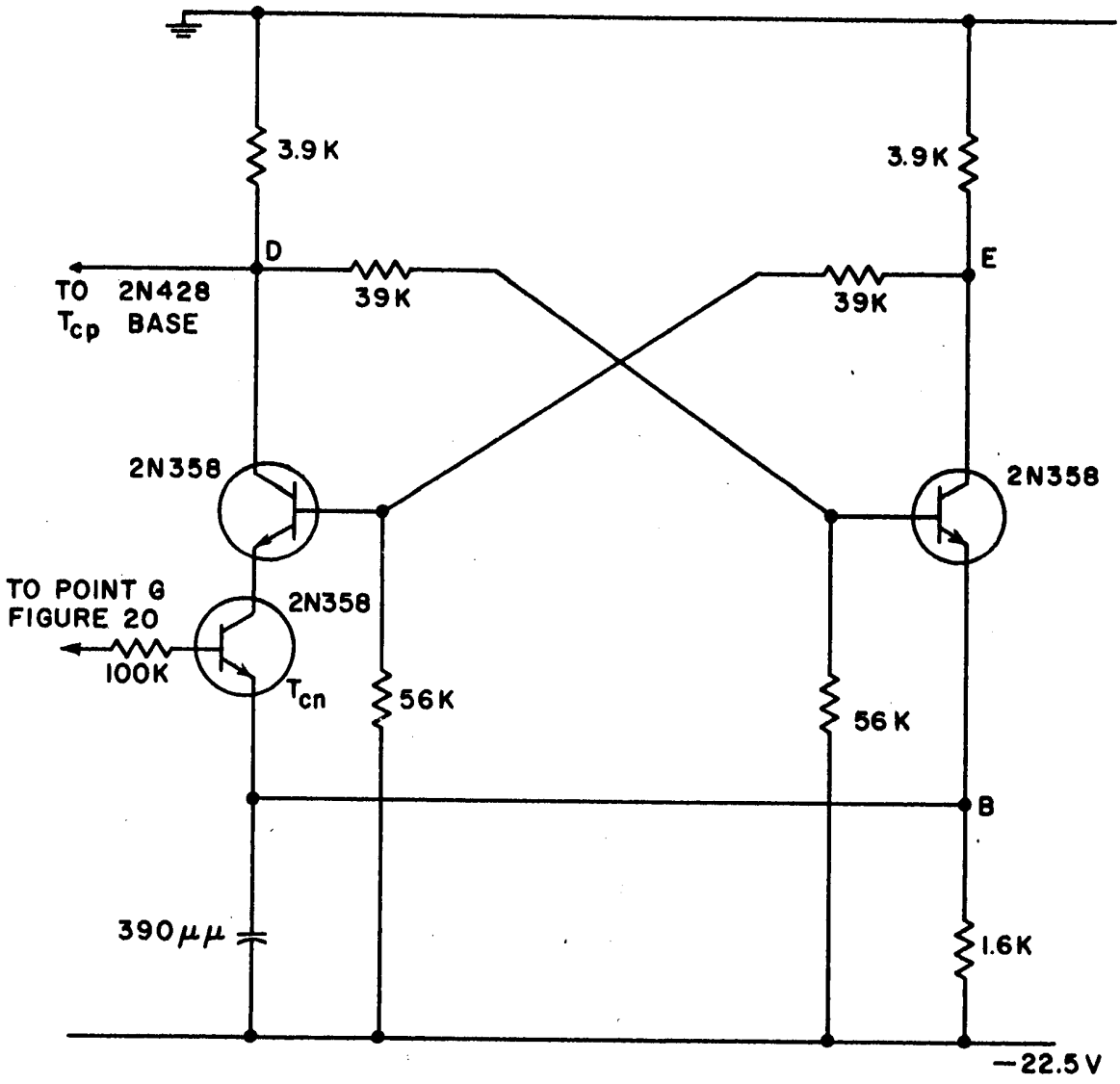


FIGURE 19

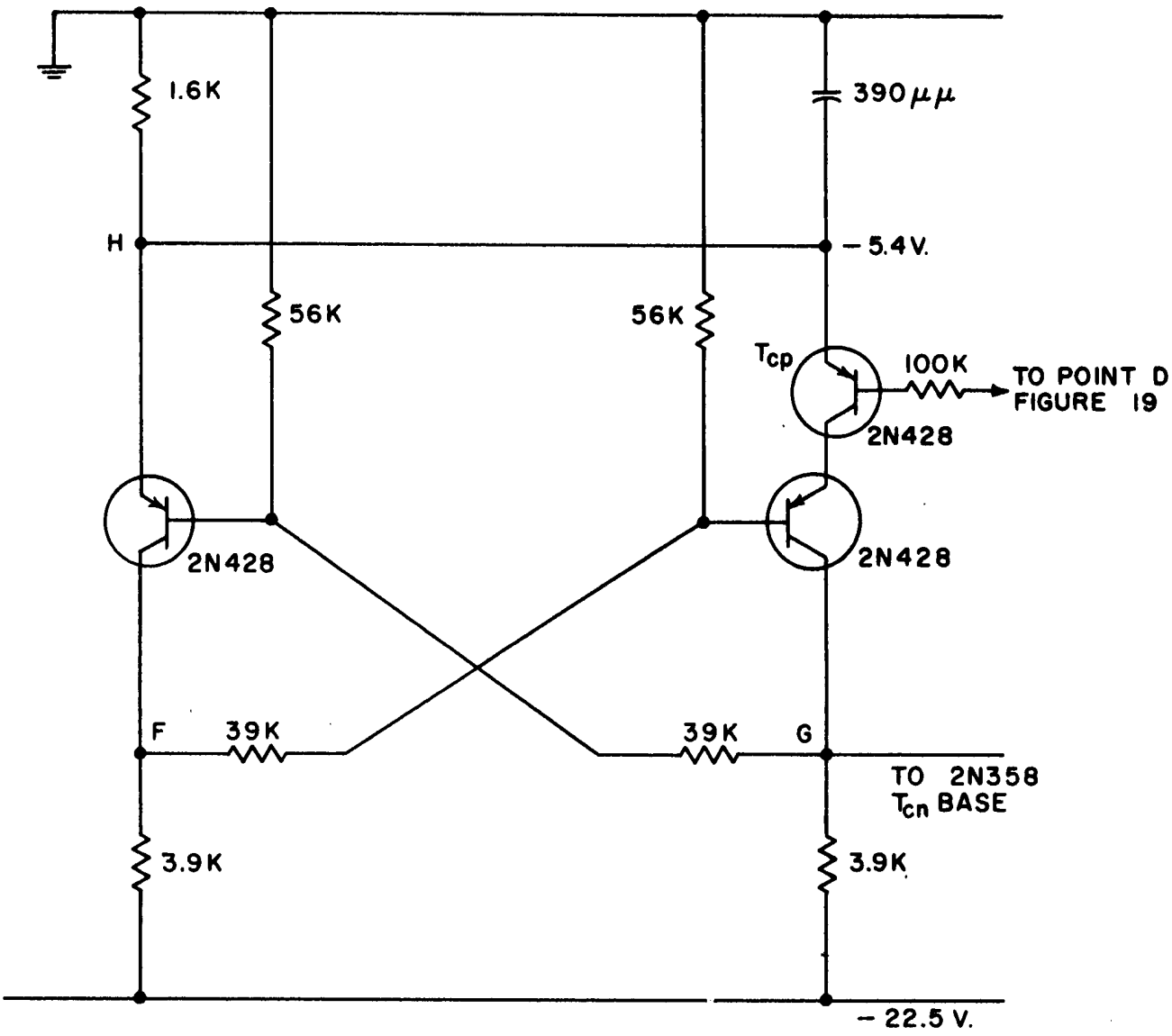


FIGURE 20

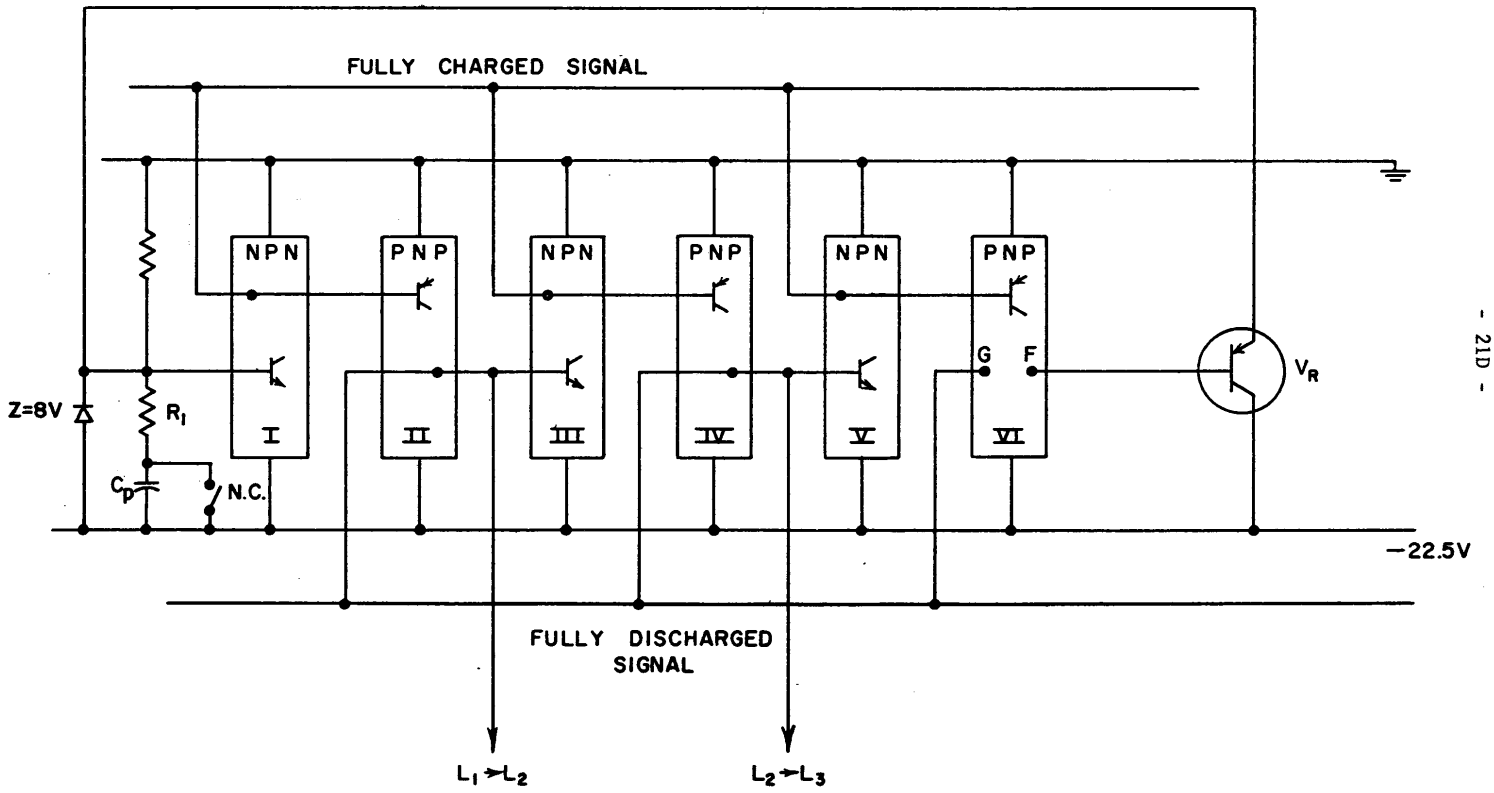


FIGURE 21

operation flip-flop No. I will get its T_{cn} forward-biased permanently by a pilot-capacitor C_p. The first "fully charged signal" will then actuate flip-flop No. I and thus forward-bias the T_{cp} in flip-flop No. II. A "fully-discharged" signal will then actuate flip-flop No. II, thereby

(i) forward-biasing the T_{cn} of flip-flop No. III, and

(ii) operating a transistor switch that changes the inductance of the tank circuit from L_1 to L_2.

In the same way a subsequent "fully-charged" signal, followed by a "fully-discharged" signal, will cause another transistor switch to change the tank circuit inductance from L_2 to L_3. After a third pair of "fully-charged" and "fully-discharged" signals, flip-flops No. V and No. VI in Figure 21 will operate. Via a transistor V_R the T_{cn} of flip-flop No. I will be reverse-biased, thereby resetting flip-flop No. I, and via the control transistors T_{cn} and T_{cp}, the whole chain is reset.

When flip-flop No. VI has reset, the transistor V_R is reverse-biased. As $R_1 x C_p$ is large compared to the resetting time of the chain, T_{cn} of flip-flop No. I will immediately be biased in the forward direction when V_R is reverse-biased. When all the six flip-flops reset, the switches that changed the tank circuit inductance will reset, thus resetting the inductance from L_3 to L_1. At resonance the sequence of "fully-charged" and "fully-discharged" signals will stop and the six flip-flops remain in the appropriate setting, thus keeping the tank circuit inductance fixed.

IV. Conclusions

The brief investigation of avalanche operation of low frequency transistors in order to obtain high power outputs at high frequencies was terminated

when it became clear that this method was not suited to the RT21 transmitter requirements.

In the investigation of matching networks, the most promising approach appears to be that using a variable transformer network. However, a change in specifications arising out of a recent visit by the customer has altered the validity of the previous conclusions. At the time of writing, the full significance of the changed specifications had not been determined.

The phase and magnitude sensing circuits have been built and satisfactory results obtained. Some care is necessary in order to obtain desirable operation over the whole 3-30 mc. range.

In the automatic tuning program, a switching circuit has been worked out which will enable coil taps to be changed automatically so that, with a maximum to minimum tuning ratio of only 2:1, the whole range from 3-30 mc. can be covered continuously. Various undesirable effects which had caused a reduction in the tuning ratio obtainable with voltage variable capacitors have been overcome. The automatic switching circuitry has been built in preliminary form but has not been operated in conjunction with the voltage tuned diodes.

The use of Texas Instrument 2N1141 transistors has resulted in a substantial increase in output power from the oscillator stage. As a result of the increased power level, the number of stages can be greatly reduced, thereby eliminating a very considerable quantity of control circuitry. The oscillator is being operated at the crystal fundamental for frequencies from 3-15 mc. and at the 3rd harmonic for frequencies from 15-30 mc.

V. Future Plans

As a result of the changed antenna matching requirements, it will be necessary to spend some time reconsidering the most advantageous method by which to achieve the desired matching range. Fortunately this will not interrupt the work being carried out on the sensing circuitry. Further work will be necessary in order to obtain uniformly satisfactory results over the whole 3-30 mc. range. Some attention is required to insure that the slope of the output as a function of error is steep around the origin in order to insure adequate sensitivity.

Efforts will be made to combine the individual circuits which have been constructed to perform the automatic tuning function. When this has been accomplished, a critical examination will be made to determine to what extent the circuitry may be simplified and optimized.

As stated in the body of this report, a number of transistors of a new type are on order. These will be evaluated for this application as soon as they are received. They will not, however, provide a solution to the output stage problem. Transistors suitable for this stage are not yet available. If this situation still prevails by the time the remainder of the program has been completed, it will be necessary to combine the outputs of several transistors in order to provide, at least, a token output in order to demonstrate the operation of the antenna matching circuitry.

VI. Identification of Key Technical Personnel

The following name should be added to the personnel reported in previous bimonthly reports.

25X1

VII. Bibliography

1. Miller, S. L., "Avalanche Breakdown in Germanium," Physical Review, Vol. 99, #4, p. 1234, August 1955.

2. Shockley, "Theory of P-N Junctions in Semiconductors and P-N Junction Transistors," Bell System Technical Journal, Vol. 28, #3, p. 435, July 1949.

3. Beale, Stephenson, Wolfdale, "A Study of High Speed Avalanche Transistors," Proc. I.R.E., Vol. 109, Part B, p. 394, July 1957.

4. R. F. Shea, Editor, "Transistor Circuit Engineering," p. 78, Wiley, New York, 1957.