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MODEL HI-4896-1/1A

MINIATURE TIME-CODE GENERATOR

and

MODEL HI-4896-2

PRESET READER

FLOW CORPORATION
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SECTION 1

INTRODUCTION

1.0 INTRODUCTION

The time-code generator system consists of two units: the Airborne Time-Code Generator (TCG) and the Ground Preset Unit (GPU). The TCG is a completely self-contained unit which generates a serial time code for periods up to a day using a self-contained battery. The GPU is used to charge the battery in the TCG, preset the time of day, and check the output code for correct format.

1.1 Overall Description

The airborne TCG is housed in a miniature package consisting of a rechargeable battery of six silver-zinc cells, a 1 megaHertz oscillator, and four printed-circuit boards containing integrated circuits and discrete components used in the power supply and modulator. The complete system operates from a regulated +5 volts obtained from the battery.

The ground unit (GPU) is used to preset the time in hours, minutes, and seconds into the TCG. The output of the TCG is read by the preset unit to insure all circuits are operating properly. The internal battery of the TCG is charged and the voltage checked by a panel meter on the GPU. Automatic cutoff is provided for unattended charger operation.

1.2 Equipment Specification

1.2.1 Airborne Time-Code Generator

1.2.1.1 Time-Base Oscillator

Stability: 1×10^{-7} per 24 hours after temperature stabilization.

Frequency Change: Less than $\pm 5 \times 10^{-6}$ over temperature range 0 to 60 degrees C.

1.2.1.2 Signal Outputs

a. All Outputs are short-circuit-proof to ground.

b. Time Code Format

XR3 time code modulated on a 1000 Hz carrier frequency (20-bit code, 25 pps bit rate). Modulation ratio adjustable from 2:1 to 6:1. Output level is a nominal 3 volts peak-to-peak into a 1000 ohms to ground. (J2)

c. 100 kHz Sine Wave

Signal level 1 volt peak-to-peak into 10,000 ohms load to ground. (J3)

1.2.1.3 Operating Controls

a. Switch, Power OFF-ON. Turns off internal battery when equipment is not in use.

b. Switch, OPERATE-RESET. Used to reset generator to zero if ground preset unit is not available.

1.2.1.4 Output Connectors

a. External preset connector J1 (Deutsch DSM04-7-15S) connects the generator to the GPU for charging battery and presetting time.

b. Code Output J2 (Miniature coax - UG1468/U) connects the serial time code to desired load. (Need not be connected during preset; however, if connected to modulated code input of Preset Reader, will provide a backup check of code accuracy after removal of umbilical.)

c. 100 kHz output J3 (miniature coax UG1468/U) connects the 100 kHz sine wave to desired load.

1.2.1.5 Equipment Mechanical Specification

a. Size (See Figure 1.1 for mounting dimensions)

Approximately 6-1/4 x 3 x 2-7/8, including mounting base. The unit is designed for direct mounting and no vibration isolators are provided.

b. Weight

Approximately 35 ounces.

1.2.1.6 Environmental

a. Vibration

5 g's to curve B of MIL-STD-810A.

b. Shock

15 g's 11-millisecond duration in all three axes.

c. Temperature and Humidity

0 to 60 degrees C at relative humidity of up to 95 percent, without condensation.

d. Altitude

To 100,000 feet.

1.2.2 Ground Preset Unit Specification

1.2.2.1 Operating Controls and Indicators

a. Power Switch S1 OFF-ON. Controls primary ac input power.

b. Charger Switch S2 ON-OFF-TRICKLE. Controls operation of battery charger. Normal position during battery-charge cycle is ON.

c. Mode Switch S3 CLEAR-SET-STOP-RUN. Allows preset of time in airborne generator. CLEAR resets all registers to zero. SET allows preset of hours, minutes, and seconds into TCG, using pushbutton advance switch. STOP resets minor counter in TCG to zero, register remains at preset value (no output code). RUN mode is normal mode of operation. The first register advance occurs one second after unit is switched to RUN mode.

d. Time Set pushbuttons ADVANCE HOURS (S4), ADVANCE MINUTES (S5), and ADVANCE SECONDS (S6). Depressing these switches cause the time to advance in the respective registers.

e. Display Bulbs V1 to V6. The Nixie display exhibits the register in hours, minutes, and seconds. The advance of the register time is "on time" with the code.

f. Meter M1 shows the state of charge of the battery in the airborne TCG. A fully-charged battery is at 9.6 volts.

1.2.2.2 Output and Input Connectors

a. J1 - Input Power MS3102A-10SL-3P.

Pin	Function
A	115 volt, 50 to 400 Hz
B	115 volt return
C	Chassis Ground

b. J2 - Deutsch DSM04-7-15P. Connects the GPU to the TCG. (See Dwg C-4896-70002)

c. Modulated Code J3 (BNC). Monitors the input code from the TCG.

d. One-Pulse-Per-Second J4 (BNC). Provides method for determining exact synchronization of generator. The leading edge of the +4-volt pulse is "on time". The pulse is 40 ms wide.

e. DC Code J5 (BNC). Monitors detected code.

1.2.2.3 Package

Overall dimensions are 5-1/4 inches high by 6-1/2 inches wide front panel. (May be rack-mounted by providing extensions.) Unit extends 12 inches behind front panel. Add 2 inches for mating connector and cable.

1.2.2.4 Power Input

The unit operates on 105 to 125 volts, 50 to 400 Hz, single-phase. Power is less than 40 watts, depending upon battery-charger requirements.

1.2.2.5 Battery-Charger Rate

The charge rate is a constant current providing a 85 percent charge in approximately 12 hours or less. The current shuts off as the voltage approaches 9.6 volts across the battery. The unit may be operated while the charger is working.

1.2.2.6 Fuses

The equipment is protected by the following fuses:

Fuse	Type	Function
F1	1/2 Amp MDL	AC primary
F2	1/4 Amp AGC	+15-volt supply
F3	1/16 Amp AGC	∓200-volt display

SECTION 2

INSTALLATION

2.0 INSTALLATION

2.1 Ground Preset Unit

a. The GPU may be rack-mounted in 5-1/4-inch panel height by the addition of extension plantes on the front panel. Optionally, the unit may be placed on the bench.

b. Connect the GPU to a source of ac power from 105 to 125 volts ac, 50 to 400 Hz. Avoid power lines with excessive surges, since the unit may be damaged by line voltage in excess of 175 volts ac for even short durations.

c. Connect the preset unit to the TCG by use of cable W1 which is prepared according to Section 2.3. The cable is connected from J2 of the GPU to J1 of the TCG.

2.2 Airborne Time-Code Generator

a. Install the TCG in a position with base down. Other positions may result in a decrease of battery life. Caution: when charging battery, airborne TCG must be mounted with mounting plate down or battery will leak with possible damage to the circuit boards. See Figure 1.1 for mounting dimensions. Use four each 6-32 screws to restrain unit. (Note that the mounting plate may be removed and other more suitable plates used, if required. Consult factory for any additional mounting requirements.)

b. Airborne TCG Installation After Preset

In some applications, the generator is preset at some location remote to the aircraft and the generator carried to the aircraft and installed while operating. Do not operate control switch while installing. The unit must remain ON and OPERATING during installation. After securing mounting base, connect coax connectors to J2 and J3. The large multi-pin connector J1 is not used during normal operation. This connector is only used on the ground to preset the generator and charge the battery.

2.3 Cables

The TCG is connected to the GPU by a cable W1, which should not be longer than 15 feet in length. A longer cable requires shielding.

a. Cable W1

Connector P1 (TCG end) Deutsch DSM07-7-15P
Connector δ2 (GPU end) Deutsch DSM07-7-15S

Connect pins indicated below with a No. 20 stranded wire Type B20, or equal.

Connect pins 1, 2, 3, 4, 5, 6, 7, 8, 10, 13, 14, 16, 17, and 19.

Omit pins 9, 11, 12, 15, and 18.

b. Cable W2 (Power Cable - Preset Unit)

Connector P1 MS3106A-10SL-3S with cable clamp MS3057-4.

Connect power cord to pins as below.

Pin A	115-volt ac
Pin B	115-volt ac return
Pin C	Safety Ground

SECTION 3

OPERATION

3.0 OPERATION

3.1 Charge Battery

The TCG (Time-Code Generator) is operated only from the battery, so for reliable operation, the battery must be charged properly to obtain the operating time required. The following steps are to be observed.

3.1.1 Connect Airborne Time-Code Generator to Ground Preset Unit using cable W1 as in Section 2. Connect GPU to the power line. Perform the following steps on the GPU.

a. Turn switch S1 to ON. Nixie display lights up.

b. Place CHARGER switch S2 to ON.

c. Observe meter M1. Voltage should read between 5 and 9.6 volts, depending on state of charge.

3.1.2 Airborne Time-Code Generator

a. Place power switch to OFF during charge. The generator is still operable if the GPU is connected and the charge time is minimized with this switch OFF.

b. Keep S2 in OPERATE position at all times.

3.1.3 Keep charger at the ON position. The meter M1 should read 9.6 volts after the battery has charged. (Up to 16 hours, depending on state of charge). At 9.6 volts, the charger will cut out. If it is desired to keep unit at full charge for standby operation, charger switch should be placed into TRICKLE. This reduces the possibility of gassing off the water in the battery.

3.2 Preset Generator

The generator may be preset any time while it is connected to the GPU. Observe the following steps.

a. Place Mode Switch S3 into CLEAR position, then move to SET. The register display now reads all zeros.

b. Depress ADVANCE button until a forthcoming time is preset into the hours, minutes, and seconds register.

c. Place Mode Switch S3 into STOP position as soon as correct time is set into register.

d. Wait for clock time to equal register time. Turn Mode Switch S3 to RUN the moment this time is reached. The register will advance one second later.

e. Observe the operation of the display. The time will advance normally if the unit is operating correctly.

NOTE: Several seconds may elapse before a correct time is read after starting. This is due to the AGC in the reader adjusting to the signal level.

f. Turn TCG power switch to ON. IMPORTANT.

g. Remove the large connector from the TCG. The unit is now ready for operation.

3.3 Operation

The generator will operate for a period up to 24 hours on one charge, depending upon the condition of the battery and temperature of operation. The generator may be turned OFF any time during operation to conserve the battery charge. The charge will be substantially the same for several days or longer, depending on the condition of the battery. After usage, turn generator OFF. If the unit is to be stored for extended periods of time, run generator until battery is discharged to 5 volts, then turn OFF. Battery condition may be checked at any time by plugging in the GPU. Be sure charger switch is OFF, to check level of battery.

3.4 Emergency Operation

The generator may be run without a GPU for preset by placing the OPERATE-RESET switch into the RESET position and returning to OPERATE position. The unit counts from zero time through 24 hours and repeat. The battery must be in a charged condition for operating.

SECTION 4

MAINTENANCE

4.0 MAINTENANCE

4.1 Maintenance - Airborne Time-Code Generator

There are two items requiring maintenance in the TCG. The battery needs an occasional check for fluid level, and the oscillator requires a frequency adjustment.

4.1.1 Battery-Level Check

Charge battery to full capacity. (See Section 3.1). Remove mounting plate from bottom of unit by removal of the two rows of screws. Remove the left side cover nearest the power switch. This exposes the battery and oscillator. See Appendix I for detailed instructions on the care of the battery.

4.1.2 Oscillator Frequency Check

WARNING: Do not reset oscillator unless source frequency has a frequency of better than p part in 10^7. Observe frequency at the 100 kHz output connector. Adjust frequency by inserting a miniature screwdriver into the adjustment hole on the bottom of the unit. The mounting plate must be removed to reach this hole.

NOTE: Clockwise rotation of control decreases frequency with an adjustment sensitivity of one part in 10^{-6} for each half-turn of rotation.

Check operation by running unit against standard such as WWV for 24 hours, and observe time drift. Drift should be less than 50 ms in a normal room environment for a 24-hour period.

4.2 Preset Unit Check

4.2.1 Battery Charger Cut-Off Voltage Check

The GPU requires periodic checking to see if the meter and charging circuit is operating correctly.

Connect TCG as in paragraph 3.1, except remove terminal + from battery, as per paragraph 4.1.1. Place a 1000-ohm resistor between the red battery lead (disconnected from battery) and the return blank lead (ground). Connect a calibrated digital voltmeter across the resistor. Measure voltage. Adjust R5 in charger if voltage is not between 9.25 and 9.35 volts. Reconnect battery lead.

SECTION 5

THEORY OF OPERATION

5.0 GENERAL

The Airborne Time-Code Generator (TCG) performs the following functions:

a. Generates serial time-of-day code modulated on a 1000-Hz carrier.

b. Provides a 100-kHz sine-wave output.

c. Operates for 24 hours on self-contained battery.

d. Can be remotely preset and monitored by the Ground Preset Unit (GPU).

e. Internal TCG battery is charged by GPU.

The Ground Preset Unit (GPU) performs the following functions:

a. Contains reader circuit to decode and display serial time code.

b. Has control circuits to stop and preset TCG.

c. Contains battery charger and meter to charge and monitor the voltage of the internal TCG battery.

d. Operates from 115-volt, 50- to 400-Hz power.

5.1 Airborne Time-Code Generator

5.1.1 Input Circuits

The diagram of the chassis wiring is in Fig. 5.1. This shows the input panel connector J1, the oscillator Y1, the battery, series regulator, and bottom board connector. The battery voltage is reduced to +5 volts by the series regulator Q1. Panel switch S1 removes battery from circuit. Panel switch S2 is used as a reset of internal dividers. The generator starts at zero time when this switch is depressed and released. The oscillator output is a one-mHz (megaHertz) signal

which is a square wave of 4 volts amplitude from 0 volts to +4 volts. The battery voltage is 9.6 volts at full charge (with charger on), and drops to approximately 6 volts when the unit becomes inoperative.

5.1.2 Input-Output Board PC-1

The board PC-1 plugs into the connector P1 mounted on the chasis. The 19-pin connector is on one end of the board and connects this board PC-1 to the chassis and output connector wiring. The second board PC-2 plugs into the male pin which protrudes from the component side of this board. The input-output board PC-1 performs the following circuit functions:

a. Regulates battery voltage to +5 volts.

b. Divides 1-mHz signal to 1000 Hz.

c. Modulates code on 1000-Hz carrier.

d. Generates 100 kHz sine wave.

e. Provides termination and filters input signals from GPU.

5.1.2.1 Power Regulator

The output of the battery is regulated by the series regulator in the chassis. The regulator amplifier consists of Q1 and Q2, and associated circuits on PC-1. Q1A is an emitter-follower which has an almost constant output voltage driving the second zener diode CR2. The voltage from CR2 is fed to one side of the differential amplifier Q2A and Q2B. The base of Q2B is driven from the divider R13 and R12 which monitors the regulator output. Transistor Q1B is an amplifier which drives the external series regulator. Table 5.1 shows voltages at each transistor element for this board.

5.1.2.2 Divider - 1 mHz to 1000 Hz

This divider, located on the PC-1 board, is a flip-flop divider chain consisting of divide-by-five and divide-by-two circuits. All of the digital circuits use a low-power R-S Master-Slave integrated-circuit-type flip-flop. Data sheets for the items used are to be found in the Appendix. Note that all flip-flops are externally connected (Q to Reset gate input and $\overline{Q}$ to Set gate input) to provide the logic equivalent of the J-K flip-flop.

All logic circuit elements are powered from the +5 and ground supplies. Output logic levels are specifically described in the product bulletin but, generally, all signals described as a 0 logic level is between 0 and +0.2 volts, and a 1 logic level between +4 and +5 volts. Waveforms are very fast — in the order of 20 to 20 ns rise and fall times.

Divider waveforms are shown in Fig. 5.5. These waveforms are identical for all dividers, and differ only in pulse rates. Shown are the flip-flop waveforms for all the circuits.

The divider on PC-1 consists of a series of ÷ 5 and ÷ 2 stages. Flip-flops A1, A4, A2 are a ÷ 5 circuit, and A3 a binary divider stage. These divide the 1 mHz down to a 100 kHz square wave. This square wave is fed to the 100-kHz shaper. (See Section 5.1.2.4). The 100 kHz is further divided to 1 kHz by two successive ÷ 10 circuits comprised of A5, A7, A6 (÷ 5), A8 (÷ 2), A9, A11, A10 (÷ 5), and A12 (÷ 2). The output of A12 is a 1000-Hz square wave.

All dividers have a common reset line on pin 5. This reset line normally sits at +5 volts, held by R37. The reset signal, a 0, forces all flip-flops to logic 0 output on pin 12 (Q output). The reset is present when the unit is first preset by the GPU, or when S2 on the front panel of the TCG is pushed to RESET.

The output of A12 (1000-Hz square wave) is fed out to the connector P1 pin 6. It is jumpered back to the board on pin 22. This jumper may be removed during test and a 1-mc from the oscillator Y1 or external signal from a generator fed into pin 22. These higher-speed signals allow more rapid testing of the registers by speeding up operation of the slower stages.

5.1.2.3 Modulator

The code output from the generator is modulated on a 1000-Hz carrier. This modulator is found on PC-1 and consists of a sine-wave shaper, a modulator, an amplifier, and output stage. The 1000-pps square wave is filtered in L1, C8, C9 into a 1000-Hz sine wave. Capacitors C8 and C9 are selected so that the zero crossing of the sine wave is in synchronism with the input square wave. Transistor Q4 is a FET, and provides a high-impedance output for the tuned circuit. The modulator is a FET Q3. This transistor clamps a percentage of the sine wave to ground as selected by the modulation-ratio potentiometer R19. Modulation ratio can be set between 0 and 100 percent by use of this control. The modulated signal is fed into the differential amplifier Q5. The Q5B input is a feedback input, and is used to reduce the output impedance. The feedback is fed through the network R23, C13, and R22. The output

driver transistor is Q6B. The output is coupled by a capacitor C12 which eliminates the dc offset. Levels of quiescent voltage of all transistors may be found in Table 5.1. The output ac level is 3 volts peak-to-peak under no load. Output impedance is under one hundred ohms, but power limitation restricts the load resistor to greater than 1000 ohms.

5.1.2.4 Sine-Wave Shaper - 100 kHz

The 100 kHz square wave from flip-flop A3 is converted into a sine wave by the network L2 and C15, C16. The output of this network is fed to Q7 and then coupled to the output amplifier Q8A and the driver transistor Q8B. The output level is a 1 volt peak-to-peak, with an output impedance of approximately 250 ohms.

5.1.2.5 Input Filters

The signals used by the preset unit (GPU) to set in a desired time-of-day are filtered on this board PC-1 before being used by the register and divider. The filter capacitors C1 through C5 are used to protect the CLEAR, SET, ADVANCE SECONDS, ADVANCE MINUTES, and ADVANCE HOURS lines from external noise pulses on the preset line. The pull-up resistors R1 through R5 insure a logic 1 at the input of all gates when preset unit is disconnected.

5.1.3 Divider-Decoder Board PC-2

The divider-decoder board is used to divide the 1000-pps signal output from PC-1 down to 1 pps, and to generate waveforms used in the construction of the code format.

5.1.3.1 Divider Flip-Flops

The 1000-pps signal is divied by two $\div 2$ flip-flops A17 and A16. This is followed by $\div 5$ D15, D16, and D17. The output of D17 is 50 pps. This is followed by a $\div 2$ A12 giving 25 pps, the basic code rate. This 25 pps is divided down to 1 pps by two $\div 5$ chains A19, A20, A21, and A22, A23, A15.

5.1.3.2 Code Format

The function of the gates A1, A2, and A3 is to generate the basic code elements of code zeros, code ones, and code markers. These elements

are width-coded, and are inserted into the code format at appropriate times. The code elements have the following lengths:

Code 0	12 ms	
Code 1	24 ms	
Code Marker	36 ms	
Code Bit Period	40 ms	(25 pps)

The code format may be found in the Fig. 5.5, which shows all waveforms. Note that the trailing edge of each code element is "on time".

The code zeros (inverted) are viewed at pin 14 of the gate A1, code ones at pin 5 of A1, and markers at pin 10 of A3.

The code ones are gated by the output of the register scan gates coming into A1 pin 10. The code ones are on A1 pin 9. The output of A1 pin 8 is the code ones (inverted). The zeros and gated ones are "or" gated, and the output of A2 pin 14 is the code zeros and ones. These are gated in A2 pin 1 and 2 by the pin 10 output of A15. This removes all moculation from the code during the last 0.2 seconds of each second. The code marker is gated on once each second during code element 25, forming a marker with the trailing edge on time at the second. The combined and completed code is found at pin 5 of A2. This code is fed to the modulator through inter-board pin 3.

5.1.3.3 Decoder X signals

The divider A19, A20, A21 is a ÷ 5 with 25-pps input and 5-pps output. The flip-flops have five combinations in the divide-by-five cycle. These five combinations are decoded into a five-line output, each one for a given period of 40 ms. Only one line is a "one" at any time. See waveforms, Fig. 5.5.

5.1.3.4 Decoder Y Code Group Gates

The dividers A22, A23, and A15 form a ÷ 5 chain with 5-pps input and 1-pps output. These five combinations are decoded into five separate signals which are observed at the outputs of the gates A7 pin 8 (Y0), A7 pin 14 (Y1), A6 pin 8 (Y2), A6 pin 14 (Y3), and A15 pin 12 (Y4). These signals are used to gate out groups of code scan outputs. The group G0 is gated by Y0, G1 by Y1, G2 by Y2, and G3 by Y3. These four scan-gate groups are obtained from the register board PC-3. The outputs of these are "or" gated, and the output of A14 pin 10 are the scan-gate outputs which gate out the code "ones".

5.1.3.5 Register Seconds Advance

The inputs to the register board PC-3 are through A18* pin 5 and A18* pin 8. The double inversion does not modify the 1-pps signal, except during the preset. Normally, the inputs of A18 pin 6 and A18 pin 9 are "ones". During preset the SET line is a zero, making the output of A18 pin 5 a one. This enables the following gate, and successive grounding of the ADVANCE SECONDS line advances the seconds register one second for each push of the preset switch. Since the code scan must take place before the new number appears in the register display, the advance of the numbers must be done slowly to prevent passing the desired number.

*On PC-2 board.

5.1.4 Register Board PC-3

The register board is the third board in the stacked assembly. It contains the flip-flop dividers which generate the BCD (binary coded decimal 8 - 4 - 2 - 1) time-of-day. The condition (zero or one) of the register flip-flops are scanned once each second to generate the new second-minute-hour time-of-day code.

5.1.4.1 Register Flip-Flops

The time is stored in the register counter flip-flops. The dividers are weighted in a BCD 1-2-4-8 format. The seconds divider is a divide-by-ten, followed by a divide-by-six. The waveforms are on the Waveform Drawing Fig. 5.5. The designation of each flip-flop, such as 10S (10 seconds), indicates the time at which the flip-flop first is set, and is also the weight of the code-bit element.

The register counts up to 23:59:59 and recycles to zero. The final divider chain is a divide-by-twenty-four counter to provide for the hours cycle.

5.1.4.2 Code-Scan Gates

The scan gates are used to generate the "ones" information in the output code. For example, if the 10S (ten-second) flip-flop is set, the corresponding bit in the code is a "one". In like manner, all of the 20 bits in the code are controlled. The scan gate opens the path from the flip-flop to the "one gate" on PC-2 over the first twenty periods of the twenty-five-pulse-per-second code. The scan gates are in a series sequence.

The two-second (2S) flip-flop, for example, is scanned by the X3 signal. The output of this gate appears on pin 6 of the interboard connectors as G3 (Group 3). The G3 signal is gated on PC-2 at time Y3. The effect is to open the gate to the 2S flip-flop at X3, Y3 time. The twenty gates are opened in sequence so that the 20 flip-flops are scanned in order from high order to low order.

5.2 Ground Preset Unit (Dwg R 4896-71006)

The Ground Preset Unit operates during the battery charge and time preset periods. The following circuits will be discussed in detail:

a. Logic power supply.

b. Battery charger.

c. Preset circuits.

d. Reader-display logic.

e. High-voltage regulator.

In addition, the individual cards are described in detail.

5.2.1 Logic Power Supply (Dwgs 4896-71001 and 4896-71002)

The logic power supply provides the regulated +5 volts for the operation of digital integrated-circuit boards. In addition, it provides an unregulated +15 and -15 volts, which are used by the battery charger and AGC boards.

The power transformer is provided with ±5 percent taps for adjustment of incoming voltage for marginal power operation, although the normal operating range is from 105 to 125 volts ac.

The transformer has the following specifications:

Pins	Winding	Voltage
1 (2), 3 (4)	Primary	115 volts, 50 to 400 Hz, ±5% taps
5, 6, 7	Secondary No. 1	7.0-0-7.0 volts, 5 amperes
8, 9, 10	Secondary No. 2	12.0-0-12.0 volts, 0.2 amperes
11, 12	Secondary No. 3	160 volts, .030 amperes

All voltages are rms read across windings with an isolated meter.

The output of secondary is full wave rectified by CR1 and CR2 with filter capacitor C1. The output is approximately 9 volts, unregulated. This voltage is regulated by the series pass transistor Q1 with A2 as an emitter-follower driver.

The plus and minus 15-volt supplies are rectifed by full-wave rectifiers on the regulator board. The output of the plus 15-volt supply is from pin 13 on A108 and filtered by C2. This current is used to charge the battery in the TCG. The minus 15-volt is from pin 16 of A108. This voltage is used as a bias on the battery monitor and as a supply for the AGC board A101.

5.2.2 Battery Charger

The battery charger is a simple resistor current-limited supply with a shunt regulator. The basic charge current comes through a 35-ohm resistor R3 for a nominal 200-ma charge current for normal CHARGE setting, or a 330-ohm R4 for a 20-ma trickle charge. The output of the battery is monitored by the meter and the viewing network CR4 and R5. The potentiometer R5 is adjusted to turn on the shunt regulator transistor Q4 when the voltage of the battery reaches the peak charge value of 9.3 volts. The base of the transistor Q4 is held negative until the battery nears the full charge voltage. At this point, the Q4 is turned on until all of the charger current is shunted by this transistor. The Appendix contains complete instructions on care and maintenance of the battery.

5.2.3 Preset Circuit Operation

The switch S3 is used in conjunction with the pushbutton switches S4, S5, and S6 in setting a desired time into the airborne time-code generator. The following listing shows the effect of each position of S3 on the airborne time-code generator.

a.	CLEAR	Register reset to 0, Divider reset to 0, no code output.
b.	SET	Divider operating, code output, register not advancing at 1 pps, register may be advanced by pushbuttons S4, S5, or S6.
c.	STOP	Divider reset to 0, register static at preset number, no code out.
d.	RUN	Generator operating independently. All input circuits open.

Note that while in the STOP position, the code is not generated and the reader does not function. The number last read will be in the display register. When the unit is switched to RUN, a short time may elapse for the reader to be synchronized to the incoming code before the correct number appears. (AGC time response).

5.2.4 Reader Logic

The reader logic is comprised of diode-transistor integrated-circuit packages mounted on seven circuit boards. The exact specifications for each package may be seen in the Appendix. However, as a general rule, the logic modules operate from the +5-volt to group supply. All levels of signals are 0 to +0.2 volts for a logic 0, and 4.0 to 5.0 for a logic 1. The linear amplifiers on the AGC card (A101) are operated from +12 and -6 volts derived from the + and -15-volt supplies. The basic logic rules are to be found in the logic circuit specifications, and are not repeated here. Waveforms are presented with each circuit card description.

5.2.4.1 Overall Operation

The reader unit consists of the following logic divisions:

a. Automatic Gain Control - Trigger Board A101 (Dwg D4876-70506)

b. Code Decoder Board A102 - (Dwg 101-40121)

c. Counter (÷ 10) A103 - (Dwg 101-40409)

d. Divider-Decoder Board A104 - (Dwg 101-40122)

e. Time Register - Seconds-Minutes-Hours A105, A106, A107 (Dwg 101-40106)

The function of the reader is to read the incoming code bit by bit, into the display register (scan-in code). The code is generated during the first 0.8 seconds of each second, and defines the time at the beginning of that code frame. (See time-code format.) During the first second, the code is read into the display one element at a time, so that at the end of 0.8 seconds, the time at 0.0 seconds is displayed. At the start of the next second, the time in the register is updated by one second, so that the time display is "in phase" with the real time as generated.

Since the updated time in the register is identical to the time coded in the time code, the scanning in of the time into the display register does not change the number in the display unless the incoming time bit is in error. Errors in the generated code are observed as changes in the display during the second after the normal advanced time.

5.2.4.2 Automatic Gain Control - Trigger Board A101 (Dwg D4876-70506)

The AGC trigger board receives the incoming code and detects two points on the wave with the level triggers. One trigger is set at the zero crossing level, so that each cycle is reproduced as a square-wave output. The second trigger is set to trigger on the "large cycles" of the code. The outputs of this trigger are only present when the tops of the large cycle are present, and only for one polarity. That is, the positive cycle top is detected and the negative cycle top is not. The outputs of each cycle trigger (EC) and large-cycle trigger (LC) are fed to the code-detector board. The output signal is approximately 2 volts peak-to-peak over the AGC range.

5.2.4.3 Code-Detector Board A102 (Dwg 101-40121)

The code-detector board receives the LC trigger and EC trigger and decodes these signals into weighted code elements in zeros, ones, or markers. The outputs of the board are shown in Fig. 5.6. These outputs occur a millisecond after the end of the code bit. Since all the code bits occur with trailing edge "on time", these outputs all occur at the same relative time at a 25-pps rate. The pulse A1 (pin 14 of A102) occurs for each code bit along with C0 (pin 15 of A102) if the bit was a zero, C1 (pin 11) if the bit was a one, or M1 (pin 12) if the bit was a one-second marker. The jumpers from D1, D2, D4, and D8, and the complements are connected to the gates at the inputs of the three-code element flip-flops which determine the presence of a zero, one, or marker. The large-cycle counter is composed of the two divide-by-two counters, followed by the D1 FF, D2 FF, D4 FF, and D8 FF, all connected as binary counters. The three-code element flip-flops 0, 1, and M1 flip-flops are set as the large-cycle counter arrives at numbers corresponding to the cross-over count between the length of a zero, one, and marker-code element. The listing below shows the setting of the code-element gates.

Large-Cycle Counter	Function
8	Set "0" flip-flop
20	Reset "0" flip-flop - Set "1" flip-flop
32	Reset "1" flip-flop - Set Marker flip-flop

Therefore, the reader determines that the code element is a binary zero if the large-cycle count is between 8 and 20 (zeros are 12-ms long); a binary "one" is between counts of 20 and 32 (ones are 24-ms long); a marker from count of 32 up (markers are 36-ms long). These counters provide a large tolerance for noise, and should read the code with great precision.

5.2.4.4 Cycle Counter A103
(Dwg 101-40409)

The cycle counter is a BCD-connected, divide-by-ten counter which is used to count each cycle. The output of this counter is used to advance the divider-decoder board counter. The cycle counter has a 1000-pps input which is the EC signal from the code trigger. The counter output is at 100 pps (every 10 ms). This counter is reset by the end of code-bit signal every 40 ms.

5.2.4.5 Divider-Decoder Board A104
(Dwg 101-40122)

The divider-decoder board is used to generate a group of five x andfive Y signals which together define any of the twenty-five code-bit periods in the time cycle. The binary counters at the input of this board divide the 100-pps down to 25 pps, the code-bit rate. The three flip-flops in the divide-by-five reduce the rate to 5 pps. The five states of these flip-flops are decoded into the X0, X1, S2, X3, and X4 signals. The last three flip-flops on A104 divide the 5-pps signal down to 1 pps. The states of these flip-flops are also decoded into five Y signals, Y0 through Y4. The X and Y signals are used to scan in the time-code bits into the respective flip-flops. The combination of X and Y signals define any of the 20 code-bit positions.

5.2.4.6 Register Boards A105, A106, A107
(Dwg 101-40106)

The three register boards each consist of a BCD-connected divide-by-sixty counter (or divide-by-twenty-four for A107). The flip-flops which constitute the storage elements in this counter each have a parallel entry gate which allows individual set or clear of any flip-flop element in the counter chain. This parallel entry is controlled in time sequence by the X and Y counter which opens each series of parallel entry gates according to the weight of the input-code bit. If the bit is a zero, the corresponding flip-flop is cleared; if a one, the flip-flop is set. The purpose of connecting

these flip-flops in a counter chain is to provide for advancing the count in the register at the second so that the register display corresponds to the real time represented by the code.

The entry into the register are the C1 or C0 lines which represent the code ones and code zeros. The C1 line becomes a logic 1 when the flip-flop corresponding to the code element is to be set and the C0 line becomes a logic 1 when the flip-flop is to be cleared.

5.2.4.7 Display Drivers V1 to V6

The displays and drivers are mounted behind the front panel, and display the contents ot the register. The flip-flop outputs and complements are fed to the Nixie driver modules*. The high voltage (+200 V) is fed into pins 11 of each module, and the logic return for the decoders is on pin 12, which sits at +2 volts. The zener diode 1N702, mounted behind the V1 driver, provides this bias for the Nixie driver.

*Burroughs Bipco Type 8211-P (Data Sheet in Appendix)

Table 5.1

TRANSISTOR VOLTAGES

TRANSISTOR		ELEMENT VOLTAGE		
Symbol	Type	Emitter	Base	Collector
Q1A	MD3251AF	5.0	4.4	0
Q1B	MD3251AF	$E_{Battery}$	$E_{Battery}$-1.0	5.0
Q2A	SP8888	3.0	3.6	$E_{Battery}$-1.0
Q2B	SP8888	3.0	3.6	+5
Q3	2N2843	0	0 V	0
Q4	2N2608	+2.5	+5.0	0
Q5A	MD3251AF	+3.0	+2.4	+0.6
Q5B	MD3251AF	+3.0	+2.4	0
Q6A	SP8888	0	+0.6	+3.0
Q6B	SP8888	+2.4	+3.0	+5
Q7	2N2608	+4.5	+5.0	0
Q8A	SP8888	+1.5	1.8	3.5
Q8B	SP8888	+3.0 V	3.5	+5.0

NOTE: All voltages measured with S2 in RESET position.

APPENDIX I

BATTERY CHARACTERISTICS

1.0 INTRODUCTION

1.1 The YARDNEY SILCAD cell is a silver-cadmium cell which differs considerably from the more familiar lead-acid cell and, to a certain extent, from other alkaline cells such as nickel-cadmium, nickel-iron, etc. The silver-cadmium cell also differs in operation and performance from the Yardney Silvercel (silver-zinc) cell.

Silver (the positive electrode) and cadmium (the negative electrode) are employed as the active elements, while the electrolyte is a strong solution of postassium hydroxide (KOH). The techniques for operating the Yardney Silcad cell are quite simple, and should be followed closely for optimum performance.

1.1.1 We recommend that the entire instruction be read carefully before using the Yardney Silcad cell.

2.0 PRECAUTIONS

2.1 For Handling or Accidental Exposure to Electrolyte

2.1.1 General Comments

The electrolyte (a strong solution of potassium hydroxide) is alkaline and corrosive. It should be handled with care. If neglected, the electrolyte will cause serious burns when it is permitted to come in contact with the eyes or skin. Alkali-proof apron, rubber gloves and splash-proof goggles or a face mask are recommended for personnel engaged in the filling and servicing of Silcad cells.

2.1.2 Antidotes, Internal

Give large quantities of water and a weak acid solution such as vinegar, lemon juice, or orange juice. Follow with one of the following: white-of-egg, olive oil, starch water, mineral oil, or melted butter. Obtain medical attention at once.

2.1.3 Antidotes, External

2.1.3.1 Thoroughly flush the affected area (skin or eyes) with large quantities of clean, lukewarm water. Neutralize, if possible, with a saturated solution of boric acid. Vinegar, lemon juice, acetic acid, etc., may be used on the skin, but should never be used for the eyes. Obtain medical attention at once.

2.1.4 Washing Glassware

The electrolyte is somewhat corrosive to glass. All beakers and syringes should be thoroughly washed with water following their use.

2.1.5 Carbon-Dioxide Absorption

Store the electrolyte in closed alkali-resistant containers, as it absorbs carbon dioxide from the air. Prolonged exposure to the air will impair the properties of the electrolyte.

2.1.6 CAUTION: Do not, under any circumstances, attempt to use any type of electrolyte other than the special electrolyte furnished with the Yardney Silcad cell. Other types of electrolyte will destroy it.

2.2 For Handling the Cell

2.2.1 The cell is capable of supplying unusually high currents if it is accidentally shorted. A prolonged short may cause serious burns to personnel and may destroy the cell. To avoid accidental short circuits, all tools used in connection with the cell or within close vicinity of the cell must be properly insulated with a double layer of electrical tape or varnish.

CAUTION

1. The cell shall be kept upright under normal handling and operating conditions.
2. When assembling a group of unsealed cells into a battery, do not exceed the recommended maximum torque for tightening the top terminal nuts.
3. Only the uppermost of the nuts on each of the cell's terminals should be removed for assembly. The lower nut, which rests on the cell cover, forms an integral part of the terminal-to-cover seal; removal of the lower nut may break this seal.

3.0 CHARGING PRACTICES

3.1 For best results, the Hardney Silcad cell should be charged in an ambient temperature of 70 to 90 degrees F. Charging can be accomplished by either the Constant-Current or Modified Constant-Potential method. While the Constant-Current method provides the fastest means of recharging and the best pre-performance check of expected operation, the Modified Constnat-Potential method requires much less personal attention, and can be accomplished with equipment of a much less complex nature.

3.1.1 Constant-Current Charge Method

Charge the cell at the rate specified in the attached Appendix until the cell voltage increases to the specified value. The cell voltage is to be measured at the cell terminals, while the cell is being charged.

3.1.2 Modified Constant-Potential Charge Method

This type of charge system consists of a constant-voltage supply modified by a current-limiting circuit or a resistor. The system should be designed in such a manner that when the cell has reached the final (cut-off) voltage specified in the attached Appendix, the current flowing through the cell will not exceed the recommended maximum; further, the initial surge current should not exceed the recommended maximum value. As the charge progresses, the current will gradually taper off from the initial value. Charge the cell in this manner until the cell voltage increases to the value specified in the Appendix. The cell voltage is to be measured at the cell terminals, while the cell is being charged.

4.0 DISCHARGE PRACTICES

4.1 The Yardney Silcad cell is designed for low to medium rate discharges. For optimum performance, the cell should not be discharged continuously at a rate higher than in the maximum value specified in the attached Appendix.

5.0 CELL MAINTENANCE

5.1 A minimum of maintenance is usually required to keep the Silcad cell in optimum operating condition. The cell vent hole and vent valve (for unsealed cells) should be occasionally inspected to be sure they are not clogged.

APPENDIX II

FUNCTIONAL USE

Constant-Current Charge Rate	0.14 amperes
Maximum Initial Charge Rate (Modified C.P. Charge)	0.28 amperes
Maximum Final Charge Rate (Modified C.P. Charge)	0.01 amperes
Final (Cut-Off) Voltage	1.60 volts
Recommended Maximum Continuous Discharge Rate	2.0 amperes
Nominal Capacity	2.0 ampere/hours
Nominal Load Voltage	1.1 volts
Final (Cut-Off) Discharge Voltage*	0.6 volts
Maximum Torque (Top Terminal Nuts - Unsealed Cells)	6-10 In/Lbs

*NOTE: If cells are assembled into a series-connected battery, final (cut-off) voltages should be as follows:

Charge: 1.55 x number of cells in battery
Discharge: 0.9 x number of cells in battery

APPENDIX III

PARALLEL OUTPUT OPTION

HI-4896-1A

Miniature time-code generators may have a parallel output option, and are readily identified by a rectangular output connector.

Figure AIII-1, AIII-2, AIII-3 and AIII-4 document the changed units. A fourth card, PC-4, is added, which provides parallel output buffers for twenty bits of BCD time, 1 pps, and ground. Logic one is +2.4 to +5.5 V, logic zero is zero to +0.3 V. Drive capability on each line is -1.8 milliamperes maximum when at logic zero. Output impedance when at logic one is about one kilohm. Outputs are short-circuit-proof to ground. Short-circuit current is between 3 and 15 milliamperes. 1 pps has transition from high to low on time.

NEW PRODUCT BULLETIN

This announcement provides preliminary engineering information on new Texas Instruments products. Definitive specifications are now being prepared for publication.

SERIES 54L, 74L

SOLID CIRCUIT® SEMICONDUCTOR NETWORKS†

LOW-POWER TRANSISTOR-TRANSISTOR LOGIC CIRCUITS

FOR AEROSPACE COMPUTER AND CONTROL SYSTEM APPLICATIONS

description

Series 54L integrated circuits have been designed and characterized for aerospace applications where high d-c noise margin, low power dissipation, and high reliability are important system considerations. Definitive specifications are provided for operating characteristics over the full military temperature range of -55°C to 125°C. Series 54L devices are available with additional high-reliability processing as specified in General Specification for SNR, SNT SOLID CIRCUIT Semiconductor Networks. This logic series includes the basic gates, flip-flop elements, and storage elements needed to perform most functions of general-purpose digital systems.

Series 74L circuits are characterized for operation over the temperature range of 0°C to 70°C.

features

LOW SYSTEM COST

- maximum number of circuits per package through use of 14-lead package
- alternate package configurations available

OPTIMUM CIRCUIT PERFORMANCE

- very low power dissipation — typically 1 mW per gate at 50% duty cycle
- relatively high speed — typical gate propagation delay time of 33 ns
- high d-c noise margin — typically one volt at 25°C
- low output impedance provides low a-c noise susceptibility
- waveform integrity over full range of loading and temperature conditions
- fan-out — 10 Series 54L loads
  — 1 Series 54 load and 2 Series 54L loads
  — 1 Series 54H load
- a standard Series 54 output will drive 40 Series 54L loads

CONTENTS

† Patented by Texas Instruments

SC-10218
JULY 1967
REPLACES SC9592, MARCH 1967

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

PRINTED IN U.S.A.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	8 V
Input Voltage V_{in} (See Notes 1 and 2)	5.5 V
Operating Free-Air Temperature Range: Series 54L	-55°C to 125°C
Series 74L	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

logic definition

Series 54L and 74L logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

LOW VOLTAGE = LOGICAL 0
HIGH VOLTAGE = LOGICAL 1

unused gates

Inputs of unused gates should be connected to ground. This sets the gate output to logical 1 to ensure minimum power dissipation.

unused inputs

Unused inputs, including preset and clear, must be maintained at a positive voltage greater than 2.4 V but not to exceed the absolute maximum rating of 5.5 V.

Some possible ways of handling unused inputs are:

a. Connect unused inputs to V_{CC} or a supply voltage of 2.4 V to 5.5 V.
b. Connect unused inputs, except preset or clear, to a used input of the same gate if maximum fan-out of the driving output will not be exceeded.
c. Connect unused inputs to the logical "1" output of an unused gate.

input-current requirements

Input-current requirements reflect worst-case V_{CC} and temperature conditions. Each input of the multiple-emitter input transistor requires that no more than -0.18 mA flow out of the input at a logical 0 voltage level; therefore, one load (N = 1) is -0.18 mA maximum. Each input (except the SN54L71R/SN74L71R, SN54L72R/SN74L72R, and SN54L73R/SN74L73R clock inputs) requires current into the terminal at a logical 1 voltage level. This current is 10 μA maximum for each emitter input. See fan-out capabilities (below) and typical characteristics (page 23) for flip-flop clock input current requirements. Currents into the input terminals are specified as positive values.

fan-out capability

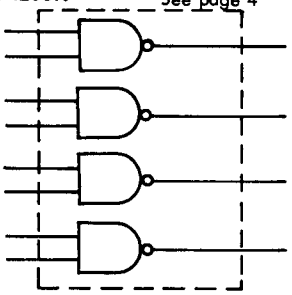
Fan-out (N) reflects the ability of an output to sink current from a number of Series 54L or 74L loads at a logical 0 voltage level and to supply current at a logical 1 voltage level. Each output is capable of sinking current or supplying current to 10 Series 54L/74L loads (N = 10), or one Series 54/74 load and two 54L/74L loads. Load currents (out of the output terminal) are specified as negative values.

A Series 54 or 74 output is capable of sinking current or supplying current to 40 Series 54L or 74L loads (N = 40). The buffer gate (SN5440/SN7440) is capable of driving 120 Series 54L/74L loads. The carry output ($\overline{C_{n+1}}$) of the SN5480/SN7480 is capable of driving 20 Series 54L/74 loads and the A* and B* nodes may be used to drive 12 loads.

When fanning out into SN54L71R/SN74L71R, SN54L72R/SN74L72R, or SN54L73R/SN74L73R clock inputs no load current (I_{load}) is drawn at $V_{in(clock)}$ = 2.4 V. Therefore, the fan-out limitation is the I_{sink} capability of the driving output. A Series 54/74 output will sink sufficient current to drive 44 clock inputs (88 loads), and the SN5440/SN7440 will sink sufficient current to drive 133 clock inputs (266 loads). The Series 54L/74L output is capable of driving five 54L/74L clock inputs and one additional load.

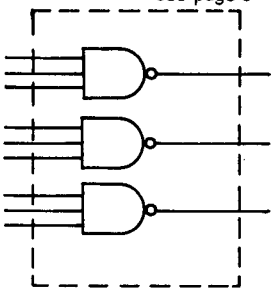
standard line summary

SN54L00R
SN74L00R
See page 4



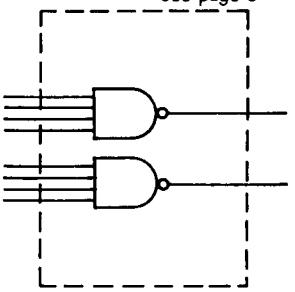
QUADRUPLE 2-INPUT
POSITIVE NAND GATE

SN54L10R
SN74L10R
See page 5



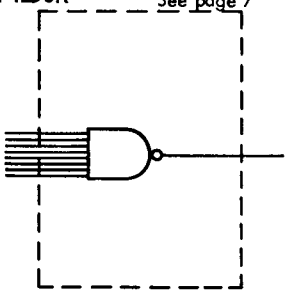
TRIPLE 3-INPUT
POSITIVE NAND GATE

SN54L20R
SN74L20R
See page 6



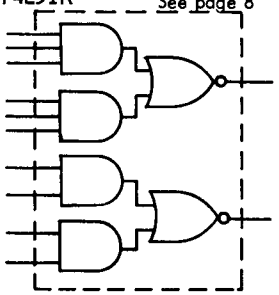
DUAL 4-INPUT
POSITIVE NAND GATE

SN54L30R
SN74L30R
See page 7



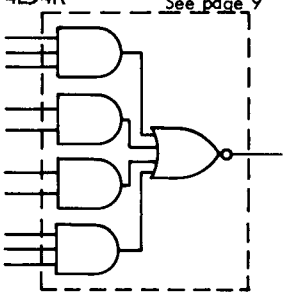
8-INPUT
POSITIVE NAND GATE

SN54L51R
SN74L51R
See page 8



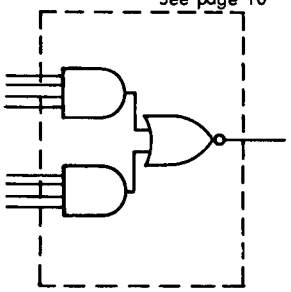
DUAL 2-WIDE 3-INPUT, 2-WIDE
2-INPUT AND-OR-INVERT GATE

SN54L54R
SN74L54R
See page 9



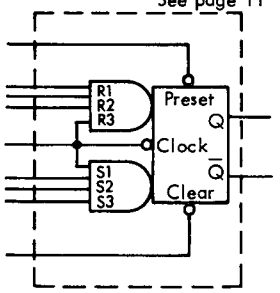
4-WIDE 3-2-2-3-INPUT
AND-OR-INVERT GATE

SN54L55R
SN74L55R
See page 10



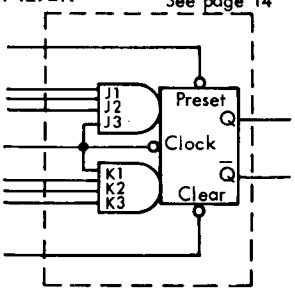
2-WIDE 4-INPUT
AND-OR-INVERT GATE

SN54L71R
SN74L71R
See page 11



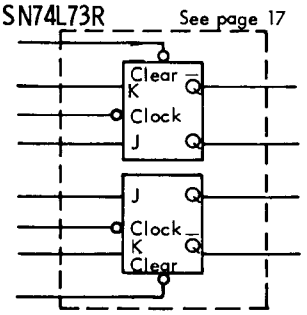
R-S MASTER-SLAVE
FLIP-FLOP

SN54L72R
SN74L72R
See page 14



J-K MASTER-SLAVE
FLIP-FLOP

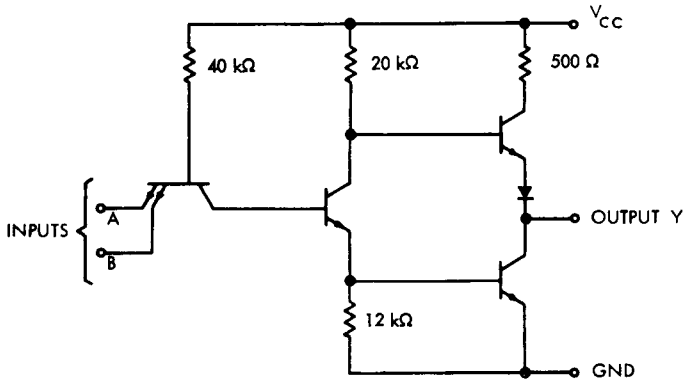
SN54L73R
SN74L73R
See page 17



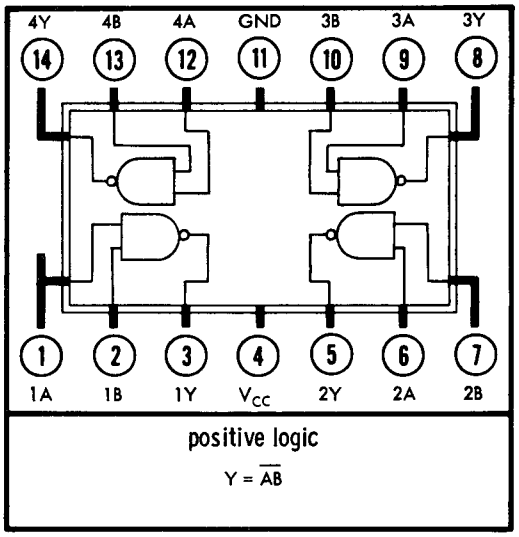
DUAL J-K
MASTER-SLAVE FLIP-FLOP

TYPES SN54L00R, SN74L00R
QUADRUPLE 2-INPUT POSITIVE NAND GATE

schematic (each gate)



Component values shown are nominal



recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L00R	4.5	5	5.5	V
SN74L00R	4.75	5	5.25	V
Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L00R	-55	25	125	°C
SN74L00R	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

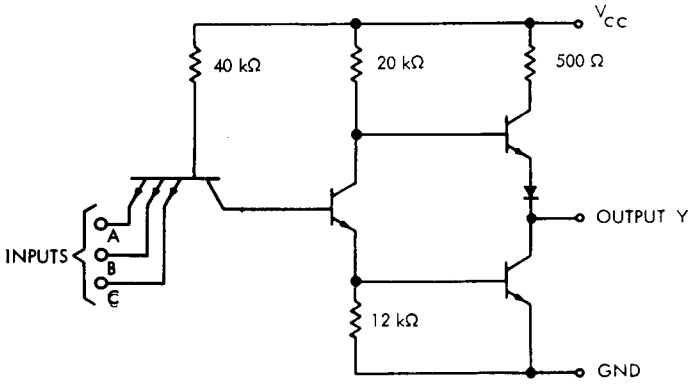
PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
$V_{In(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN,	$V_{out(0)} \leq 0.3$ V	2			V
$V_{In(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = MIN,	$V_{out(1)} \geq 2.4$ V			0.7	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -100 μA	V_{In} = 0.7 V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 2 mA	V_{In} = 2 V,			0.3	V
$I_{In(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.3 V			-0.18	mA
$I_{In(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4 V			10	μA
		V_{CC} = MAX,	V_{in} = 5.5 V			100	μA
I_{OS}	Short-circuit output current	V_{CC} = MAX,	V_{in} = 0, V_{out} = 0	-3		-15	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	V_{CC} = 5 V,	V_{in} = 5 V		0.29	0.46	mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	V_{CC} = 5 V,	V_{in} = 0		0.11	0.18	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, see figure 1

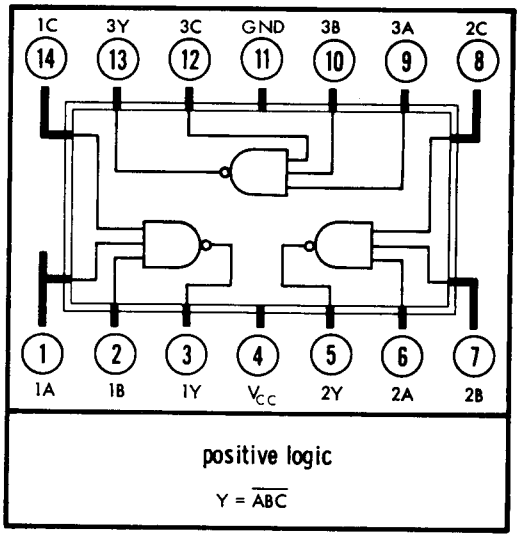
PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_l = 50 pF		31	60	ns
t_{pd1}	Propagation delay time to logical 1 level	C_l = 50 pF		35	60	ns

† For conditions shown as MIN or MAX, use the MIN or MAX value specified under recommended operating conditions for the applicable device type.

schematic (each gate)



Component values shown are nominal



recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L10R	4.5	5	5.5	V
SN74L10R	4.75	5	5.25	V
Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L10R	-55	25	125	°C
SN74L10R	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
$V_{In(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN,	$V_{out(0)} \leq 0.3$ V	2			V
$V_{In(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = MIN,	$V_{out(1)} \geq 2.4$ V			0.7	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -100 μA	V_{in} = 0.7 V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 2 mA	V_{in} = 2 V,			0.3	V
$I_{In(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.3 V			-0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4 V			10	μA
		V_{CC} = MAX,	V_{in} = 5.5 V			100	μA
I_{OS}	Short-circuit output current	V_{CC} = MAX,	V_{in} = 0, V_{out} = 0	-3		-15	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	V_{CC} = 5 V,	V_{in} = 5 V		0.29	0.46	mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	V_{CC} = 5 V,	V_{in} = 0		0.11	0.18	mA

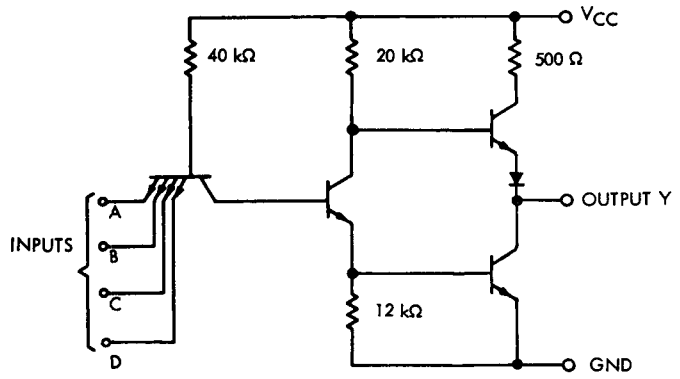
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, see figure 1

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_l = 50 pF		31	60	ns
t_{pd1}	Propagation delay time to logical 1 level	C_l = 50 pF		35	60	ns

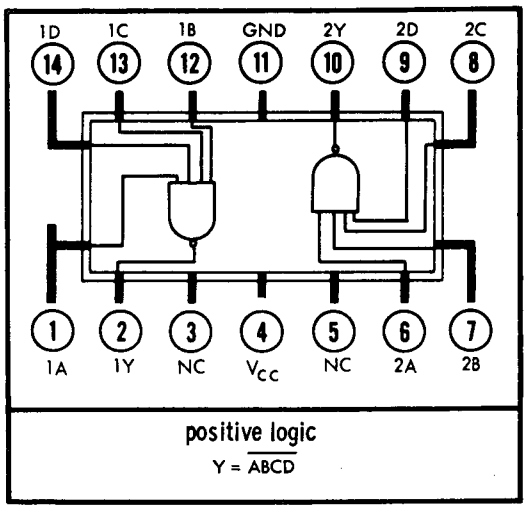
† For conditions shown as MIN or MAX, use the MIN or MAX value specified under recommended operating conditions for the applicable device type.

TYPES SN54L20R, SN74L20R
DUAL 4-INPUT POSITIVE NAND GATE

schematic (each gate)



Component values shown are nominal



recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L20R	4.5	5	5.5	V
SN74L20R	4.75	5	5.25	V
Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L20R	-55	25	125	°C
SN74L20R	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

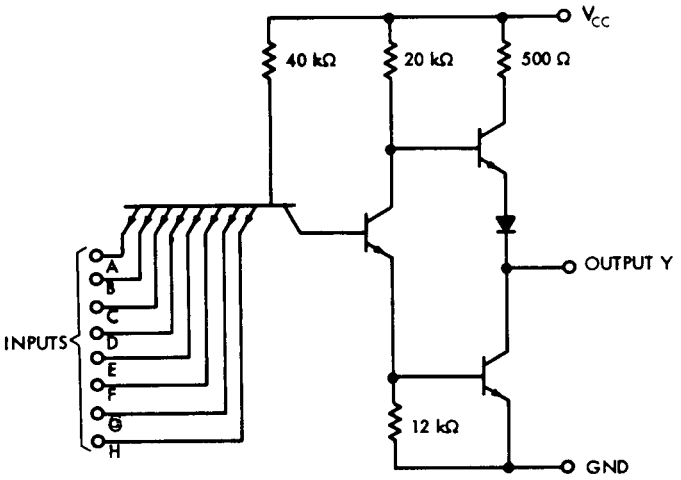
PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
$V_{In(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN,	$V_{out(0)} \leq 0.3$ V	2			V
$V_{In(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = MIN,	$V_{out(1)} \geq 2.4$ V			0.7	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -100 μA	V_{in} = 0.7 V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 2 mA	V_{in} = 2 V,			0.3	V
$I_{In(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.3 V			-0.18	mA
$I_{In(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4 V			10	μA
		V_{CC} = MAX,	V_{in} = 5.5 V			100	μA
I_{OS}	Short-circuit output current	V_{CC} = MAX,	V_{in} = 0, V_{out} = 0	-3		-15	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	V_{CC} = 5 V,	V_{in} = 5 V		0.29	0.46	mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	V_{CC} = 5 V,	V_{in} = 0		0.11	0.18	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, see figure 1

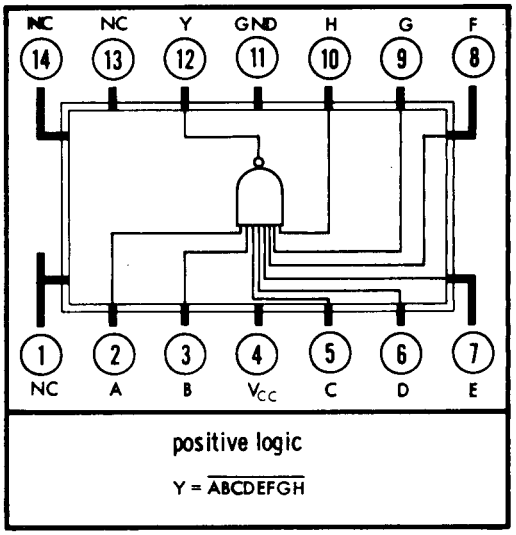
PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_l = 50 pF		31	60	ns
t_{pd1}	Propagation delay time to logical 1 level	C_l = 50 pF		35	60	ns

† For conditions shown as MIN or MAX, use the MIN or MAX value specified under recommended operating conditions for the applicable device type.

schematic



Component values shown are nominal



positive logic

$Y = \overline{ABCDEFGH}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L30R	4.5	5	5.5	V
SN74L30R	4.75	5	5.25	V
Fan-Out From Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L30R	-55	25	125	°C
SN74L30R	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
$V_{In(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN,	$V_{out(0)} \leq 0.3$ V	2			V
$V_{In(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = MIN,	$V_{out(1)} \geq 2.4$ V			0.7	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -100 μA	V_{in} = 0.7 V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 2 mA	V_{in} = 2 V,			0.3	V
$I_{In(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.3 V			-0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4 V			10	μA
		V_{CC} = MAX,	V_{in} = 5.5 V			100	μA
I_{OS}	Short-circuit output current	V_{CC} = MAX,	V_{in} = 0, V_{out} = 0	-3		-15	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = 5 V,	V_{in} = 5 V		0.29	0.46	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = 5 V,	V_{in} = 0		0.11	0.18	mA

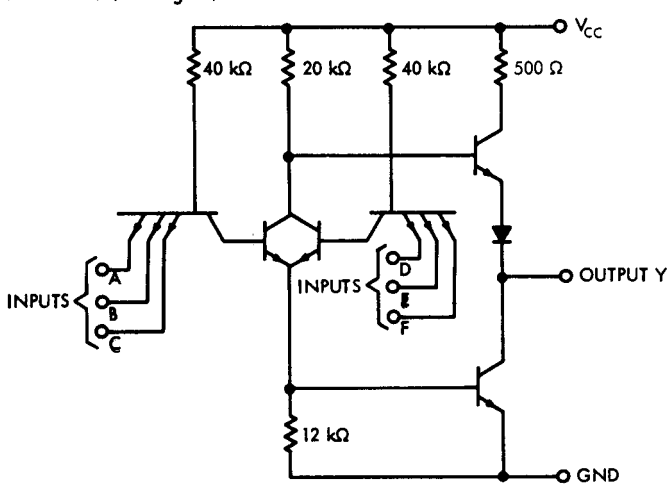
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, see figure 1

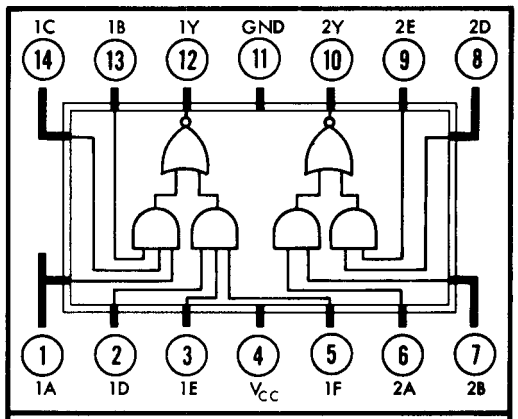
PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_l = 50 pF		70	100	ns
t_{pd1}	Propagation delay time to logical 1 level	C_l = 50 pF		35	60	ns

† For conditions shown as MIN or MAX, use the MIN or MAX value specified under recommended operating conditions for the applicable device type.

TYPES SN54L51R, SN74L51R
DUAL 2-WIDE 3-INPUT, 2-WIDE 2-INPUT AND-OR-INVERT GATE

schematic (each gate)





positive logic

$1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$

$2Y = \overline{(2A \cdot 2B) + (2D \cdot 2E)}$

NOTES: 1. Component values shown are nominal.
2. Inputs C and F are available on gate 1 only.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L51R	4.5	5	5.5	V
SN74L51R	4.75	5	5.25	V
Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L51R	-55	25	125	°C
SN74L51R	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
$V_{In(1)}$	Logical 1 input voltage required at all input terminals of either AND section to ensure logical 0 at output	V_{CC} = MIN,	$V_{out(0)} \leq 0.3$ V	2			V
$V_{In(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	V_{CC} = MIN,	$V_{out(1)} \geq 2.4$ V			0.7	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -100 μA	V_{in} = 0.7 V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 2 mA	V_{in} = 2 V,			0.3	V
$I_{In(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0			-0.18	mA
$I_{In(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4 V			10	μA
		V_{CC} = MAX,	V_{in} = 5.5 V			100	μA
I_{OS}	Short-circuit output current	V_{CC} = MAX		-3		-15	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	V_{CC} = 5 V,	V_{in} = 5 V		0.38	0.59	mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	V_{CC} = 5 V,	V_{in} = 0		0.22	0.36	mA

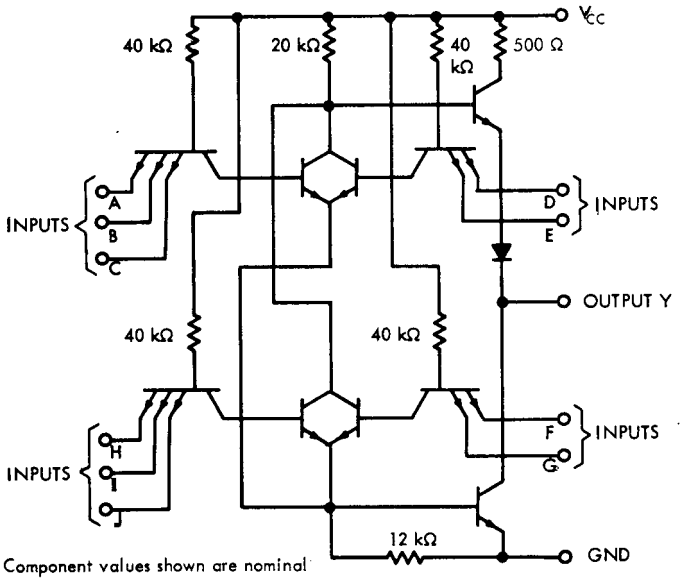
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, see figure 1

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_l = 50 pF		35	60	ns
t_{pd1}	Propagation delay time to logical 1 level	C_l = 50 pF		50	90	ns

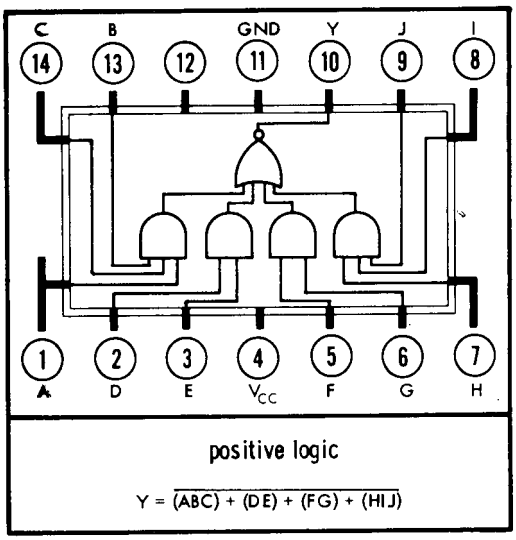
† For conditions shown as MIN or MAX, use the MIN or MAX value specified under recommended operating conditions for the applicable device type.

4-WIDE 3-2-2-3 INPUT AND-OR-INVERT GATE

schematic



Component values shown are nominal



recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L54R	4.5	5	5.5	V
SN74L54R	4.75	5	5.25	V
Fan-Out From Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L54R	-55	25	125	°C
SN74L54R	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of either AND section to ensure logical 0 at output	V_{CC} = MIN,	$V_{out(0)} \leq 0.3$ V	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	V_{CC} = MIN,	$V_{out(1)} \geq 2.4$ V			0.7	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -100 μA	V_{in} = 0.7 V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 2 mA	V_{in} = 2 V,			0.3	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0.3 V			-0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4 V			10	μA
		V_{CC} = MAX,	V_{in} = 5.5 V			100	μA
I_{OS}	Short-circuit output current	V_{CC} = MAX		-3		-15	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = 5 V,	V_{in} = 5 V		0.6	0.9	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = 5 V,	V_{in} = 0		0.39	0.72	mA

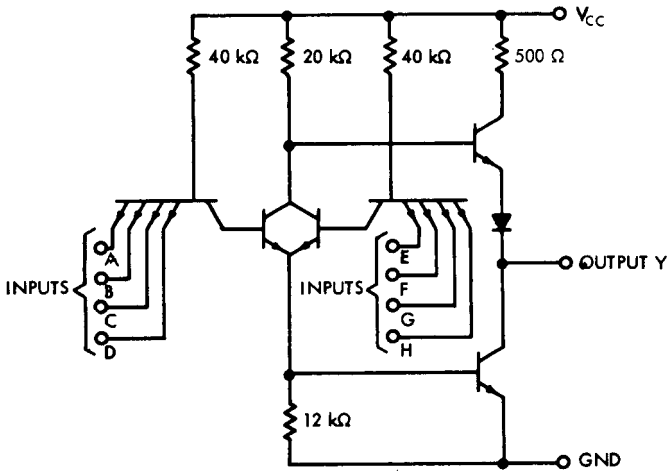
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, see figure 1

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_l = 50 pF		35	60	ns
t_{pd1}	Propagation delay time to logical 1 level	C_l = 50 pF		50	90	ns

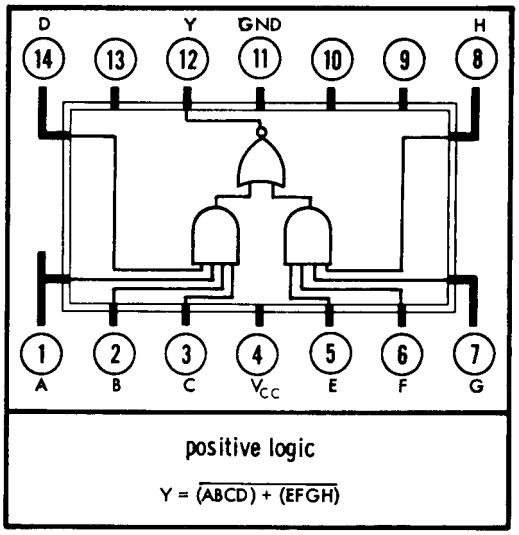
† For conditions shown as MIN or MAX, use the MIN or MAX value specified under recommended operating conditions for the applicable device type.

TYPES SN54L55R, SN74L55R
2-WIDE 4-INPUT AND-OR-INVERT GATE

schematic



Component values shown are nominal



recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L55R	4.5	5	5.5	V
SN74L55R	4.75	5	5.25	V
Fan-Out From Output, N			10	
Operating Free-Air Temperature Range, T_A: SN54L55R	-55	25	125	°C
SN74L55R	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals of either AND section to ensure logical 0 at output	V_{CC} = MIN,	$V_{out(0)} \leq 0.3$ V	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	V_{CC} = MIN,	$V_{out(1)} \geq 2.4$ V			0.7	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -100 μA	V_{in} = 0.7 V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 2 mA	V_{in} = 2 V,			0.3	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX,	V_{in} = 0			-0.18	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX,	V_{in} = 2.4 V			10	μA
		V_{CC} = MAX,	V_{in} = 5.5 V			100	μA
I_{OS}	Short-circuit output current	V_{CC} = MAX		-3		-15	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = 5 V,	V_{in} = 5 V		0.38	0.59	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = 5 V,	V_{in} = 0		0.22	0.36	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, see figure 1

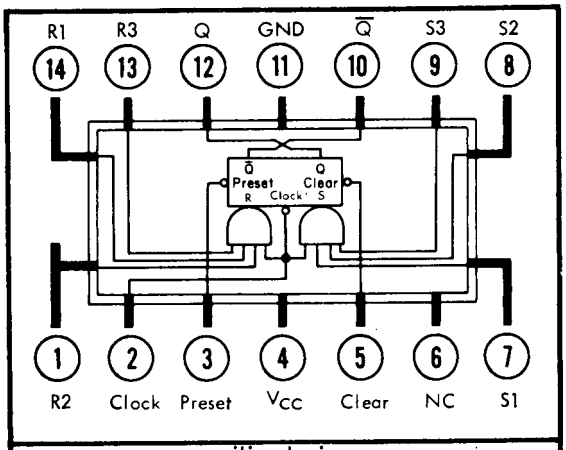
PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	C_L = 50 pF		35	60	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L = 50 pF		50	90	ns

† For conditions shown as MIN or MAX, use the MIN or MAX value specified under recommended operating conditions for the applicable device type.

logic

TRUTH TABLE		
t_n		t_{n+1}
R	S	Q
0	0	Q_n
0	1	1
1	0	0
1	1	Indeterminate

NOTES: 1. R = R1 ● R2 ● R3
2. S = S1 ● S2 ● S3
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.

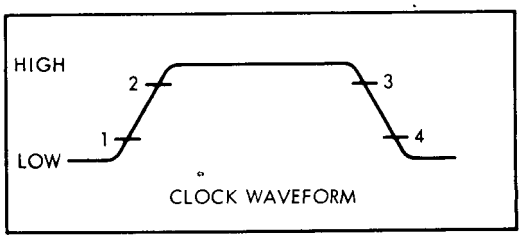


positive logic
Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock

description

This R-S flip-flop is based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L71R	4.5	5	5.5	V
SN74L71R	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54L71R	-55	25	125	°C
SN74L71R	0	25	70	°C
Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See figure 2)	200			ns
Width of Preset Pulse, $t_{p(preset)}$ (See figure 2)	100			ns
Width of Clear Pulse, $t_{p(clear)}$ (See figure 2)	100			ns
Input Setup Time, t_{setup} (See figure 2)	100			ns
Input Hold Time, t_{hold} (See figure 2)	≥0			

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

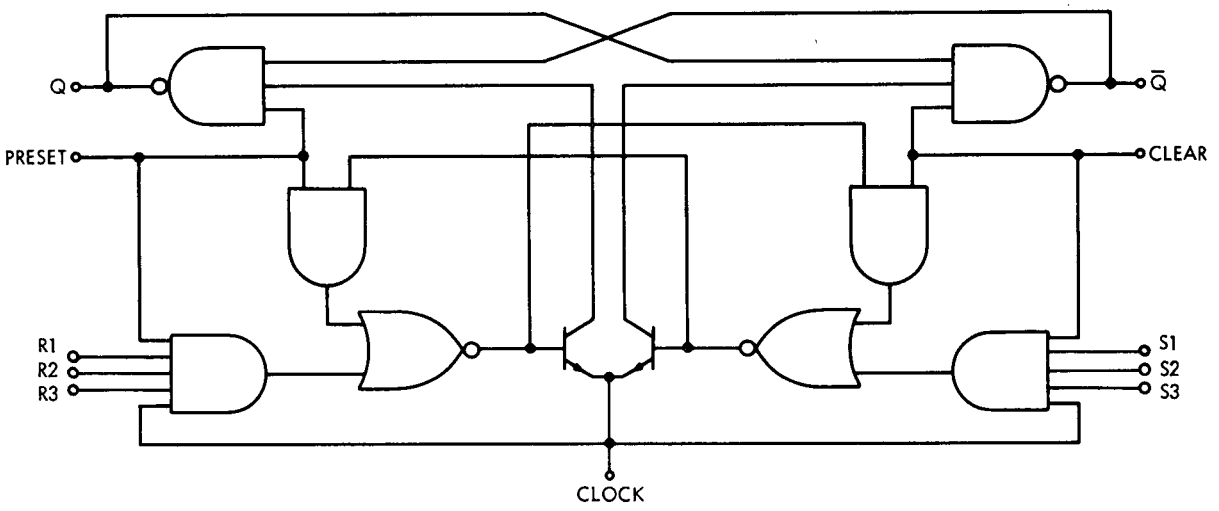
PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal except clock	V_{CC} = MIN			0.7	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at clock input terminal	V_{CC} = MIN			0.6	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -100 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 2 mA			0.3	V
$I_{in(0)}$	Logical 0 level input current at R1, R2, R3, S1, S2, or S3	V_{CC} = MAX, V_{in} = 0.3 V			-0.18	mA
$I_{in(0)}$	Logical 0 level input current at preset, clear, or clock	V_{CC} = MAX, V_{in} = 0.3 V			-0.36‡	mA
$I_{in(1)}$	Logical 1 level input current at R1, R2, R3, S1, S2, or S3	V_{CC} = MAX, V_{in} = 2.4 V			10	μA
		V_{CC} = MAX, V_{in} = 5.5 V			100	μA
$I_{in(1)}$	Logical 1 level input current at preset or clear	V_{CC} = MAX, V_{in} = 2.4 V			20	μA
		V_{CC} = MAX, V_{in} = 5.5 V			200	μA
$I_{in(1)}$	Logical 1 level current into the clock input	V_{CC} = MAX, V_{in} = 2.4 V			0‡	μA
		V_{CC} = MAX, V_{in} = 5.5 V			200‡	μA
I_{OS}	Short-circuit output current	V_{CC} = MAX,	-3		-15	mA
I_{CC}	Supply Current	V_{CC} = 5 V, $V_{in(clock)}$ = 0		0.76	1.3	mA

† For conditions shown as MIN or MAX, use the MIN or MAX value specified under recommended operating conditions for the applicable device type.
‡ For typical clock input current see page 23.

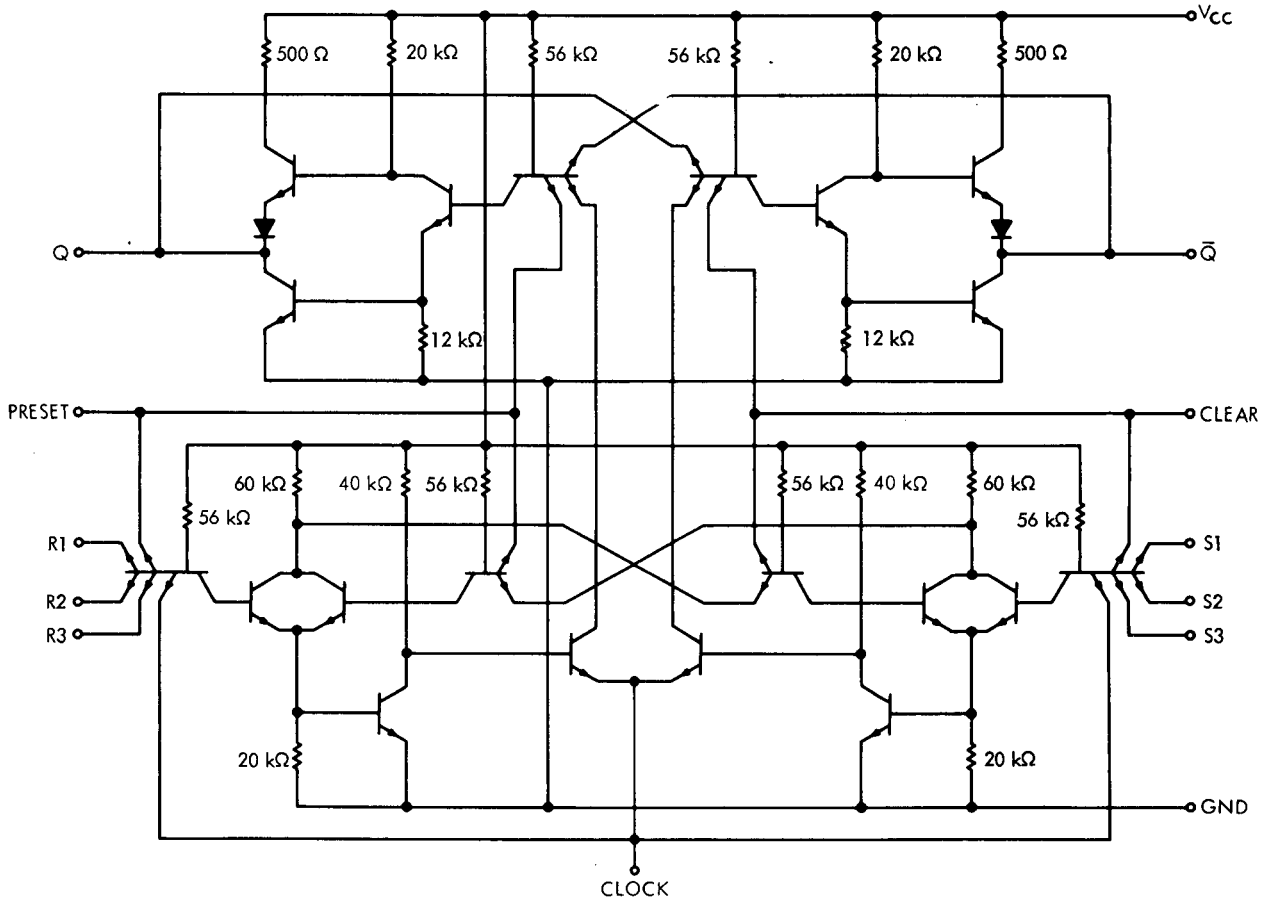
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10 (see figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_l = 50 pF		3		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	C_l = 50 pF		35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	C_l = 50 pF		60	150	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_l = 50 pF	10	35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_l = 50 pF	10	60	150	ns

functional block diagram



schematic



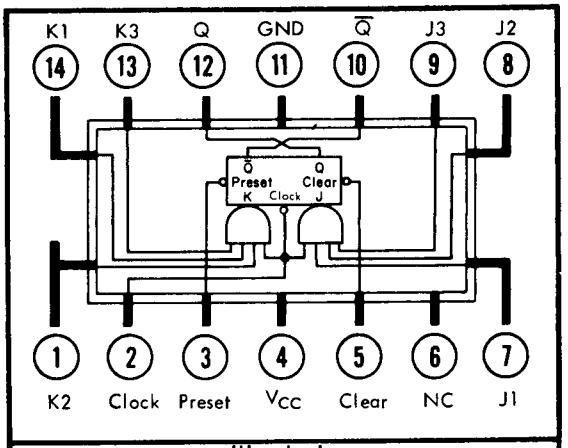
Component values shown are nominal.

TYPES SN54L72R, SN74L72R
J-K MASTER-SLAVE FLIP-FLOP

logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. $J = J1 \bullet J2 \bullet J3$
2. $K = K1 \bullet K2 \bullet K3$
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.



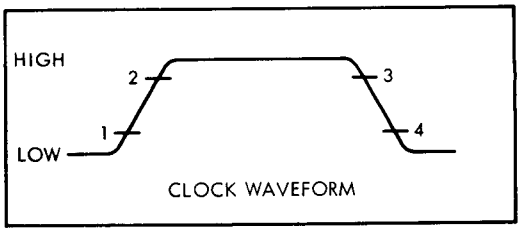
positive logic
Low input to preset sets Q to logical 1
Low input to clear sets Qto logical 0
Preset and clear are independent of clock

description

This J-K flip-flop is based on the master-slave principle. The AND gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L72R	4.5	5	5.5	V
SN74L72R	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54L72R	-55	25	125	°C
SN74L72R	0	25	70	°C
Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See figure 2)	200			ns
Width of Preset Pulse, $t_{p(preset)}$ (See figure 2)	100			ns
Width of Clear Pulse, $t_{p(clear)}$ (See figure 2)	100			ns
Input Setup Time, t_{setup} (See figure 2)	$\geq t_{p(clock)}$			
Input Hold Time, t_{hold} (See figure 2)	≥0			

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal except clock	V_{CC} = MIN			0.7	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at clock input terminal	V_{CC} = MIN			0.6	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −100 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 2 mA			0.3	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, or K3	V_{CC} = MAX, V_{in} = 0.3 V			−0.18	mA
$I_{in(0)}$	Logical 0 level input current at preset, clear, or clock	V_{CC} = MAX, V_{in} = 0.3 V			−0.36‡	mA
$I_{in(1)}$	Logical level input current at J1, J2, J3, K1, K2, or K3	V_{CC} = MAX, V_{in} = 2.4 V			10	μA
		V_{CC} = MAX, V_{in} = 5.5 V			100	μA
$I_{in(1)}$	Logical 1 level input current at preset or clear	V_{CC} = MAX, V_{in} = 2.4 V			20	μA
		V_{CC} = MAX, V_{in} = 5.5 V			200	μA
$I_{in(1)}$	Logical 1 level current into the clock input	V_{CC} = MAX, V_{in} = 2.4 V			0‡	μA
		VCC = MAX, V_{in} = 5.5 V			200‡	μA
I_{OS}	Short-circuit output current	V_{CC} = MAX	−3		−15	mA
I_{CC}	Supply current	V_{CC} = 5 V, $V_{in(clock)}$ = 0		0.76	1.3	mA

† For conditions shown as MIN or MAX, use the MIN or MAX value specified under recommended operating conditions for the applicable device type.

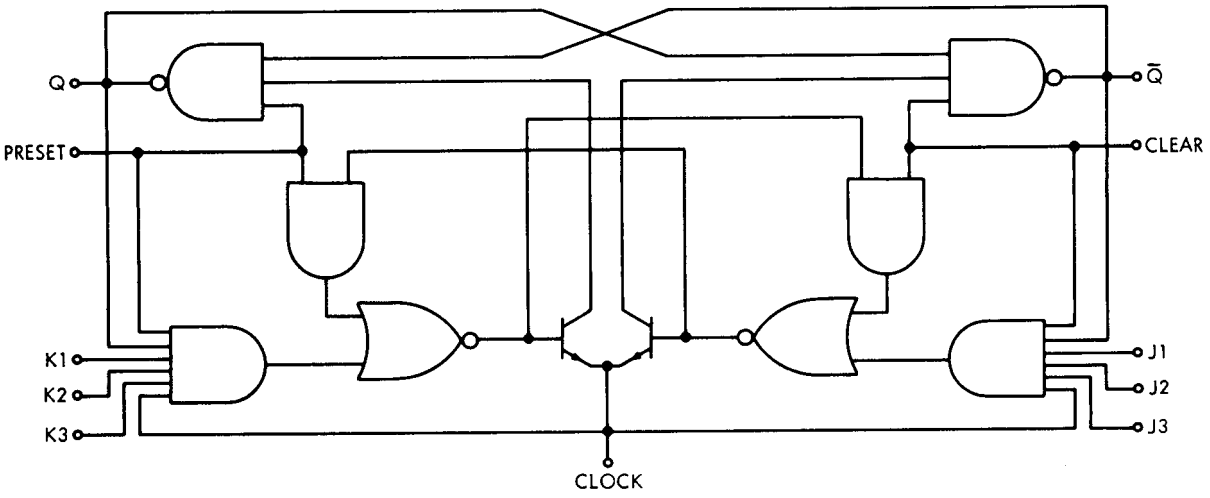
‡ For typical clock input current see page 23.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10 (See figure 2)

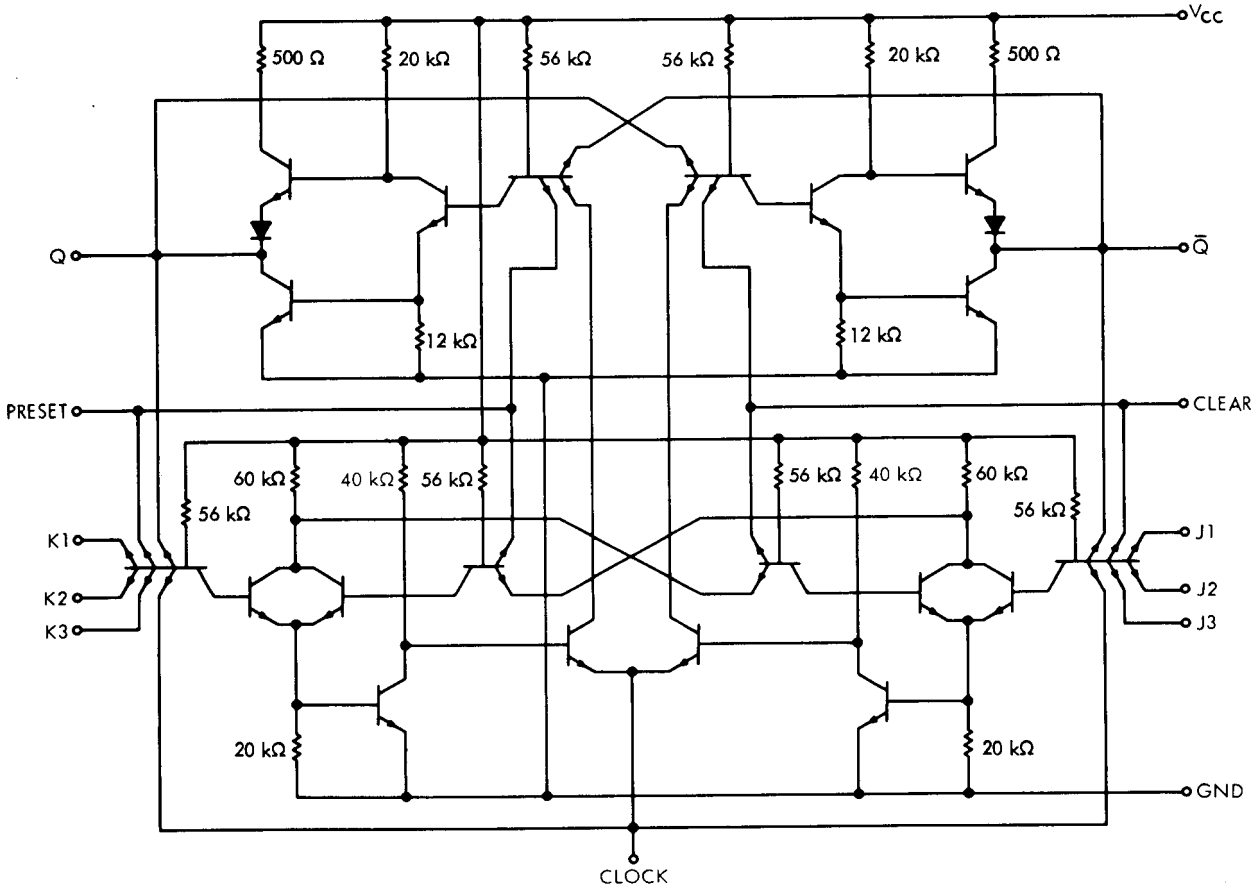
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	Unit
f_{clock}	Maximum clock frequency	C_l = 50 pF		3		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	C_l = 50 pF		35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	C_l = 50 pF		60	150	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_l = 50 pF	10	35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_l = 50 pF	10	60	150	ns

TYPES SN54L72R, SN54L72R
J-K MASTER-SLAVE FLIP-FLOP

functional block diagram



schematic



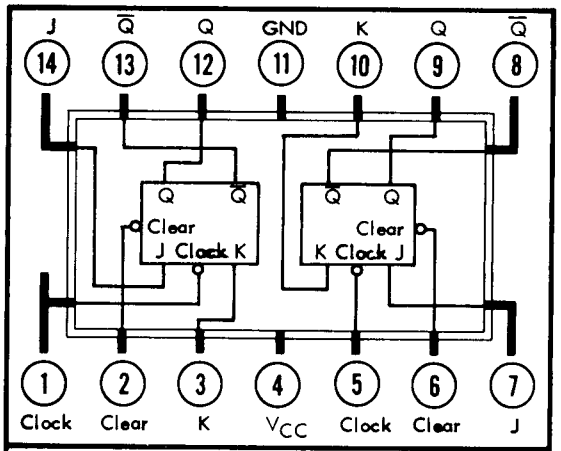
Component values shown are nominal.

TYPES SN54L73R, SN74L73R
DUAL J-K MASTER-SLAVE FLIP-FLOP

logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.



positive logic

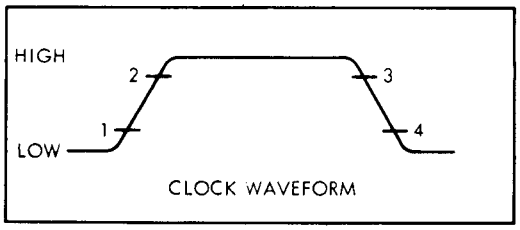
Low input to clear sets Q to logical 0
Clear is independent of clock

description

This J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state.



CLOCK WAVEFORM

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN54L73R	4.5	5	5.5	V
SN74L73R	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN54L73R	-55	25	125	°C
SN74L73R	0	25	70	°C
Fan-Out From Each Output, N			10	
Width of Clock Pulse, $t_{p(clock)}$ (See figure 2)	200			ns
Width of Preset Pulse, $t_{p(preset)}$ (See figure 2)	100			ns
Width of Clear Pulse, $t_{p(clear)}$ (See figure 2)	100			ns
Input Setup Time, t_{setup} (See figure 2)	$\geq t_{p(clock)}$			
Input Hold Time, t_{hold} (See figure 2)	≥0			

DUAL J-K MASTER-SLAVE FLIP-FLOP

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal except clock	V_{CC} = MIN			0.7	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at clock input terminal	V_{CC} = MIN			0.6	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −100 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 2 mA			0.3	V
$I_{in(0)}$	Logical 0 level input current at J or K	V_{CC} = MAX, V_{in} = 0.3 V			−0.18	mA
$I_{in(0)}$	Logical 0 level input current at clear, or clock	V_{CC} = MAX, V_{in} = 0.3 V			−0.36‡	mA
$I_{in(1)}$	Logical 1 level input current at J or K	V_{CC} = MAX, V_{in} = 2.4 V			10	μA
		V_{CC} = MAX, V_{in} = 5.5 V			100	μA
$I_{in(1)}$	Logical 1 level input current at clear	V_{CC} = MAX, V_{in} = 2.4 V			20	μA
		V_{CC} = MAX, V_{in} = 5.5 V			200	μA
$I_{in(1)}$	Logical 1 level current into the clock input	V_{CC} = MAX, V_{in} = 2.4 V			0‡	μA
		V_{CC} = MAX, V_{in} = 5.5 V			200‡	μA
I_{OS}	Short-circuit output current	V_{CC} = MAX	−3		−15	mA
I_{CC}	Supply current (each flip-flop)	V_{CC} = 5 V, $V_{in(clock)}$ = 0		0.76	1.3	mA

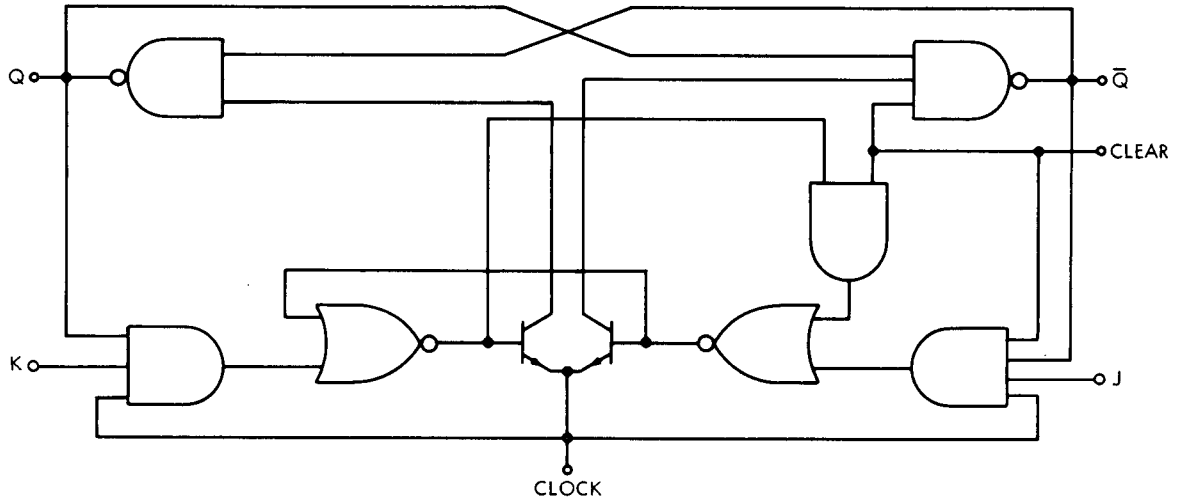
† For conditions shown as MIN or MAX, use the MIN or MAX value specified under recommended operating conditions for the applicable device type.

‡ For typical clock input current see page 23.

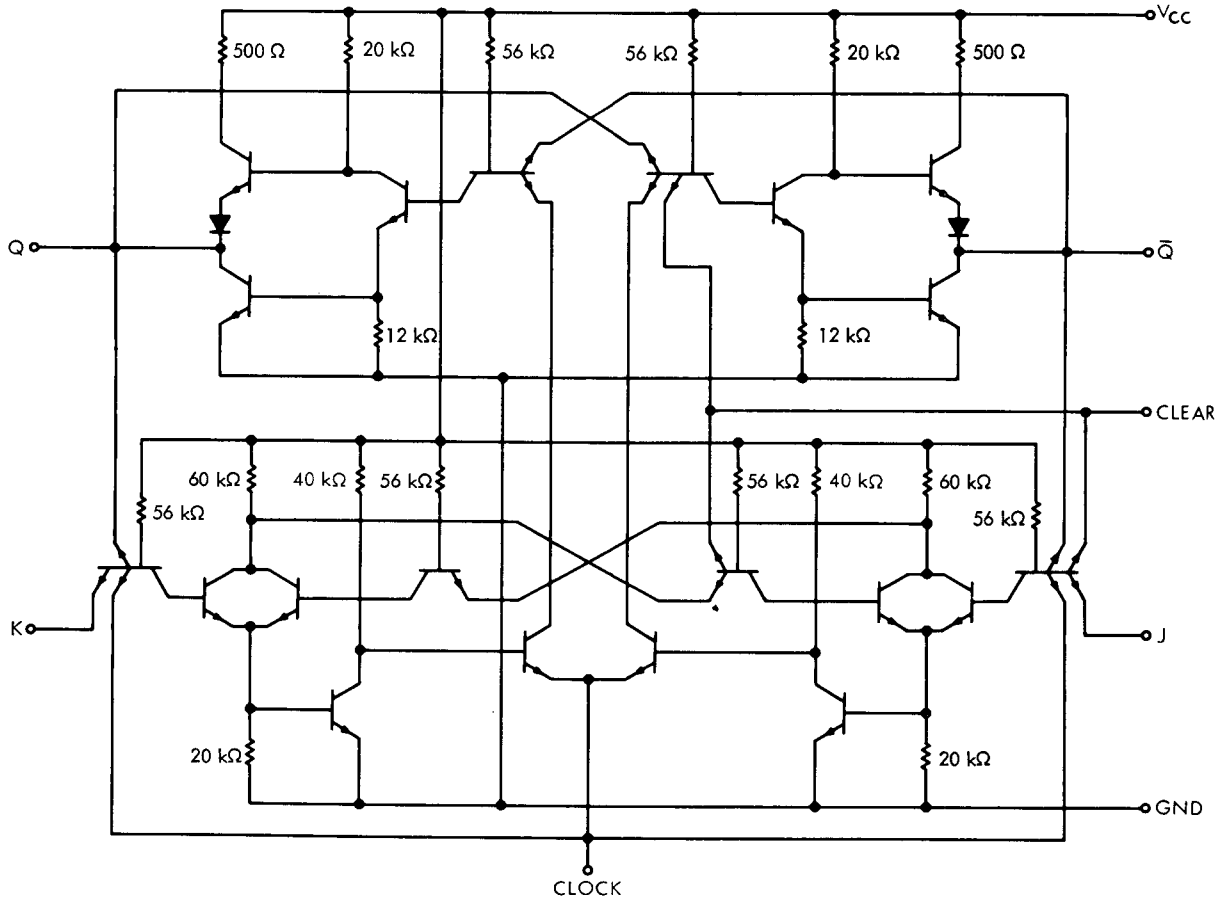
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10 (see figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	Unit
f_{clock}	Maximum clock frequency	C_1 = 50 pF		3		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	C_1 = 50 pF		35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	C_1 = 50 pF		60	150	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_1 = 50 pF	10	35	75	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_1 = 50 pF	10	60	150	ns

functional block diagram (each flip-flop)

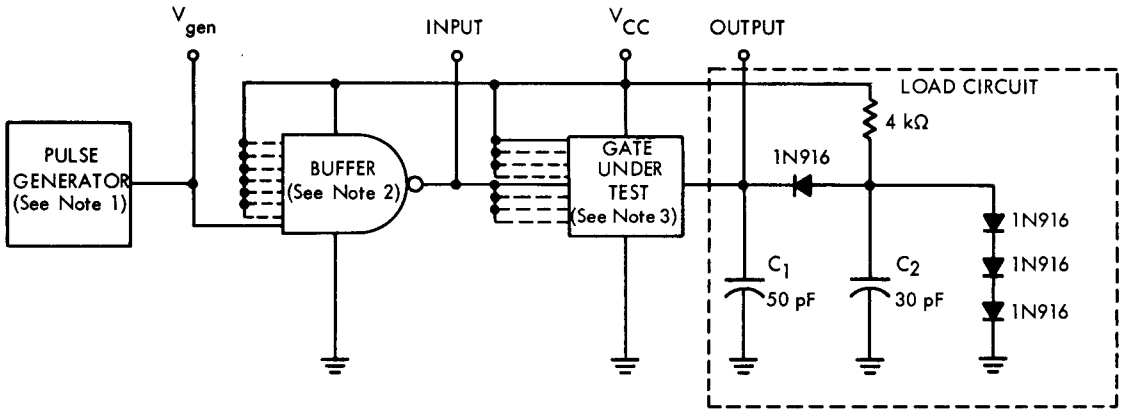


schematic (each flip-flop)

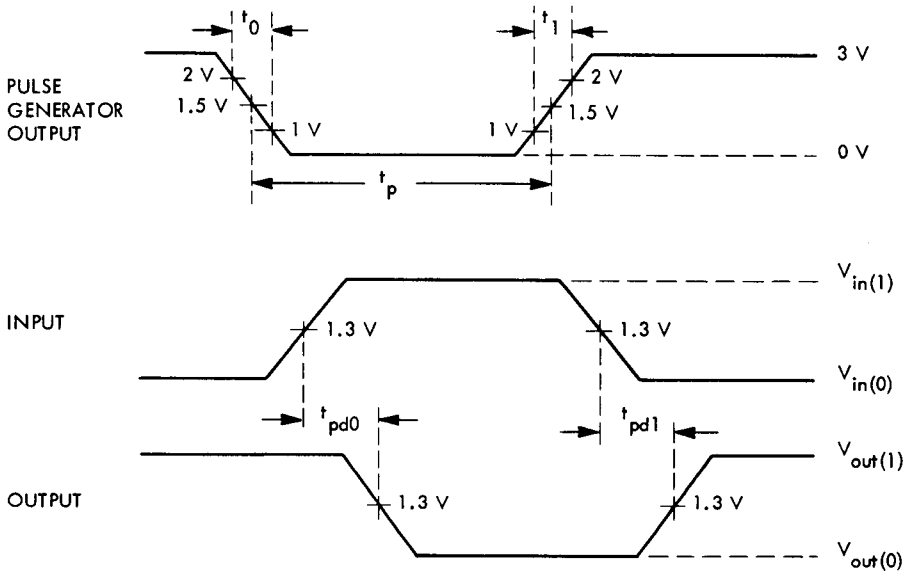


Component values shown are nominal.

switching characteristics



TEST CIRCUIT

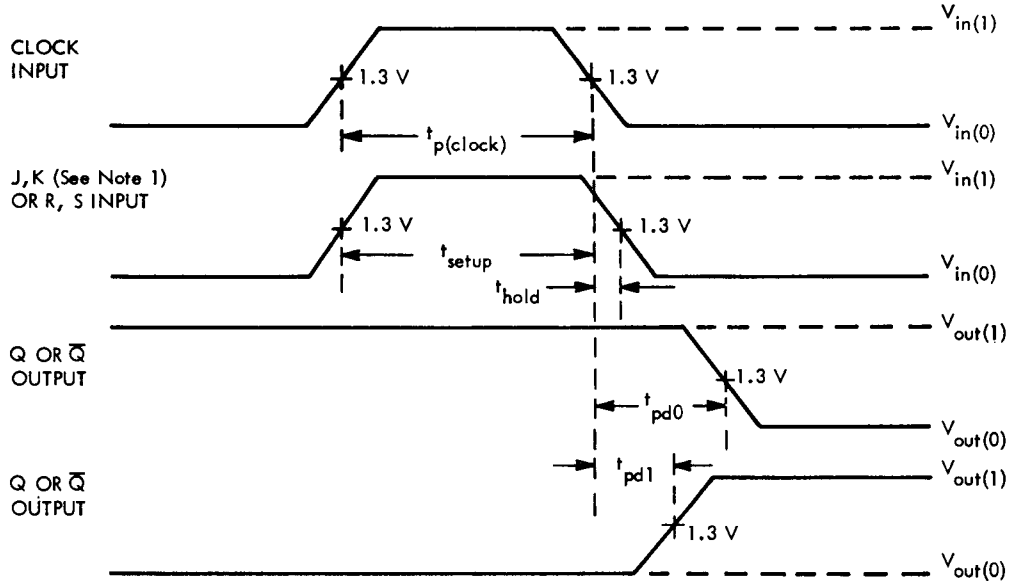


VOLTAGE WAVEFORMS

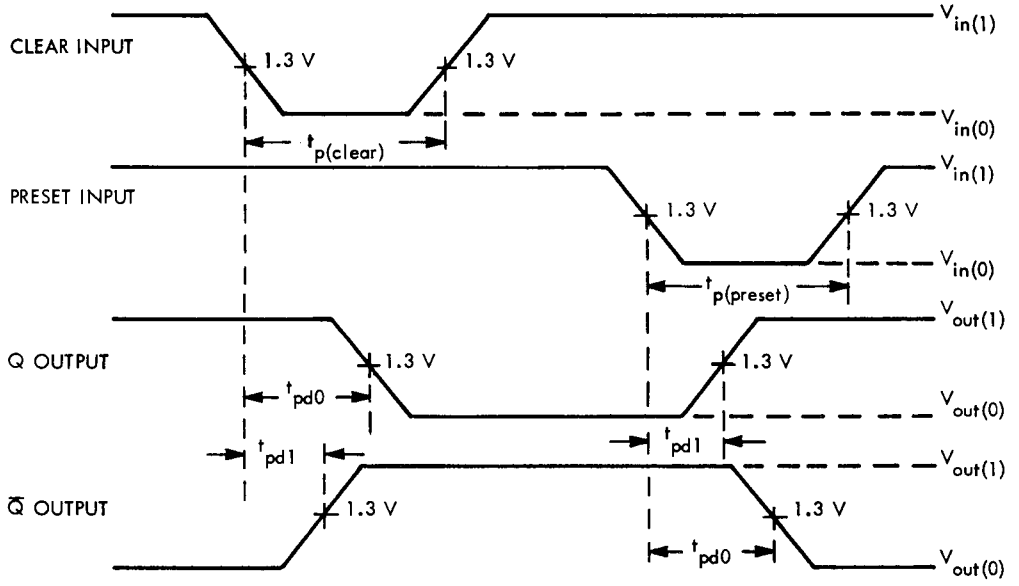
NOTES:
1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_1 = t_0$ = 15 ns, f = 500 kHz, duty cycle = 50%, $Z_{out} \approx 50\ \Omega$.
2. The buffer gate is a series 54L/74L gate.
3. When testing SN54L00R/SN74L00R, SN54L10R/SN74L10R, SN54L20R/SN74L20R, and SN54L30R/SN74L30R the input signal is applied to one input and all unused inputs are at V_{CC}. When testing SN54L51R/SN74L51R, SN54L54R/SN74L54R and SN54L55R/SN74L55R the input signal is applied to one input of each AND section and all other inputs are at V_{CC}.
4. C_1 includes probe and jig capacitance.

FIGURE 1 — GATE PROPAGATION DELAY TIMES

FLIP-FLOP WAVEFORM DEFINITIONS



CLOCK AND INPUT/OUTPUT VOLTAGE WAVEFORMS



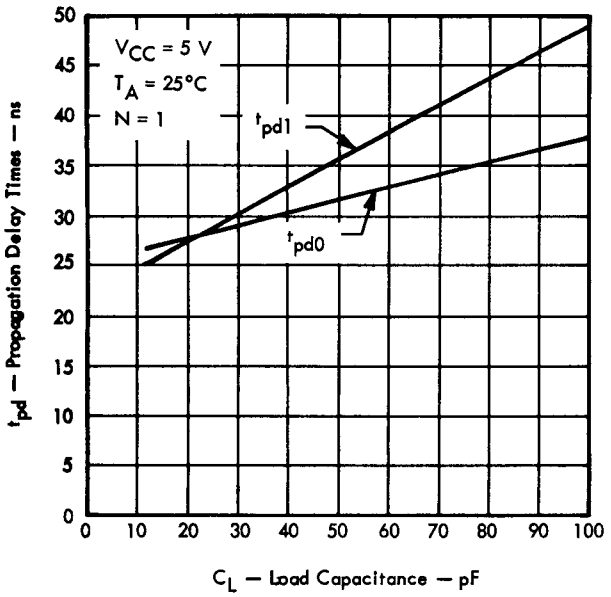
PRESET AND CLEAR INPUT/OUTPUT VOLTAGE WAVEFORMS

NOTES: 1. Logical state of J and K inputs must not be allowed to change during $t_{p(clock)}$.
2. Load circuit is same as shown on figure 1.

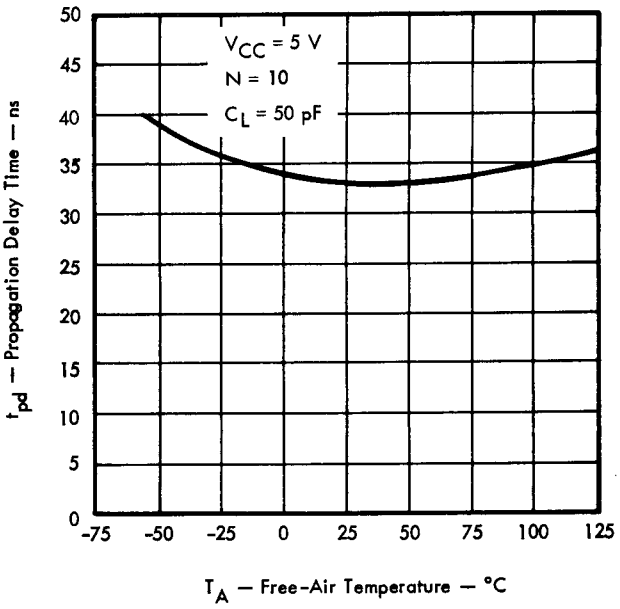
FIGURE 2 — FLIP-FLOP VOLTAGE WAVEFORM DEFINITIONS

TYPICAL CHARACTERISTICS (GATE PROPAGATION DELAY TIMES)

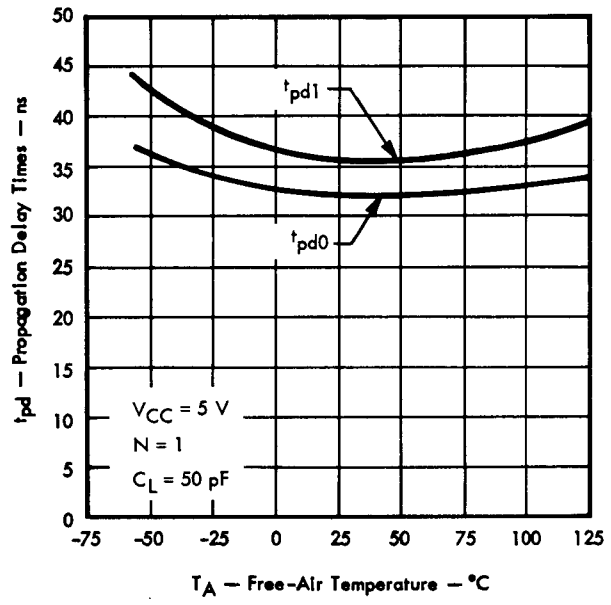
PROPAGATION DELAY TIMES
vs
LOAD CAPACITANCE



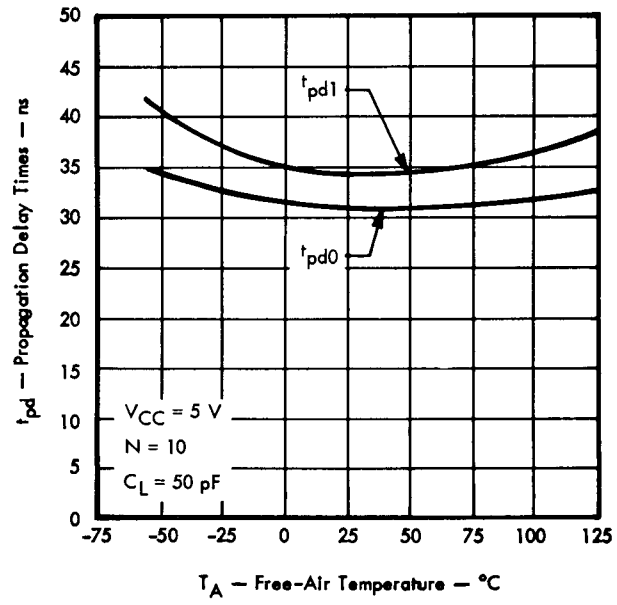
PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE



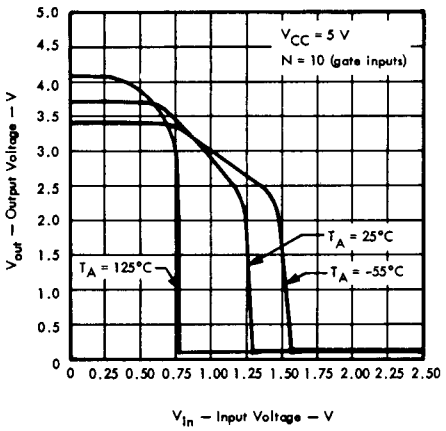
PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE



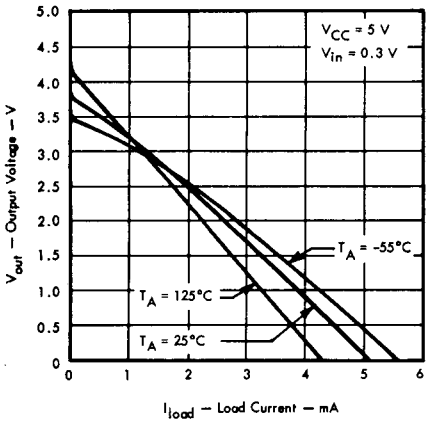
TYPICAL CHARACTERISTICS

OUTPUTS

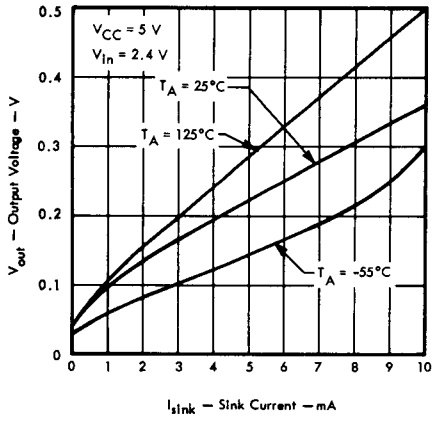
OUTPUT VOLTAGE
vs
INPUT VOLTAGE



OUTPUT VOLTAGE
vs
LOAD CURRENT

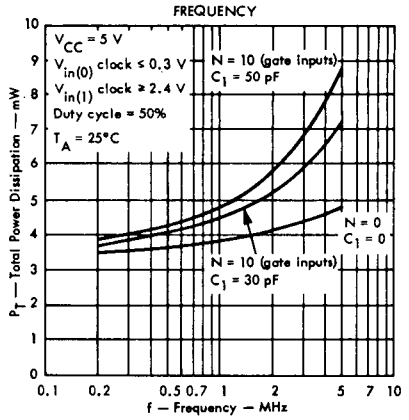


OUTPUT VOLTAGE
vs
SINK CURRENT

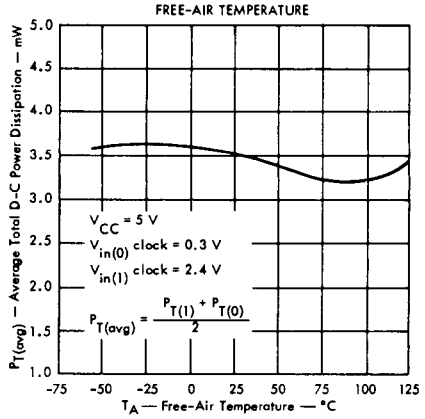


FLIP-FLOPS

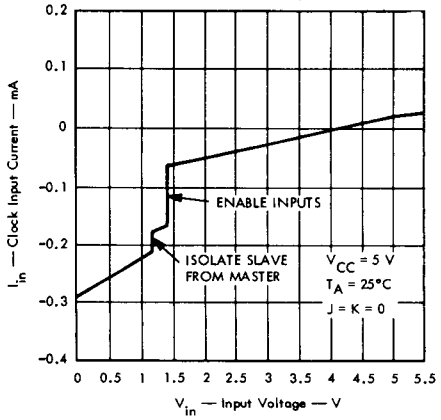
TOTAL POWER DISSIPATION
vs
FREQUENCY



AVERAGE TOTAL D-C POWER DISSIPATION
vs
FREE-AIR TEMPERATURE



CLOCK INPUT CURRENT
vs
INPUT VOLTAGE

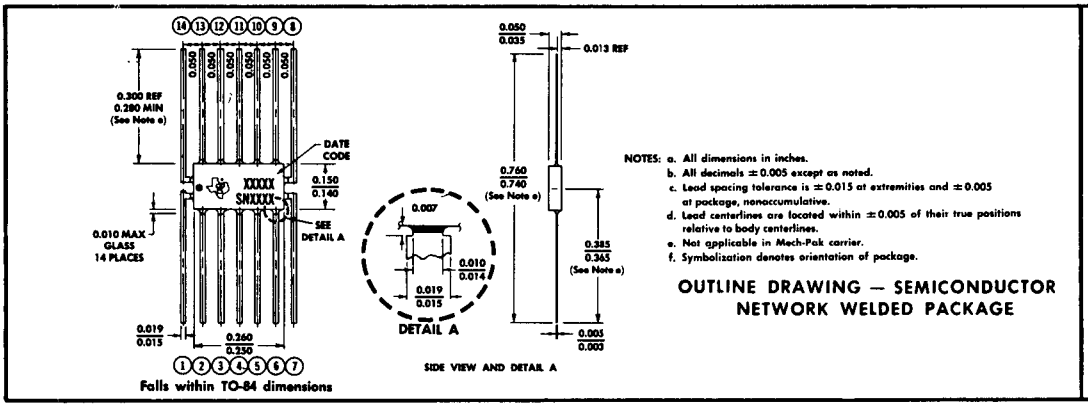


SERIES 54L/74L
SOLID CIRCUIT® SEMICONDUCTOR NETWORKS†

MECHANICAL DATA

general

Series 54L/74L semiconductor networks are mounted in a glass-to-metal hermetically sealed, welded package. Package body and leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated from leads and circuit. All Series 54L/74L networks are available with formed leads, insulator attached, and/or mounted in a Mech-Pak carrier.



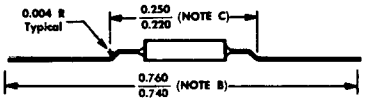
NOTES: a. All dimensions in inches.
b. All decimals ± 0.005 except as noted.
c. Lead spacing tolerance is ± 0.015 at extremities and ± 0.005 at package, nonaccumulative.
d. Lead centerlines are located within ± 0.005 of their true positions relative to body centerlines.
e. Not applicable in Mech-Pak carrier.
f. Symbolization denotes orientation of package.

OUTLINE DRAWING — SEMICONDUCTOR NETWORK WELDED PACKAGE

leads

Gold-plated F-15† leads require no additional cleaning or processing when used in soldered or welded assembly. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Networks are removed from Mech-Pak carriers with lead lengths of 0.300 inch (0.750 inch tip-to-tip).

FORMED LEADS

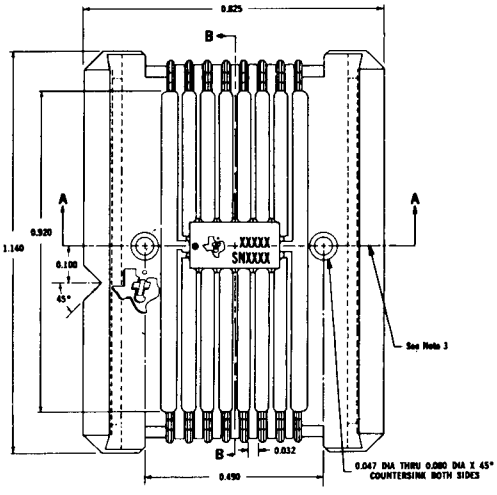


NOTES: A. All dimensions in inches
B. Not applicable in Mech-Pak Carrier
C. Measured from centerline of outside bends

insulator

An insulator, secured to the back surface of the package, permits mounting networks on circuit boards which have conductors passing beneath the package. The insulator is 0.0025 inches thick and has an insulation resistance of 10 megohms at 25°C.

MECH-PAK DIMENSIONS



NOTES: 1. All dimensions are nominal in inches unless otherwise specified.
2. Overall thickness is 0.175 and nestled height is 0.150 each.
3. In the plane shown, package centerline is located within ±0.015 of the tooling holes centerline.

mech-pak carrier

The Mech-Pak carrier facilitates handling the network, and is compatible with automatic equipment used for testing and assembly. The carrier is particularly appropriate for mechanized assembly operations and will withstand temperatures of 125°C for indefinite periods.

ordering instructions

Variations in mechanical configuration of semiconductor networks are identified by suffix numbers shown in a table at the right.

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.300 inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	-6	-7	-1	-2	-3	-4	-5

†Patented by Texas Instruments Incorporated.

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SOLID CIRCUIT® SEMICONDUCTOR NETWORKS†

SERIES 15 830N
BULLETIN NO. DL-S 668942, NOVEMBER, 1966

DIODE-TRANSISTOR-LOGIC SEMICONDUCTOR NETWORKS IN MOLDED PLUG-IN PACKAGES

description

Series 15 830N consists of the Series 15 830 general-purpose DTL circuits mounted within a 14-pin plastic package and characterized for operation over the temperature range of 0°C to 75°C.

features

LOW SYSTEM COST
- multifunction gates offering low cost per logic function
- electrically designed specifically for monolithic integrated-circuit technology
- plug-in configuration ideal for flow-soldering techniques
- pins on 100-mil grid spacings for industrial-type circuit-boards

PERFORMANCE
- high speed
- high d-c noise margins
- low power dissipation
- good fan-out capability

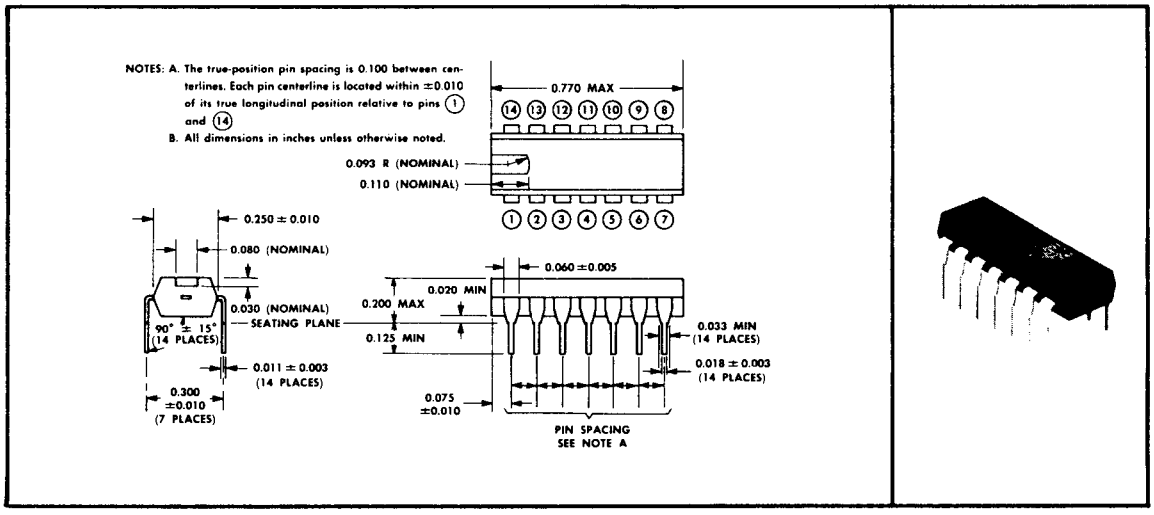
EASE OF DESIGN
- familiar logic configuration (DTL)
- single-ended output — dot-OR logic
- complete family for design flexibility
- single power supply

specifications, logic symbols and terminal designations

Schematic diagrams, fan-out rules, maximum ratings, and electrical characteristics for Series 15 830N networks are identical to those of the corresponding Series 15 830 type numbers except for maximum propagation delay times‡. Terminal designations for the Series 15 830N networks are shown in this data sheet.

mechanical data

Series 15 830N networks are mounted on a 14-lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperatures with no deformation, and circuit performance characteristics remain stable when operated in high-humidity conditions.



†Patented by Texas Instruments

‡Maximum t_{pd1} and t_{pd0} for Series 15 830N are 5 ns higher than for Series 15 830. The increase in the typical or median value is negligible.

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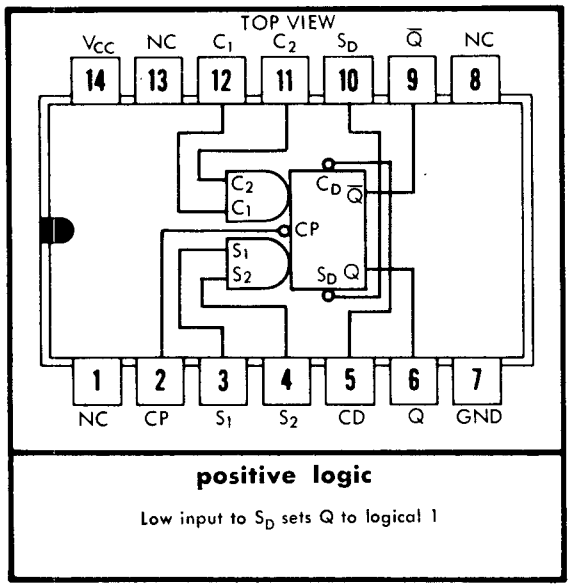
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SN15 831N, SN15 845N, SN15 848N
MASTER-SLAVE FLIP-FLOPS



positive logic

Low input to S_D sets Q to logical 1

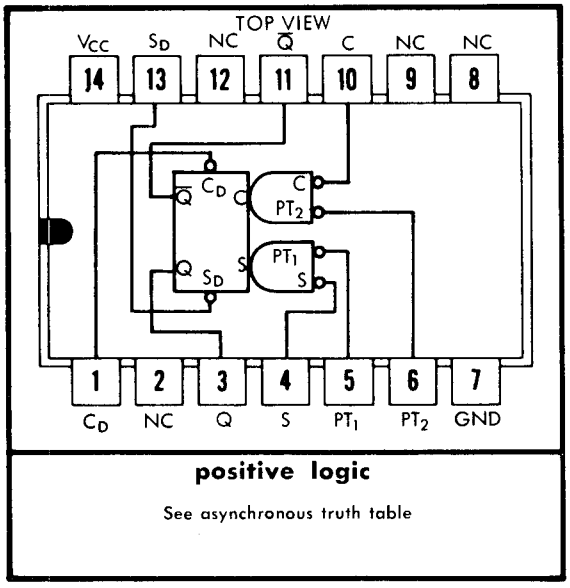
TRUTH TABLES

R-S MODE				
t_n				t_{n+1}
S_1	S_2	C_1	C_2	Q
0	X	0	X	Qn
0	X	X	0	Qn
X	0	0	X	Qn
X	0	X	0	Qn
0	X	1	1	0
X	0	1	1	0
1	1	0	X	1
1	1	X	0	1
1	1	1	1	Indeterminate

J-K MODE		
t_n		t_{n+1}
S_1	C_1	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\bar{Q}n$

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.
3. X indicates that either a logical 1 or a logical 0 may be present.
4. Logical 1 is more positive than logical 0
5. For operation in the J-K mode connect S_2 to $\bar{Q}$, and C_2 to Q.

SN15 850N
PULSE-TRIGGERED BINARY



positive logic

See asynchronous truth table

TRUTH TABLES

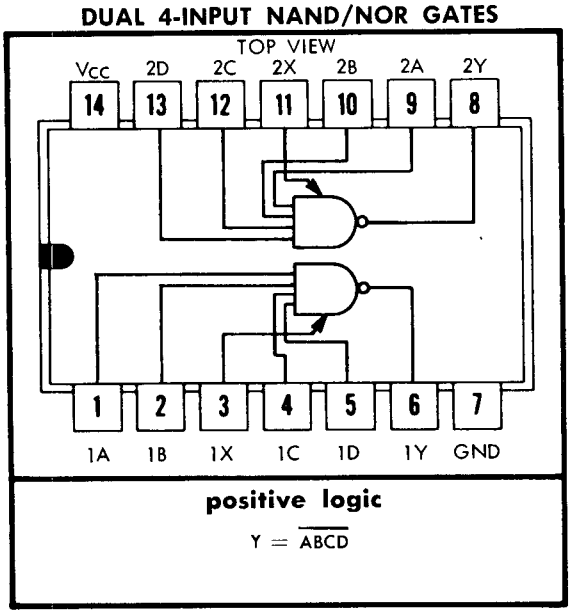
SYNCHRONOUS					
t_n PULSE INPUT				t_{n+1} OUTPUT	
S	C	PT_1	PT_2	Q	$\bar{Q}$
1	X	X	1	Qn	$\bar{Q}n$
X	1	1	X	Qn	$\bar{Q}n$
0	1	0	X	1	0
0	X	0	1	1	0
1	0	X	0	0	1
X	0	1	0	0	1
0	0	0	0	Indeterminate	

ASYNCHRONOUS			
DIRECT INPUT		OUTPUT	
S_D	C_D	Q	$\bar{Q}$
1	1	Qn	$\bar{Q}n$
0	1	0	1
1	0	1	0
0	0	1	1

NOTES:
1. X indicates that either a logical 1 or a logical 0 may be present.
2. Logical 1 is more positive than logical 0.
3. Logical states shown for pulse inputs PT_1 and PT_2 indicate that a transition to that state has just occurred.
4. Truth tables reflect individual conditions at the inputs. Either direct input may be used to inhibit its corresponding pulse input.

SOLID CIRCUIT® SEMICONDUCTOR NETWORKS

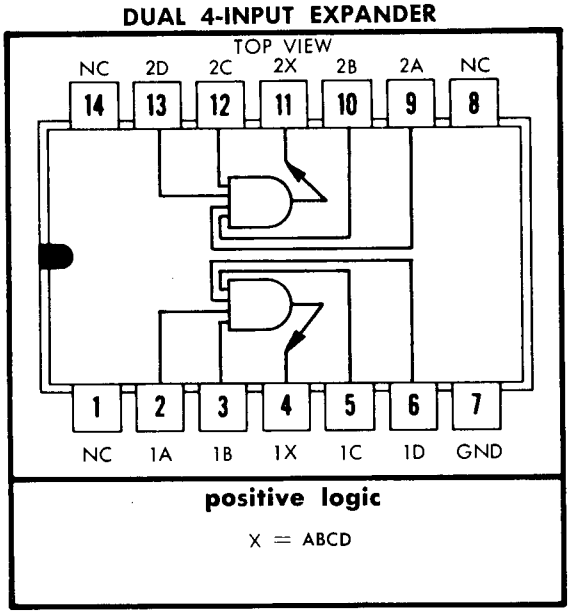
SN15 830N, SN15 832N (BUFFER), SN15 844N (POWER)
DUAL 4-INPUT NAND/NOR GATES



positive logic

$Y = \overline{ABCD}$

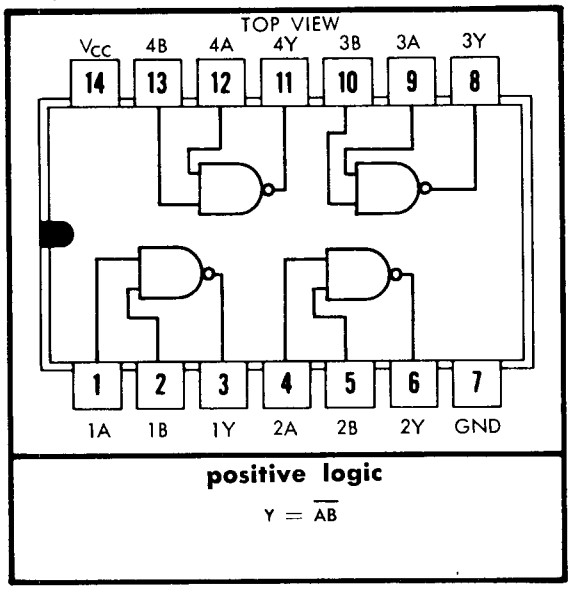
SN15 833N
DUAL 4-INPUT EXPANDER



positive logic

$X = ABCD$

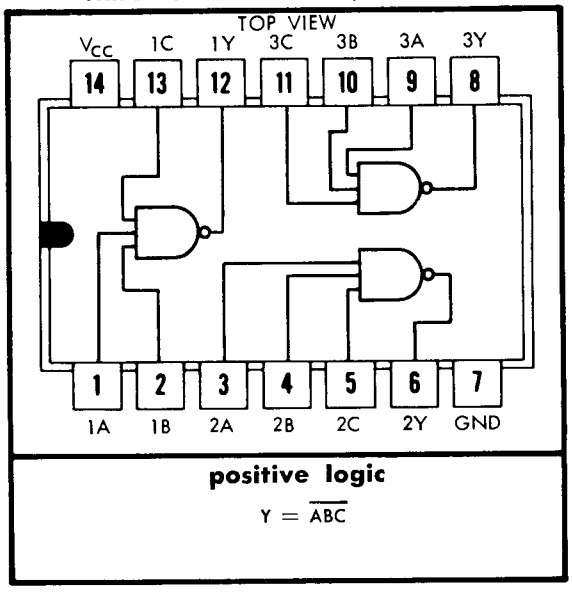
SN15 846N
QUADRUPLE 2-INPUT NAND/NOR GATE



positive logic

$Y = \overline{AB}$

SN15 862N
TRIPLE 3-INPUT NAND/NOR GATE

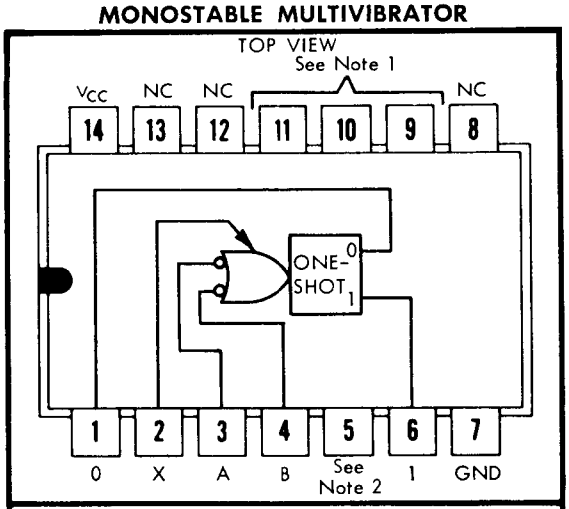


positive logic

$Y = \overline{ABC}$

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

SN15 851N
MONOSTABLE MULTIVIBRATOR



NOTES: 1. Refer to the schematic diagram for using pins (9), (10), and (11) to control one-shot pulse width.
2. Input sensitivity can be decreased by adding a capacitor from pin (5) to ground.

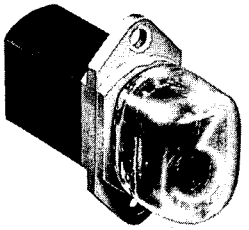
PRINTED IN U.S.A.

TEXAS INSTRUMENTS
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

BULLETIN NO. 1054B
December 15, 1966
(Supersedes Bulletin No. 1054C)

BCD TO DECIMAL READOUT DRIVER

TYPE
BIP-8211P
BIP-8507P



The BIP-8211P Decoder/Driver provides decimal readout on a standard rectangular NIXIE® Tube, type 8422 (B-5991) from 8 wire 8-4-2-1 binary-coded decimal inputs. Decoder circuitry which accepts logic level separations of 2.3V to 30V is completely solid state, and controls the selection of the NIXIE tube numeral elements. The BIP-8507P drives a plus/minus rectangular NIXIE tube, type B-5992. The modules feature a socket pack construction; i.e., socket and decoder are an integral unit. Height and width dimensions are those of the socket itself, permitting minimum center-to-center spacing of multi-digit displays. Refer to Bulletin 1066 for typical applications and theory of operation. Bezel assemblies for multi-tube displays are described in Bulletin 1020.

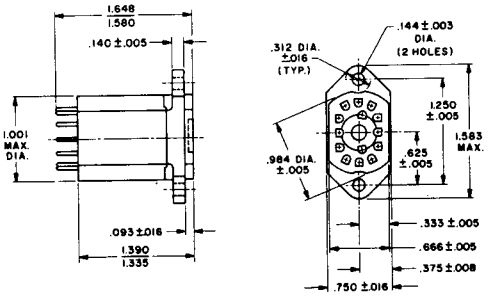


Figure 1. OUTLINE DRAWING

ELECTRICAL SPECIFICATIONS

INPUT REQUIREMENTS (Figure 2)

INPUT SIGNAL BIP-8211P..... 4 bit (8 lines) 8-4-2-1 BCD*
BIP-8507P..... 2 lines
Logic "1" = E_1 volts ..... Turn "ON"
Logic "0" = E_0 volts ±0.5V ... Turn "OFF"
BCD VOLTAGE LEVELS ..... BCD voltage levels may be any set of two levels within limitations specified under Logic Level Separations.

INPUT CURRENT (Each input line) BIP-8211P... 1.0 ma max.
BIP-8507P... 0.5 ma max.

POWER REQUIREMENTS (Note 3)

DC Supply Voltage Note 5..... +200 ± 10 Vdc
DC Supply Current BIP-8211P ..... 3.7 ma nom.
BIP-8507P ..... 1.5 ma nom.

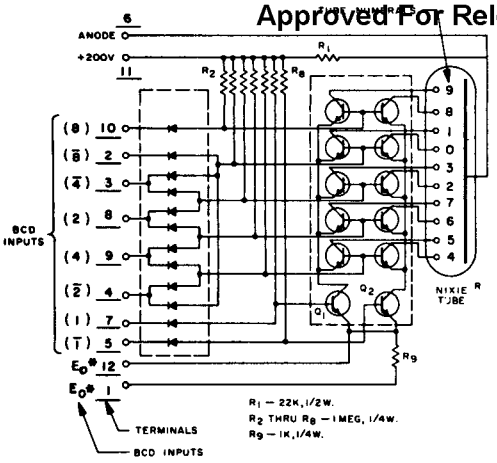
* Other modules which can accept other BCD codes such as 5-4-2-1, 2-4-2'-1, 4-2-2'-1, Watts, cyclic 20 Gray, etc., are also available. **(SEE BULLETIN 1108)**

BCD INPUT SIGNAL LEVEL REQUIREMENTS

Bias Terminals (Note 7)	Using Terminal 12 (Note 9)	Using Terminal 1 or 10 (Note 10)
Minimum Logic Level Separation	2.3V to 30V	5.2V to 26V
E_0 = Logic "0"	−5.0V to −0.9V	−1.0V to +0.5V
E_1 = Logic "1"	+1.4V to +25V	+5.7V to +25V

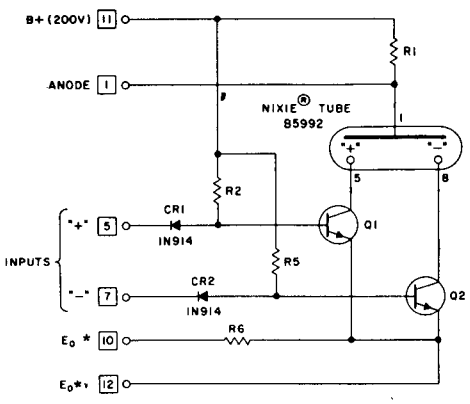
MECHANICAL CHARACTERISTICS

Connector ..... 12 pin rectangular socket base
Receptacle ..... SK-169 (Figure 4) (Note 4)
Mounting Diagram ..... Figure 5, Note 8
Weight ..... 1 oz. nom.
Basing Diagram ..... Figure 3
Outline drawing ..... Figure 1
Terminal Connections ..... Table 1
Temperature
Operating ..... −20°C to +85°C
Non-Operating ..... −50°C to +85°C



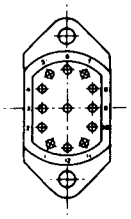
*See Notes 3, 7

Figure 2a. BIP-8211P SCHEMATIC



*See Notes 3, 7

Figure 2b. BIP-8507P SCHEMATIC



BOTTOM VIEW

NOTE:
A polarizing pin is added to the connector. This pin is not internally connected and mates with terminal 14 of receptacle SK-169.

Figure 3. BASING DIAGRAM

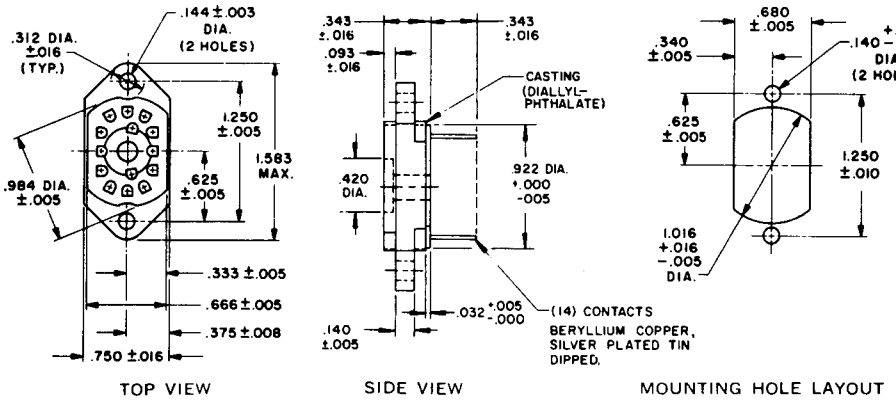


Figure 4. RECEPTACLE SK-169 (Note 4)

TERMINAL	BIP-8211P	BIP-8507P
1	E_o *	Note 1
2	BCD $\overline{8}$	–
3	BCD $\overline{4}$	–
4	BCD $\overline{2}$	–
5	BCD $\overline{1}$	"+" plus
6	Note 1	–
7	BCD 1	"–" minus
8	BCD 2	–
9	BCD 4	–
10	BCD 8	E_o*
11	+200 Vdc	+200 Vdc
12	*	*

* see Notes 3 and 7.

Table 1. TERMINAL CONNECTIONS

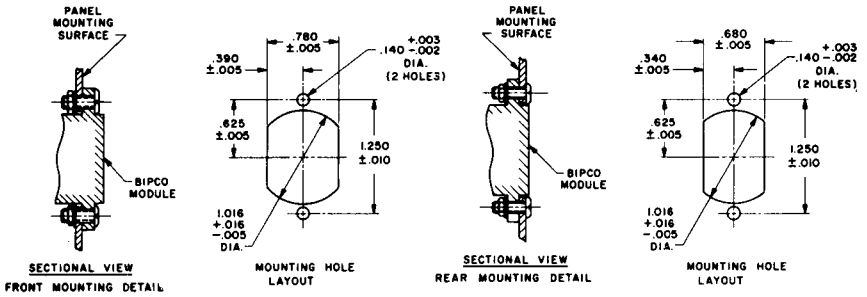


Figure 5. MOUNTING CONFIGURATIONS (Note 8)

NUMERAL	CODE 8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

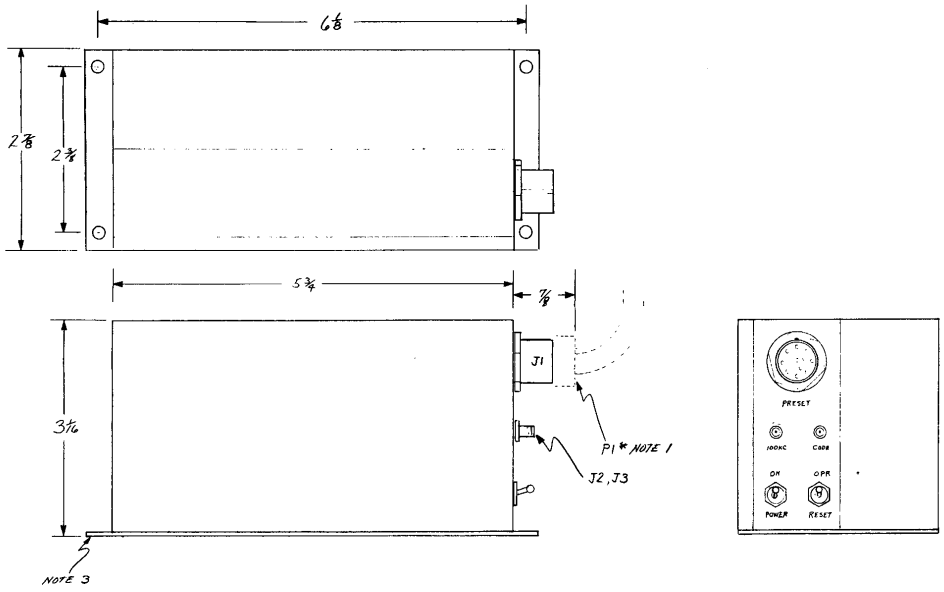
Table 2. BIP-8211P TRUTH TABLE

NOTES

1. Pin 6 on BIP-8211P and Pin 1 on BIP-8507P (NIXIE Tube Anode) are used for test purposes only.
2. NIXIE tube is not included as part of the module and must be ordered separately.
3. D.C. return for the +200V supply is normally connected to the one E_o input terminal being used.
4. Receptacle SK-169 is not part of the module and must be ordered separately.
5. For B+ voltages higher than +200 Vdc, a resistor (R) must be added in series with R_i (see Figures 2a and 2b) so that the voltage at pin 11 is 200V ±10V. For example, to operate the BIP-8211P at +300 Vdc, R is calculated by dividing the voltage difference, 100V (300-200) by the nominal current, 3.7 ma. This gives a result of 27K (100/3.7).
6. For logic "0" more positive than logic "1", reverse inputs and input complements.
7. All voltages given are referenced to terminal 1 or 12 (BIP-8211P) and 10 or 12 (BIP-8507P); i.e., the voltage at terminal 11 is +200V greater than at terminals 1, 10 or 12. Only one of the bias terminals is used in a given application.
8. Modules may be mounted either in front of or behind the panel (Figure 5). Front mounting should be employed only when there is no back lighting. Rear mounting may be used whether or not back lighting is present. Following this rule will eliminate light showing through the panel.
9. This applies to both modules.
10. This applies to terminal 1 (BIP-8211P) or terminal 10 (BIP-8507).

Burroughs Corporation / ELECTRONIC COMPONENTS DIVISION
PLAINFIELD, NEW JERSEY 07061

Printed in U.S.A. 15M1266



NOTE 1 * P1 NOT USED DURING OPERATION - PRESET ONLY
2 WEIGHT APPOX 35 OZ.
3 MOUNTING PLATE REMOVED WHEN OVEN IS USED

ITEM	PART NO.	DESCRIPTION	QTY.	REMARKS
P2,P3	UG1465/U	COAX CONNECTOR (USE UG188A COAX)	2	QPL
J2,J3	UG1468/U	COAX - CHASSIS CONNECTOR	2	QPL
P1	DSM07-7-15P	EXTERNAL CONNECTOR - PRESET ONLY	1	DEUTSCH CO
J1	DSM04-7-15S	PRESET CHASSIS CONNECTOR	1	DEUTSCH CO.

LIST OF MATERIAL

MAT'L. COVER - STAINLESS ST. FINISH PASSIVATE

UNLESS OTHERWISE SPECIFIED
FRACTIONS ±1/64
DECIMALS ±.005
ANGLES ±1°
REMOVE BURRS AND SHARP EDGES

	BY	DATE
DR.	[illegible]	23 Jun 67
CHK.		
ENG.		
PROD.		

FLOW CORPORATION
205 SIXTH STREET, CAMBRIDGE, MASS.

TITLE MINIATURE TIME CODE GENERATOR

SCALE 1:1 DO NOT SCALE PRINT
DWG. NO. C 4896-00001
REV. 0

FIGURE 1-1

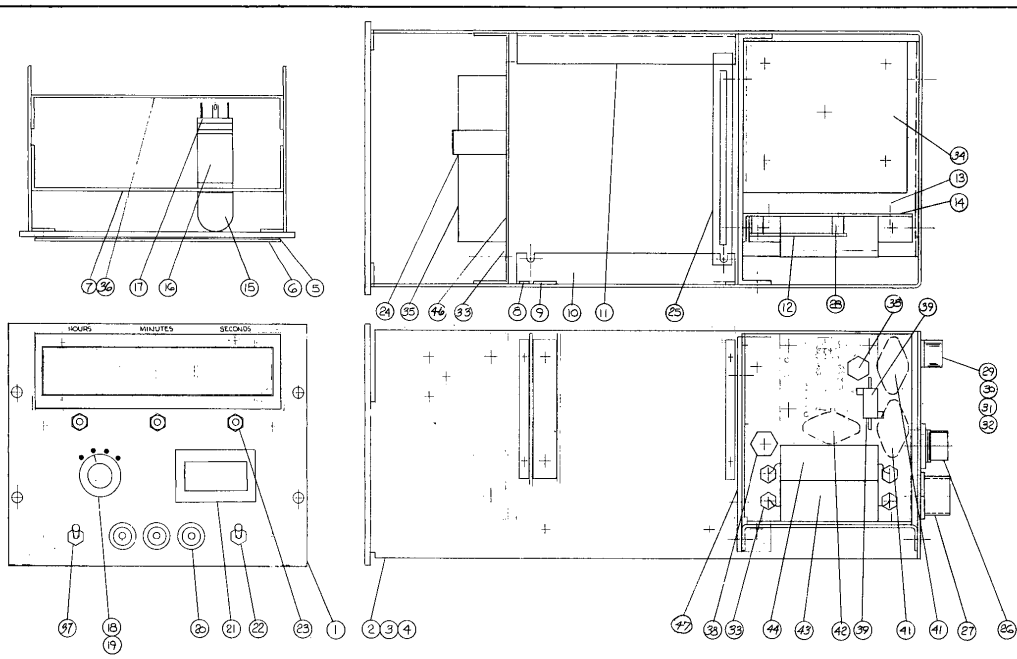


FIGURE 5.1

REVISIONS				
REV.	DESCRIPTION	BY	DATE	APPD.

ITEM	PART NO.	DESCRIPTION	QTY.	REMARKS
48	101-40121	CODE STRIPPER P.C. Bd. A-102	1	Digital Tech. Inc.
47	C-4896-11007	Bracket Stiffener Power Supply	1	
46	C-4896-11005	Bracket Capacitor Mounting	1	
45	C-4896-11001	Schematic		
44	39D	Capacitor 1000 μf @ 25V C3	1	Sprague
43	39D	" 110 μf @ 25V C4	1	Sprague
42	2N3584	Transistor (With Insulating Kit) Q3	1	QPL
41	2N3740	" " Q1-Q2	2	QPL
40				
39	RH-5	Resistor 35Ω 7½W R3	1	Dale
38	1N3879	Diode CR1-CR2	2	QPL
37	7055K20	Switch Toggle	1	Cutler Hammer
36	39D	Capacitor 10,000 μf @ 10V C1	1	Sprague
35	39D	" 4,000 μf @ 25V C2	1	"
34	5600-001	Transformer (Citan # TT-7078) T1	1	D.T.I
33	4826-1-0519	Terminal Standoff	8	CTC
32	3AG	Fuse 1/16 A. F3	1	Buss
31	3AG	" ¼ A. F2	1	"
30	3AG	" ½ A F1	1	"
29	HKP	Fuse Holder XFI-2-3	3	Buss
28	2372	Spacer ¼ OD x ½ Lg #4-40 Tap	4	H.H. Smith
27	MS3102A-10SL-3P	Connector	1	Amphenol
26	DSM04-7-15P	"	1	Deutsch
25	2VH31/1CN5	Connector	8	Viking
24	TM-23	Clamp Capacitor	2	Mallory
23	30-1	Switch Pushbutton	3	Grayhill
22	7050K20	" Toggle	1	Cutler Hammer
21	1521	Meter 0-10V Scale	1	Simpson
20	UG1094/U	Connector	3	Amphenol
19	V54031N	Switch Rotary 4 Pole 4 Positions	1	J.B.T.
18	1015-2B	Knob (With Index Line)	1	Vemaline
17	SK-149	Socket Nixie Tube	6	Burroughs
16	BIP-8211-P	Bipo Modules	6	"
15	B-5991	Tube Nixie	6	"
14	C-4896-11006	Support Angle P.S.	1	
13	D-4896-11003	Mtg. Base P.S.	1	
12	B-4896-11009	Clamp Bo Det. & Assy	1	
11	B-4896-11011-P2	Support Connector	1	
10	B-4896-11011-P1	" "	1	
9	B-4896-11010-1	Guides P.C. Card	14	
8	B-4896-11010-2	" "	4	
7	B-4896-11012	Support Nixie Tubes	1	
6	B-4896-11008	Mask	1	
5	B-4896-11013	Filter	1	
4	D-4896-11004-1	Cover Protective Top	1	
3	D-4896-11004-2	" " Bottom	1	
2	D-4896-11002	Chassis Detail	1	
1	D-4896-11001	Panel Front Detail & Engraving	1	

LIST OF MATERIAL

MAT'L	FINISH	BY	DATE
		DR. [illegible]	8-16-67
UNLESS OTHERWISE SPECIFIED		CHK.	
FRACTIONS ±1/64		ENG.	
DECIMALS ±.005		PROD.	
REMOVE BURRS AND SHARP EDGES			

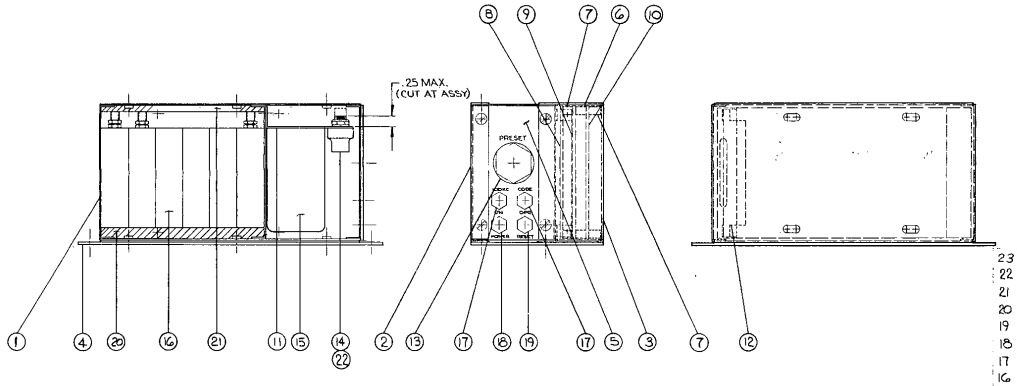
FLOW CORPORATION
205 SIXTH STREET, CAMBRIDGE, MASS.

TITLE: MAIN ASSY READER/PRESET

SCALE 1-1 | DWG. NO. D-4896-41001 | REV. A

DO NOT SCALE PRINT

54
53 A-4896-41506 A.G.C. Board A-101 1 Flow
52 A-4896-41002 Power Supply Board A-105 1 Flow
51 101-40909 Quad Flip Flop Board A-103 1 Digital Tech
50 [illegible] A-104 1 Digital Tech.
49 101-40122 Divider / Decoder Board A-104 1 Digital Tech.



NOTE:
1. INSULATE ITEM 8 FROM ITEM 1 BY CEMENTING MYLAR TO ITEM 1.

REVISIONS				
REV.	DESCRIPTION	BY	DATE	APPD.

ITEM	PART NO.	DESCRIPTION	QTY.	REMARKS
23	4896-1107	SHIELD	2	FLOW
22	2N1613	TRANSISTOR		QPL
21		NEOPRENE RUBBER 1/8" THK.	AR	GREENE Rubber
20		" " 1/4" THK.	AR	" "
19	7065K20	SWITCH, TOGGLE DPST (S2)	1	CUTLER HAMMER
18	7055K20	SWITCH, TOGGLE SPST (S1)	1	" "
17	UG1468/U	CONNECTOR (J2,3)	2	AMPHENOL
16	YS-2	BATTERY (BT1-6)	6	YARDNEY
15	MOD 1650	OSCILLATOR 1MC (Y1)	1	FLOW CORP
14	254-S1	HEAT SINK	1	WAKEFIELD ENG.
13	DSM04-7155	CONNECTOR (J1)	1	DEUTSCH
12	WD-22S	CONNECTOR (P1)	1	WINCHESTER
11	4896-1102	MTG. BRACKET OSCILLATOR	1	FLOW
10	4896-40004	ASSY PC-3 BOARD	1	FLOW
9	4896-40003	" PC-2 "	1	FLOW
8	4896-40002	" PC-1 "	1	FLOW
7	4896-1106-P2	SPACER	4	FLOW
6	4896-1106-P1	"	8	FLOW
5	4896-1103	PANEL, FRONT SILK SCREEN	1	FLOW
4	4896-1101	MOUNTING PLATE	1	FLOW
3	4896-1104	COVER, RIGHT	1	FLOW
2	4896-1104	COVER, LEFT	1	FLOW
1	4896-1105	CHASSIS	1	FLOW

LIST OF MATERIAL

MATL.	FINISH	BY	DATE
		DRWN.	8-3-67
UNLESS OTHERWISE SPECIFIED		CHK.	
FRACTIONS ±1/64		ENG.	
DECIMALS ±.005		PROD.	
REMOVE BURRS AND SHARP EDGES			

FLOW CORPORATION
203 SIXTH STREET, CAMBRIDGE, MASS.

TITLE: MAIN ASSEMBLY
MINIATURE TIME CODE GENERATOR

SCALE 1:1 | DWG. NO. 4896-40009 | REV. A

DO NOT SCALE PRINT

FIGURE 5-2

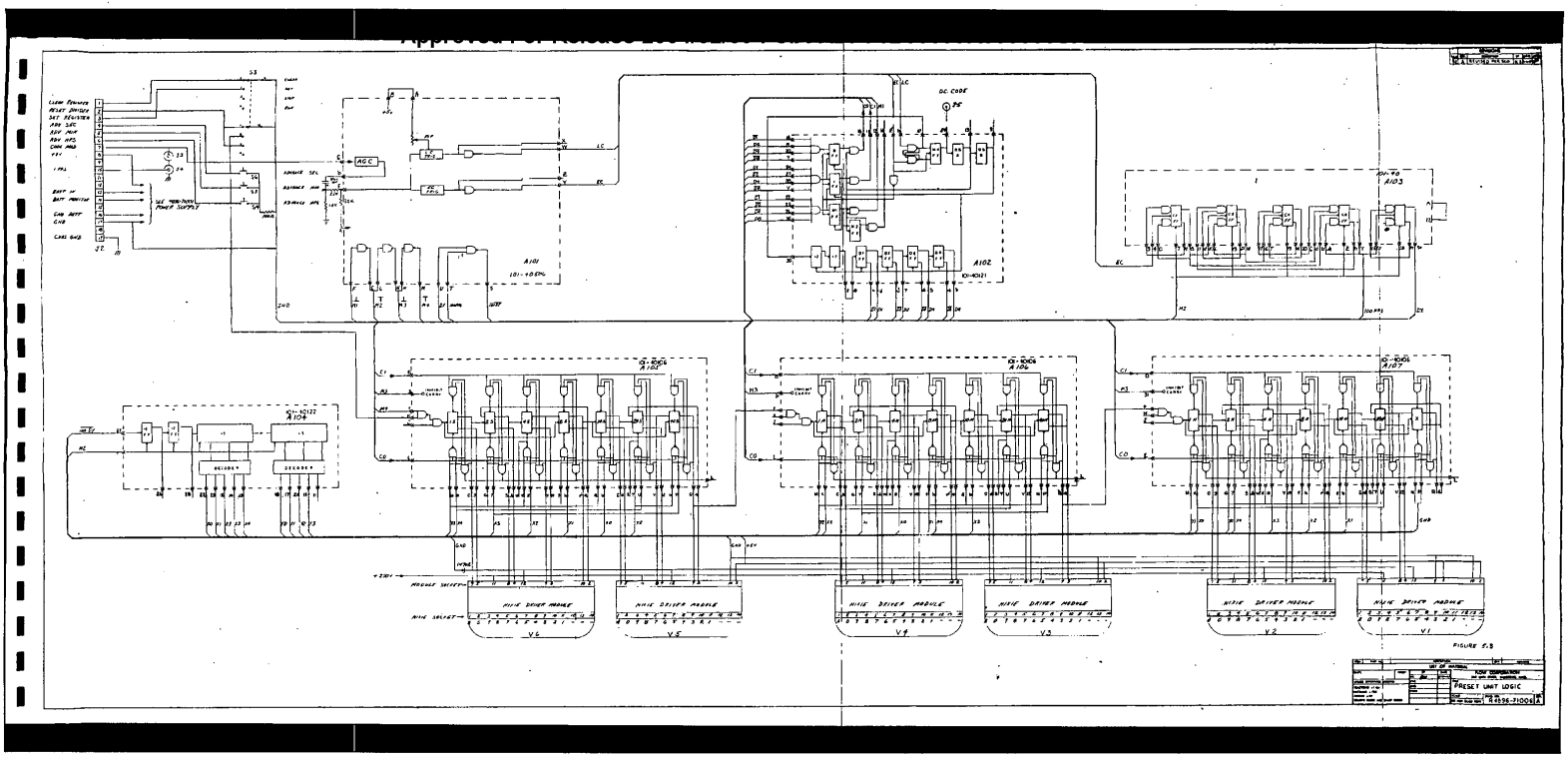
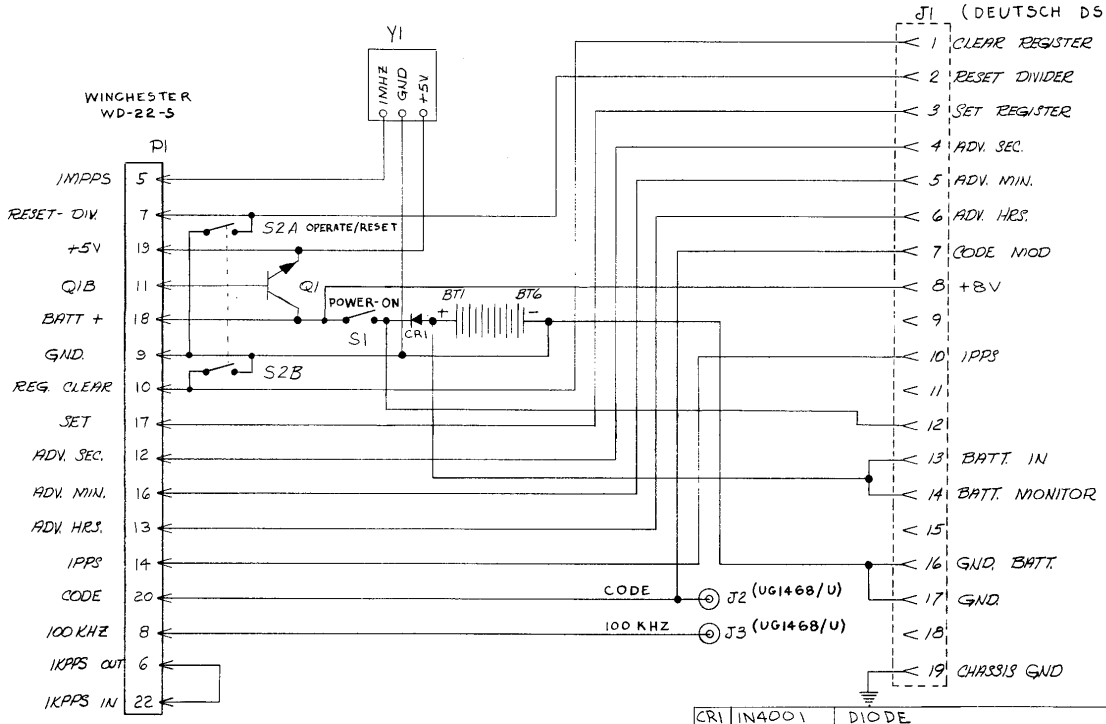


FIGURE 5-8

REVISIONS				
REV.	DESCRIPTION	BY	DATE	APPD.
A	E.C.O. #32	K.S.	4-12-68	



ITEM	PART NO.	DESCRIPTION	QTY.	REMARKS
CR1	IN4001	DIODE	1	QPL
S2	7065K20	SWITCH DPST	1	CUTLER HAMMER
S1	7055K20	SWITCH SPST	1	CUTLER HAMMER
P1	WD-22S	CONNECTOR	1	WINCHESTER
BT1-6	YS-2	BATTERY	6	YARDNEY
Q1	2N1613	TRANSISTOR	1	QPL
Y1	MOD. 1650	OSCILLATOR 1MC	1	FLOW CORP.
J1	DSM04-7-15S	CONNECTOR	1	DEUTSCH
J2,3	UG1468/U	CONNECTOR	1	QPL

LIST OF MATERIAL

MAT'L.	FINISH	BY	DATE
		DR.	7-7-67
UNLESS OTHERWISE SPECIFIED		CHK.	
FRACTIONS ±1/64		ENG.	
DECIMALS ±.005		PROD.	
ANGLES ±1° REMOVE BURRS AND SHARP EDGES			

FLOW CORPORATION
205 SIXTH STREET, CAMBRIDGE, MASS.

TITLE WIRING DIAGRAM
MINIATURE TIME CODE GENERATOR

SCALE DO NOT SCALE PRINT | DWG. NO. C-4896-70002 | REV. A

FIGURE 5.4

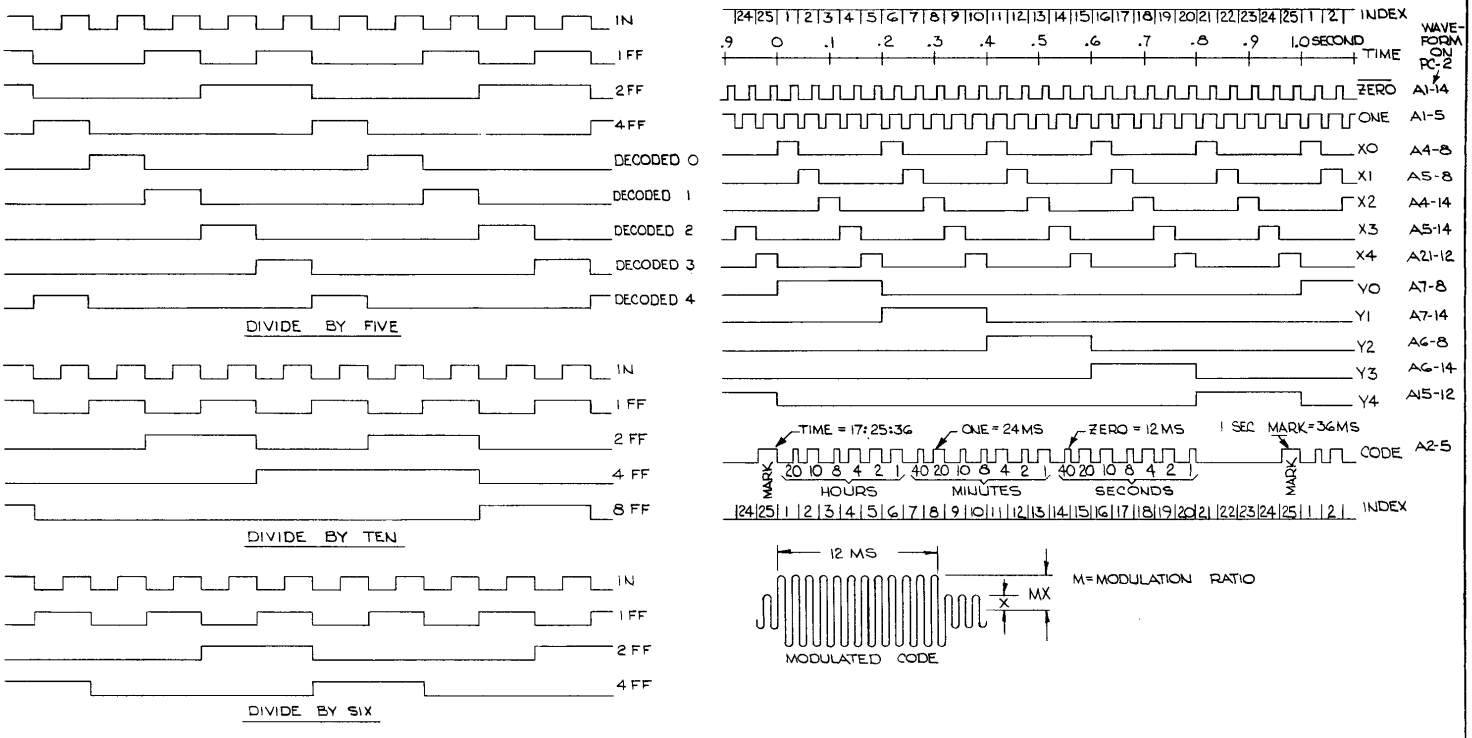
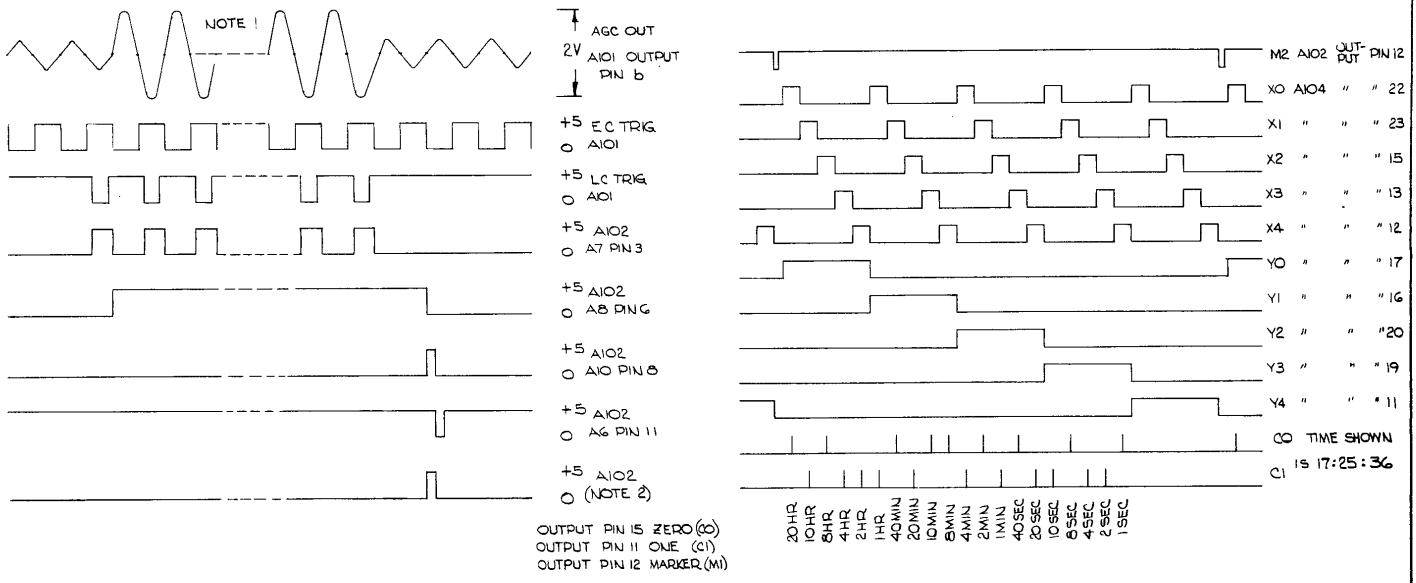


FIGURE 5.5

TIME CODE GENERATOR WAVEFORMS

FIGURE 5.5

FLOW CORPORATION
WATERTOWN, MASS.
WAVEFOMS, TIME CODE
GENERATOR C-4896-00002



NOTE:

1.- NUMBER OF LARGE CYCLES VARIES WITH BIT WEIGHT

2.- OUTPUT PULSE DEPENDS ON BIT WEIGHT.

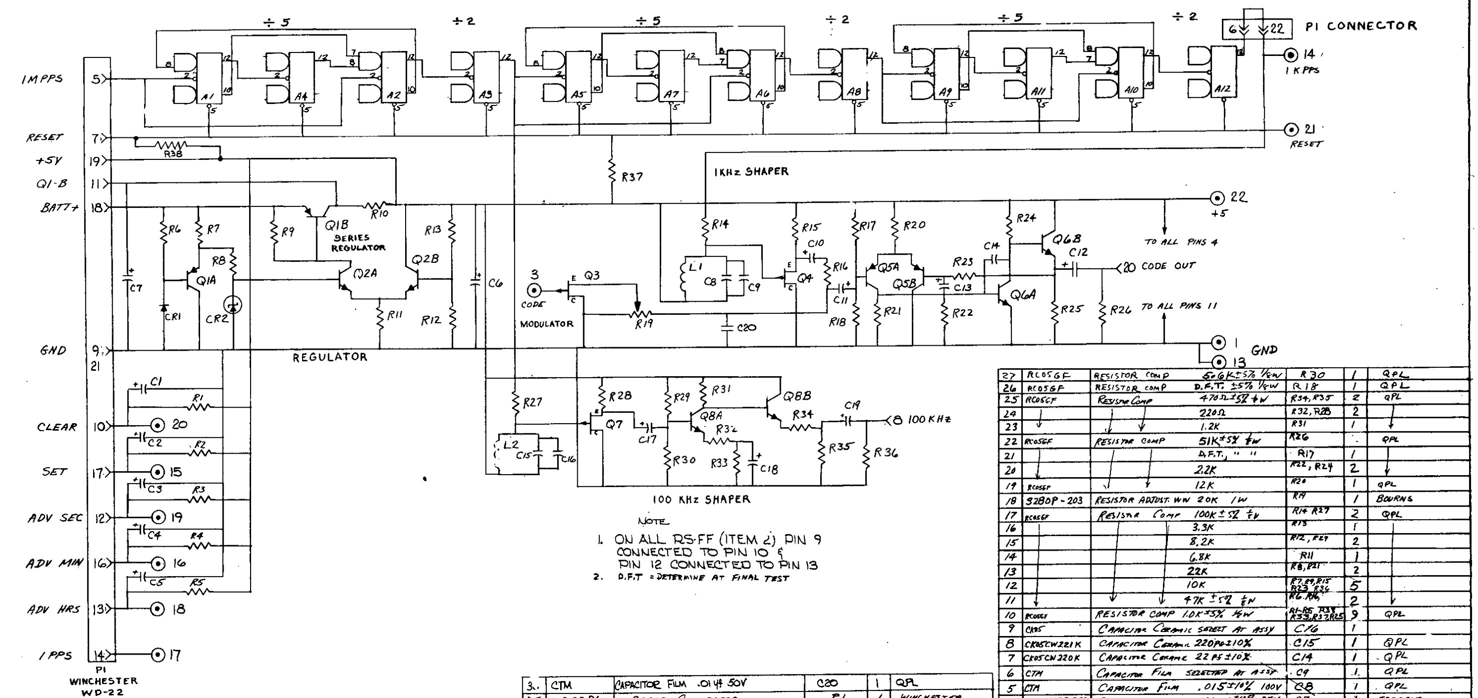
FIGURE 5.6

DECODER WAVEFORM

FIGURE 5.6

FLOW CORPORATION
WATERTOWN, MASS
WAVEFORMS, GROUND PRESET
UNIT C-4896-00003

REVISIONS				
REV.	DESCRIPTION	BY	DATE	APPD.
A	INITIAL RELEASE			
B	GEN REV.			
C	E.C.O. #32	K.S.	4-12-68	



NOTE

1. ON ALL RS-FF (ITEM 2) PIN 9 CONNECTED TO PIN 10 & PIN 12 CONNECTED TO PIN 13
2. D.F.T. = DETERMINE AT FINAL TEST

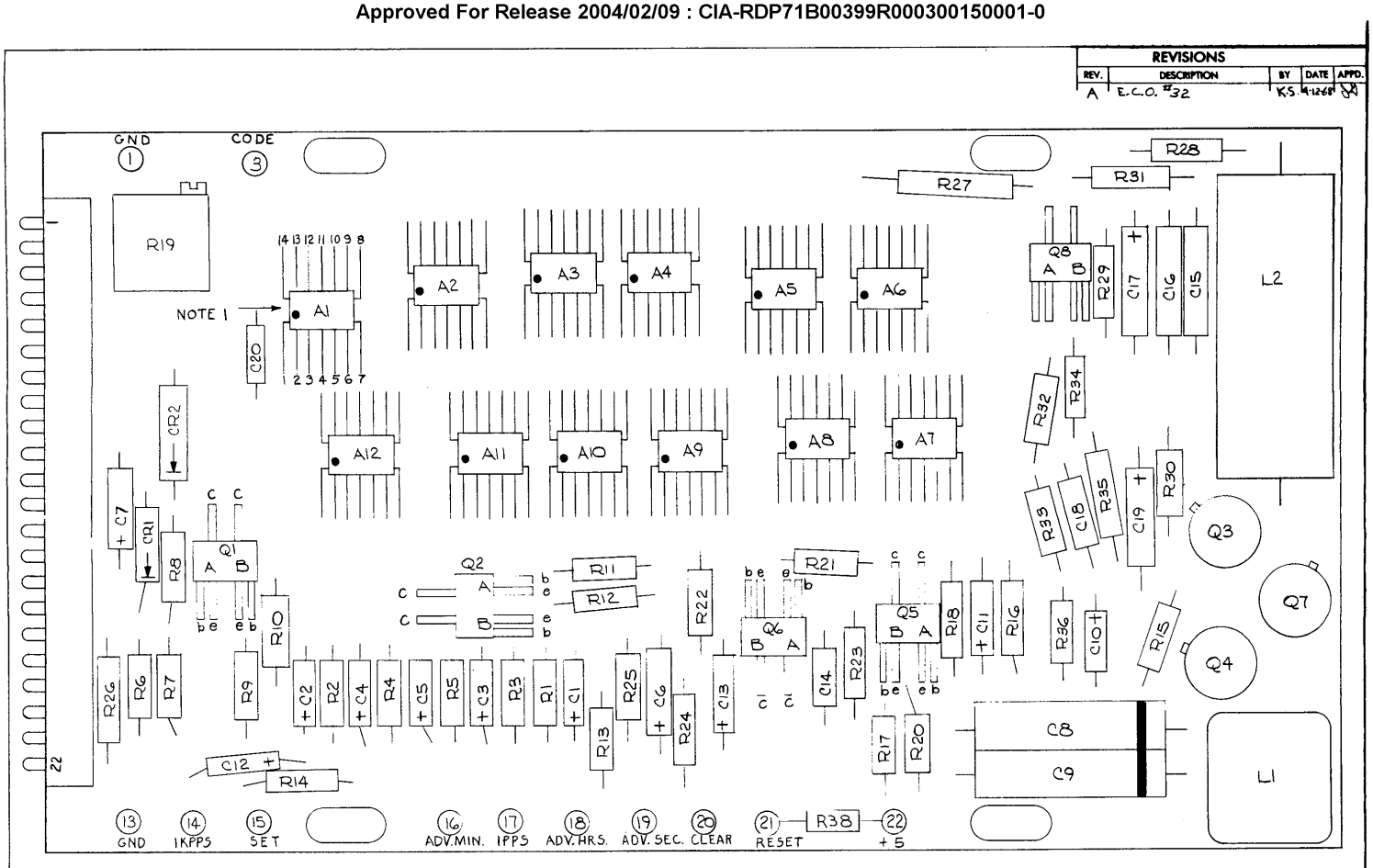
FIGURE 5.7

ITEM	PART NO.	DESCRIPTION	REFERENCE	QTY.	REMARKS
3.	CTM	CAPACITOR FILM .01 µf 50V	C20	1	QPL
35	WD22P6	BOARD CONNECTOR	P1	1	WINCHESTER
34	3220-2	CONNECTOR PLUG	AB1→AB12	12	CAMBION
33	1N 4685	DIODE ZENER	CR2	1	TRW/PSI
32	1N 4687	DIODE ZENER	CR1	1	TRW/PSI
31	2N 2608	TRANSISTOR FET	Q4 Q7	2	SILICONIX
30	2N2843	TRANSISTOR FET	Q3	1	SILICONIX
29	SP8888	TRANSISTOR DUAL NPN SILICON	Q2 Q6 Q8	3	FAIRCHILD
28	MD3251AF	TRANSISTOR DUAL PNP SILICON	Q1 Q5	2	MOTOROLA
27	3500-42	INDUCTOR 10MH (MS16223)	L2	1	DELEVAN
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

ITEM	PART NO.	DESCRIPTION	REFERENCE	QTY.	REMARKS
27	RC05GF	RESISTOR COMP 5.6K ±5% 1/8W	R30	1	QPL
26	RC05GF	RESISTOR COMP D.F.T. ±5% 1/8W	R18	1	QPL
25	RC05GF	RESISTOR COMP 470Ω ±5% 1/4W	R34, R35	2	QPL
24	↓	↓ 220Ω	R32, R28	2	↓
23		1.2K	R31	1	
22	RC05GF	RESISTOR COMP 51K ±5% 1/4W	R26	.	QPL
21	↓	D.F.T. " "	R17	1	↓
20		2.2K	R22, R24	2	
19	RC05GF	12K	R20	1	QPL
18	3280P-203	RESISTOR ADJUST. WW 20K 1W	R19	1	BOURNS
17	RC05GF	RESISTOR COMP 100K ±5% 1/8W	R14 R27	2	QPL
16	↓	↓ 3.3K	R13	1	↓
15		8.2K	R12, R29	2	
14		6.8K	R11	1	
13		22K	R8, R21	2	
12		10K	R7, R9, R15 R23 R36	5	
11		47K ±5% 1/8W	R6, R16	2	
10	RC05GF	RESISTOR COMP 1.0K ±5% 1/8W	R1-R5 R38 R33, R37, R25	9	QPL
9	CK05	CAPACITOR CERAMIC SELECT AT ASSY	C16	1	
8	CK05CW221K	CAPACITOR CERAMIC 220PF ±10%	C15	1	QPL
7	CK05CN220K	CAPACITOR CERAMIC 22PF ±10%	C14	1	QPL
6	CTM	CAPACITOR FILM SELECTED AT ASSY	C9	1	QPL
5	CTM	CAPACITOR FILM .015 ±10% 100V	C8	1	QPL
4	150D223X9035A	CAPACITOR TANT .022µf ±10% 35V	C7	1	SPRAGUE
3	CS13BC475K	CAPACITOR TANTALUM 4.7µf ±10% 10V	C1 to C6, C10 to C13, C17 to C19	13	QPL
2	SN74L71R-1	INTEGRATED CIRCUIT RS FF	A1 to A12	12	TEXAS INSTRUMENTS
1	4891-30002	P.C. BOARD	PC-1	1	FLOW CORP

LIST OF MATERIAL

MAT'L.	FINISH	BY	DATE	FLOW CORPORATION 205 SIXTH STREET, CAMBRIDGE, MASS.
UNLESS OTHERWISE SPECIFIED		DR. P.Q. Harvey	3 Jul 67	TITLE MINIATURE TCG PC-1 INPUT-OUTPUT SCHEMATIC
FRACTIONS ±1/64		CHK.		
DECIMALS ±.005		ENG.		
ANGLES ±30'		PROD.		SCALE / DO NOT SCALE PRINT
REMOVE BURRS AND SHARP EDGES				DWG. NO. 4896-70001 S1 — REV. C



SCHEMATIC # 4896-70001 S1

ITEM	PART NO.	DESCRIPTION	QTY.	REMARKS

LIST OF MATERIAL

MAT'L.	FINISH	BY	DATE
		DR. [illegible]	8-2-67
UNLESS OTHERWISE SPECIFIED		CHK.	
FRACTIONS ±1/64		ENG.	
DECIMALS ±.005		PROD.	
REMOVE BURRS AND SHARP EDGES			

FLOW CORPORATION
205 SIXTH STREET, CAMBRIDGE, MASS.

TITLE ASSY PC-1 BOARD

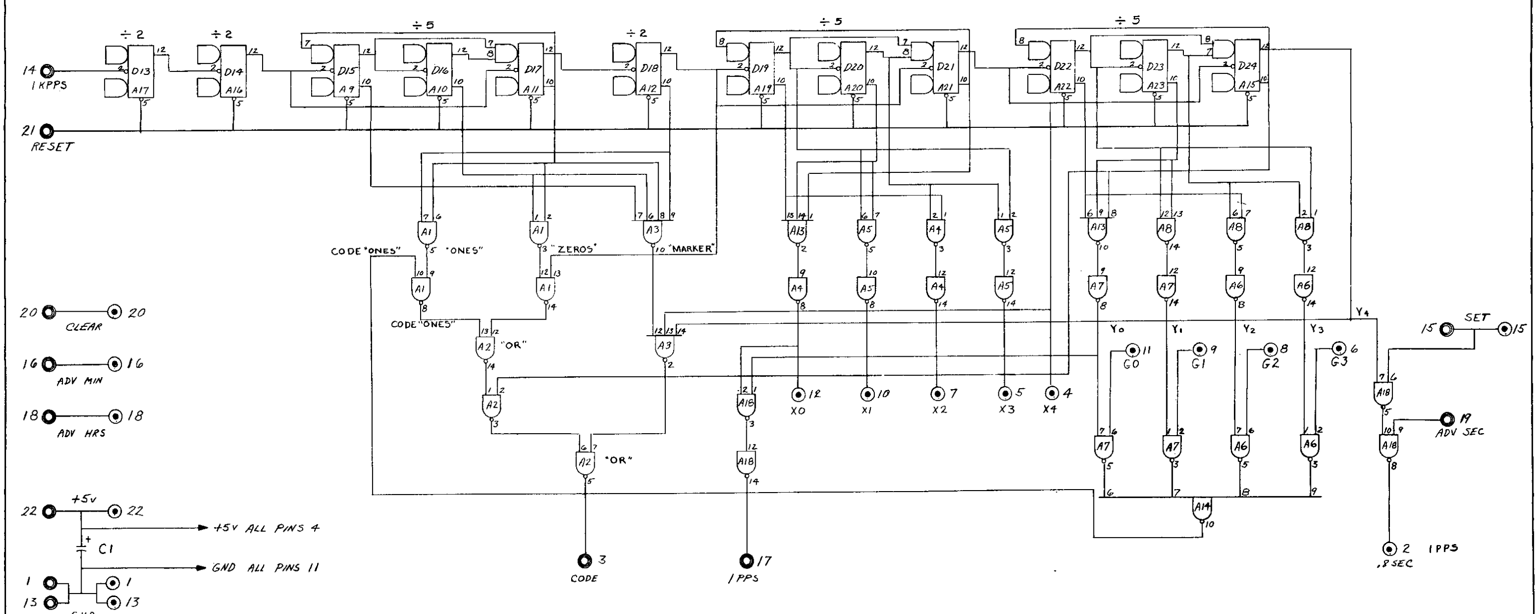
SCALE 4:1 DO NOT SCALE PRINT

DWG. NO. 4896-40002 REV. A

FIGURE 5.8

REVISIONS

REV.	DESCRIPTION	BY	DATE	APPD.
B	A18 CHANGED TO SN74L20 SCHEMATIC REVISED			



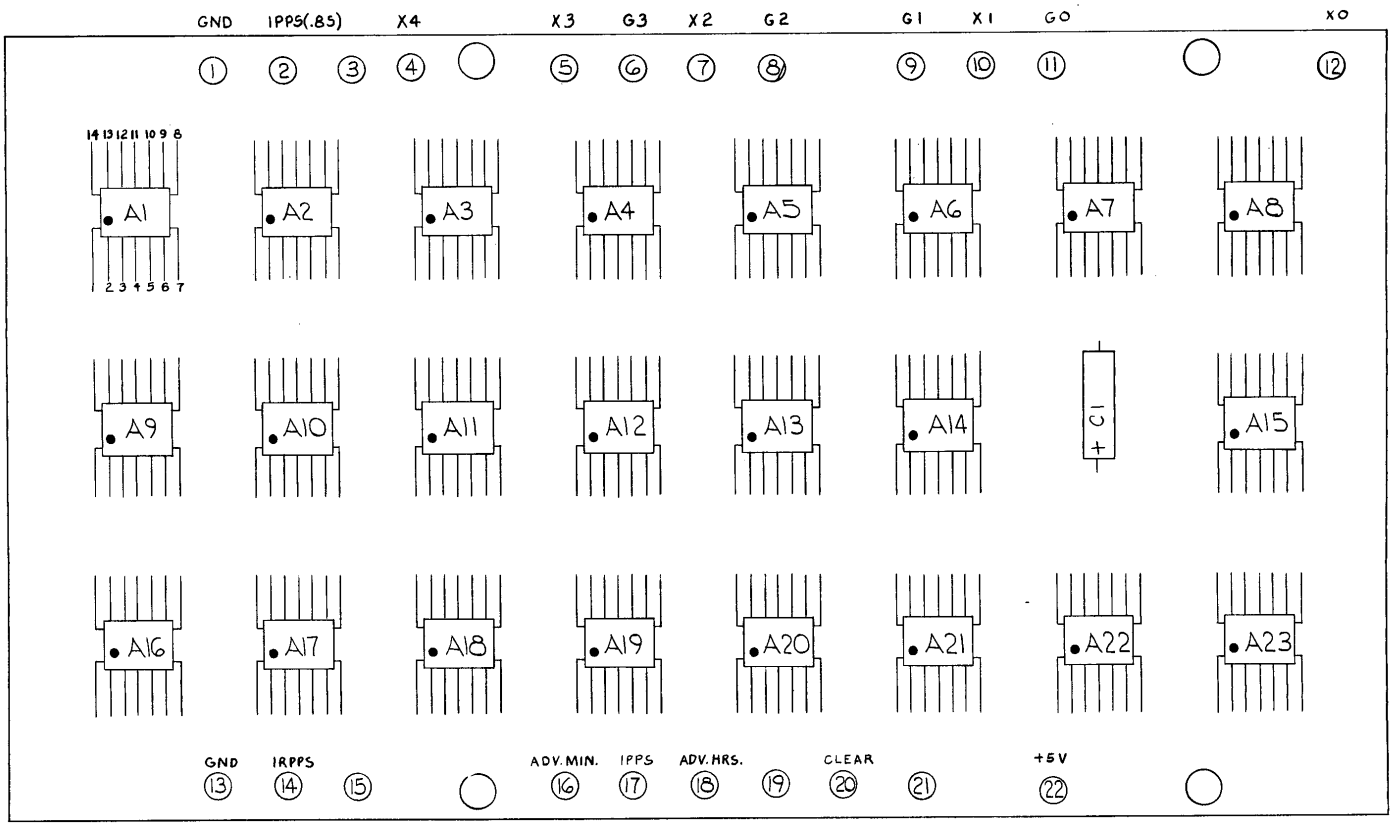
NOTE.
1. ON ALL RS-FF (ITEM 2) PIN 9 CONNECTED TO PIN 10 & PIN 12 CONNECTED TO PIN 13

ITEM	PART NO.	DESCRIPTION	REFERANCE	QTY.	REMARKS
8	3220-2	CONNECTOR PLUG	2, 4 TO 12	10	CAMBION
7	2650-2	CONNECTORS PLUG-JACK	1,13,15,16,18,20,22	7	CAMBION
6	2378-2	CONNECTORS JACKS	3,14,17,19,21	5	CAMBION
5	CS13BC475K	CAPACITOR TANTALUM 4.7 μf ±10% 10V	C1	1	QPL
4	SN74L00R-1	INTEGRATED CIRCUIT QUAD 2 IN NAND	A1, A2, A4 TO 8, A18	8	TEXAS INSTRUMENTS
3	SN74L20R-1	" " DUAL 4 IN NAND	A3, A13, A14	3	" "
2	SN74L71R-1	" " RS FLIP FLOP	A9 TO A12, A15, A16, A17, A19 TO 23	12	" "
1	4891-30003	P.C. BOARD	PC2	1	FLOW CORP

LIST OF MATERIAL

MAT'L.	FINISH	BY	DATE	
		DR.	30 Jun 67	FLOW CORPORATION 205 SIXTH STREET, CAMBRIDGE, MASS.
UNLESS OTHERWISE SPECIFIED		CHK.		TITLE MINIATURE TCG PC-2 DIVIDER DECODER SCHEMATIC
FRACTIONS ±1/64 DECIMALS ±.005 ANGLES ±30' REMOVE BURRS AND SHARP EDGES		ENG.		SCALE ~ DO NOT SCALE PRINT
		PROD.		DWG. NO. D4896-70001-S2 REV. B

FIGURE 5.9



SCHEMATIC # 4896-70001 SH2

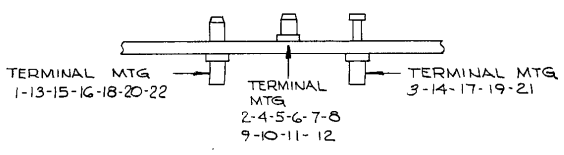
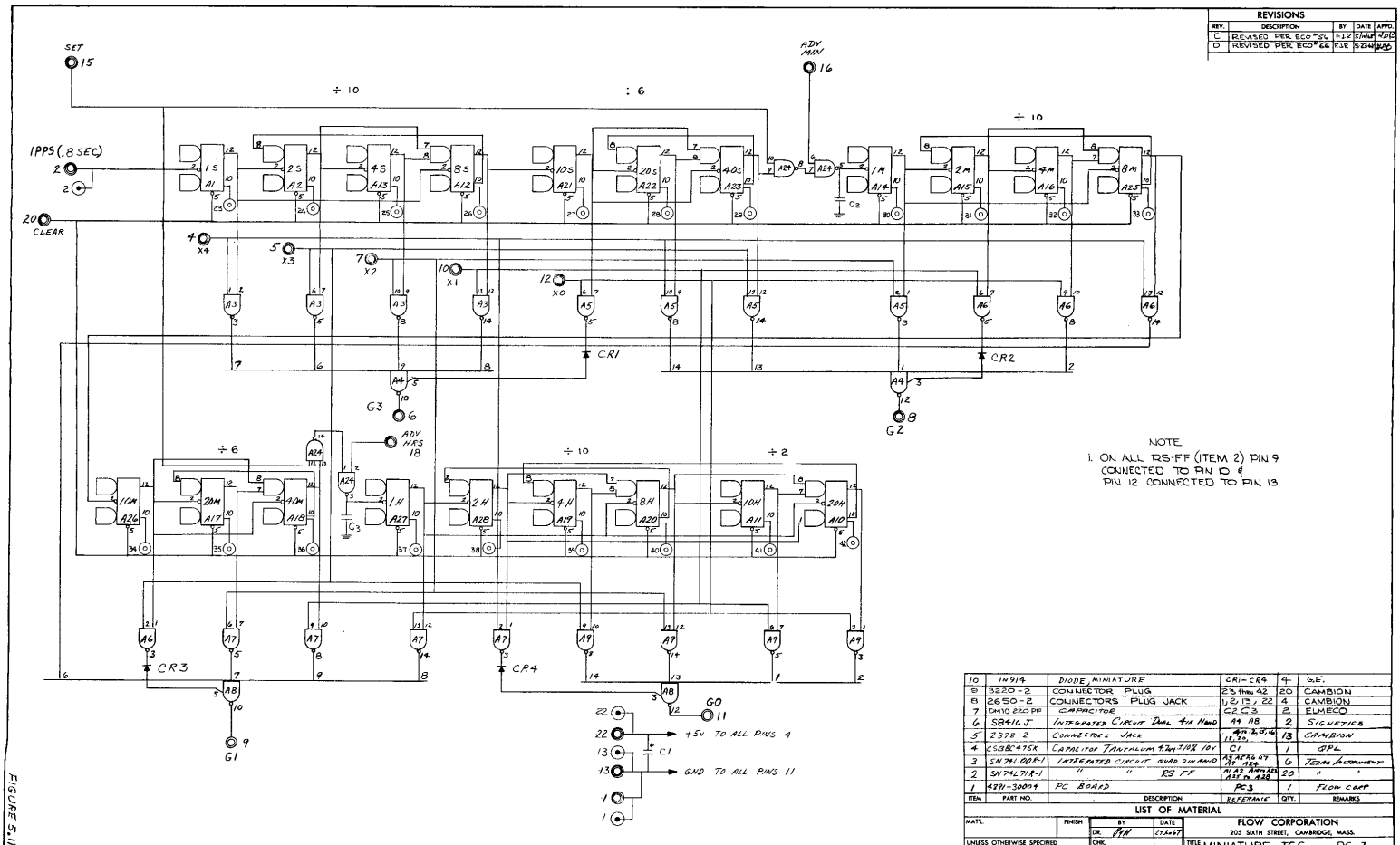


FIGURE 5.10

ITEM	PART NO.	DESCRIPTION	QTY.	REMARKS
		LIST OF MATERIAL		

MAT'L.	FINISH	BY DAT WE	DATE 8-3-67	FLOW CORPORATION 205 SIXTH STREET, CAMBRIDGE, MASS.
UNLESS OTHERWISE SPECIFIED		CHK.		TITLE ASSY PC-2 BOARD
FRACTIONS ±1/64 DECIMALS ±.005 ANGLES ±1° REMOVE BURRS AND SHARP EDGES		ENG. PROD.		SCALE 4:1 DO NOT SCALE PRINT DWG. NO. 4896-40003 REV. A



NOTE
1. ON ALL RS-FF (ITEM 2) PIN 9 CONNECTED TO PIN 5 & PIN 12 CONNECTED TO PIN 13

REVISIONS				
REV.	DESCRIPTION	BY	DATE	APPD.
C	REVISED PER ECO "54	F.J.C	2/4/67	[illegible]
D	REVISED PER ECO "66	F.J.C	5/23/67	[illegible]

ITEM	PART NO.	DESCRIPTION	REFERENCE	QTY.	REMARKS
10	IN914	DIODE, MINIATURE	CR1-CR4	4	G.E.
9	3220-2	CONNECTOR PLUG	23 thru 42	20	CAMBION
8	2650-2	CONNECTORS PLUG JACK	1 & 13, 22	4	CAMBION
7	DM10,250 PF	CAPACITOR	C2,C3	2	ELMECO
6	SB416J	INTEGRATED CIRCUIT DUAL 4in NAND	A4 A8	2	SIGNETICS
5	2378-2	CONNECTOR JACK	A7 thru A9, 12, 15, 16, 24, 26	13	CAMBION
4	CSBBC475K	CAPACITOR TANTALUM 4.7uf 10V	C1	1	GPL
3	SN74L00P-1	INTEGRATED CIRCUIT QUAD 2in NAND	A3 A5 A6 A7 A8 A9	6	TEXAS INSTRUMENT
2	SN74L71P-1	" " RS FF	A1 A2 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21 A22 A23 A25 A27	20	" "
1	4891-30004	PC BOARD	PC-3	1	FLOW CORP

LIST OF MATERIAL

MATL.	FINISH	BY	DATE
		DR. RTH	12-1-67
UNLESS OTHERWISE SPECIFIED		CHK.	
FRACTIONS ±1/64		ENG.	
DECIMALS ±.010		PROD.	
REMOVE BURRS AND SHARP EDGES			

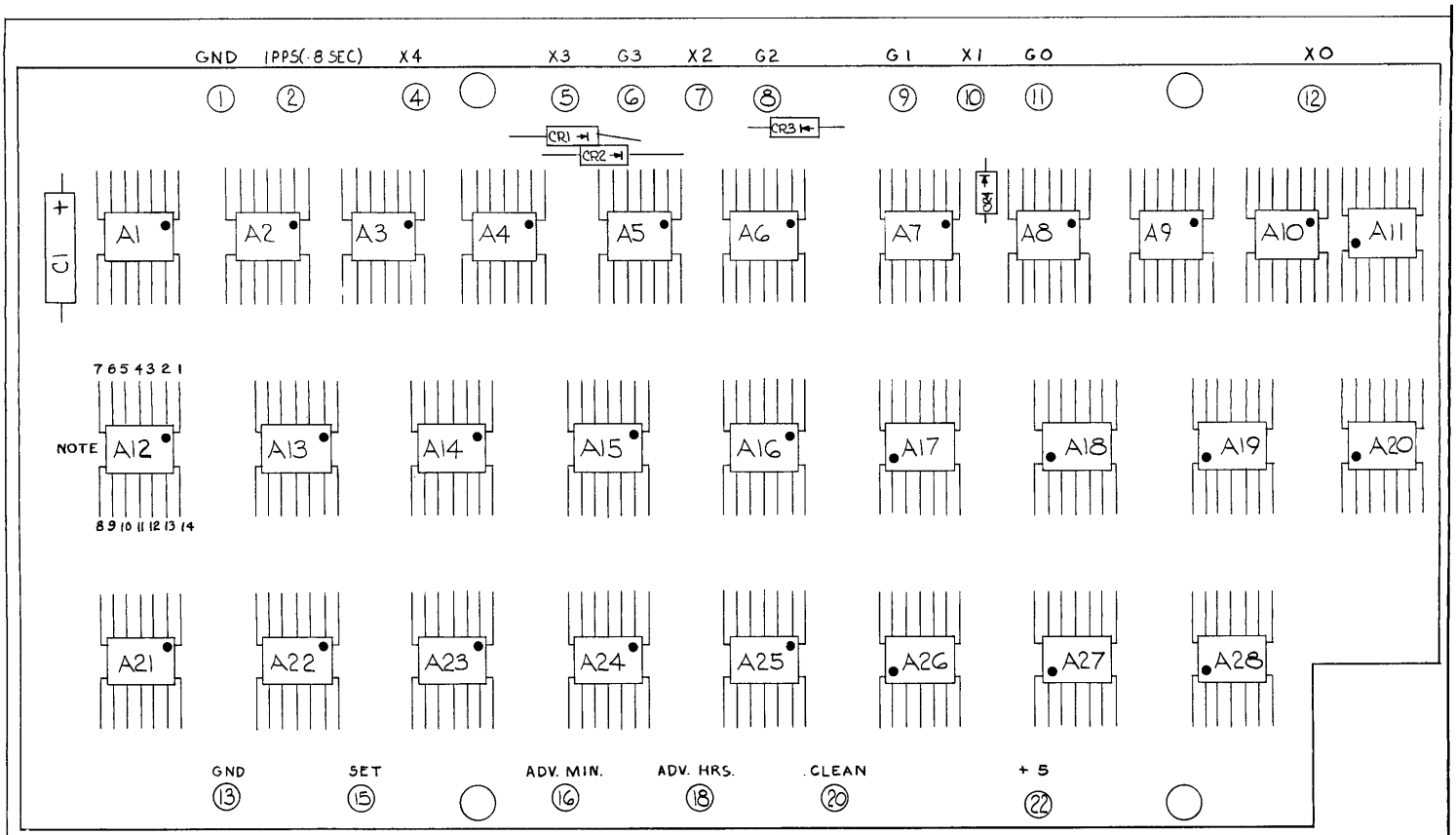
FLOW CORPORATION
205 SIXTH STREET, CAMBRIDGE, MASS.

TITLE MINIATURE TCG PC-3 REGISTER SCHEMATIC

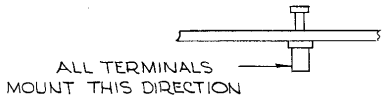
SCALE DO NOT SCALE PRINT

DWG. NO. D 4896-70001-S3 REV. D

FIGURE 5.11



SCHEMATIC #4896-70001-53



ITEM	PART NO.	DESCRIPTION	QTY.	REMARKS

LIST OF MATERIAL

MAT'L.	FINISH	BY	DATE
		DR.	8-367
UNLESS OTHERWISE SPECIFIED		CHK.	
FRACTIONS ±1/64		ENG.	
DECIMALS ±.005		PROD.	
ANGLES ±1°			
REMOVE BURRS AND SHARP EDGES			

FLOW CORPORATION
205 SIXTH STREET, CAMBRIDGE, MASS.

TITLE ASSY PC-3 BOARD

SCALE 4:1 | DWG. NO. 4896 40004 | REV. B

DO NOT SCALE PRINT

FIGURE 5-12

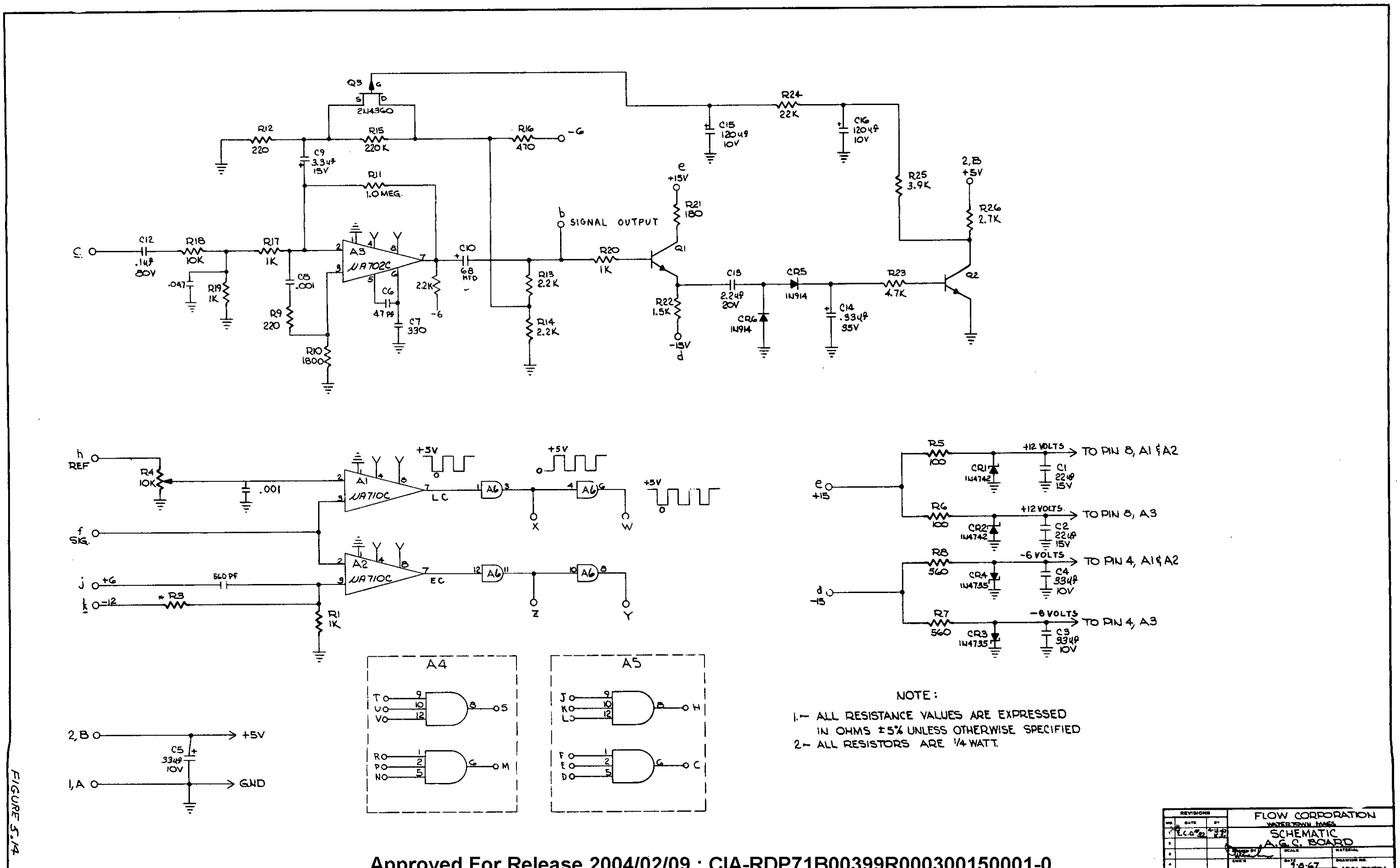


FIGURE 5.14

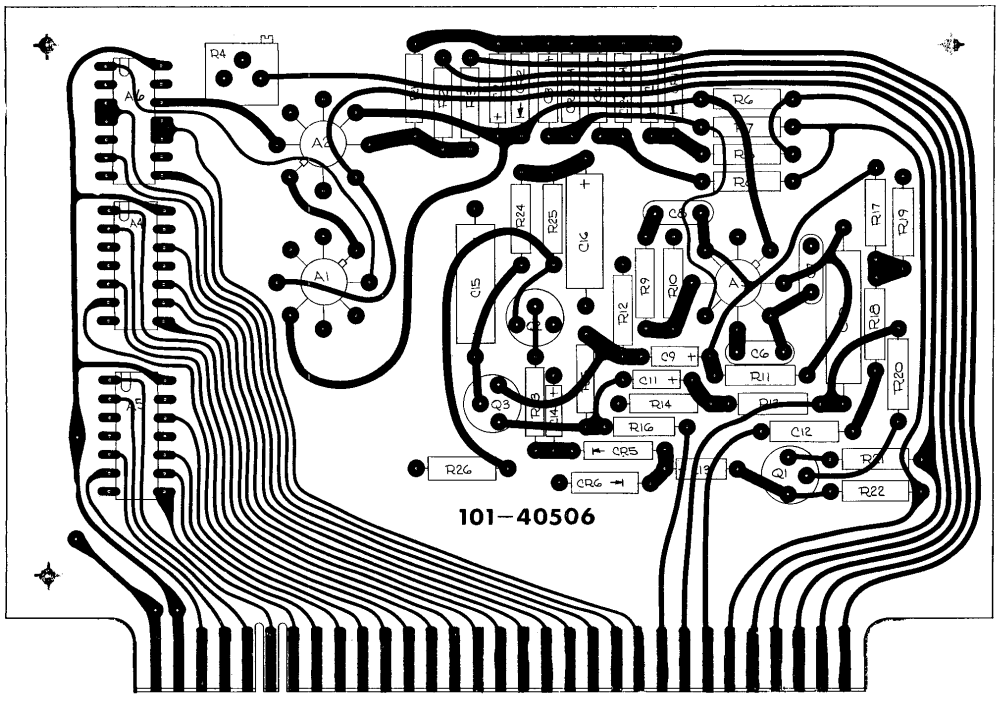


FIGURE 5.14

ITEM	PART NO.	DESCRIPTION	QTY.	REMARKS
		LIST OF MATERIAL		

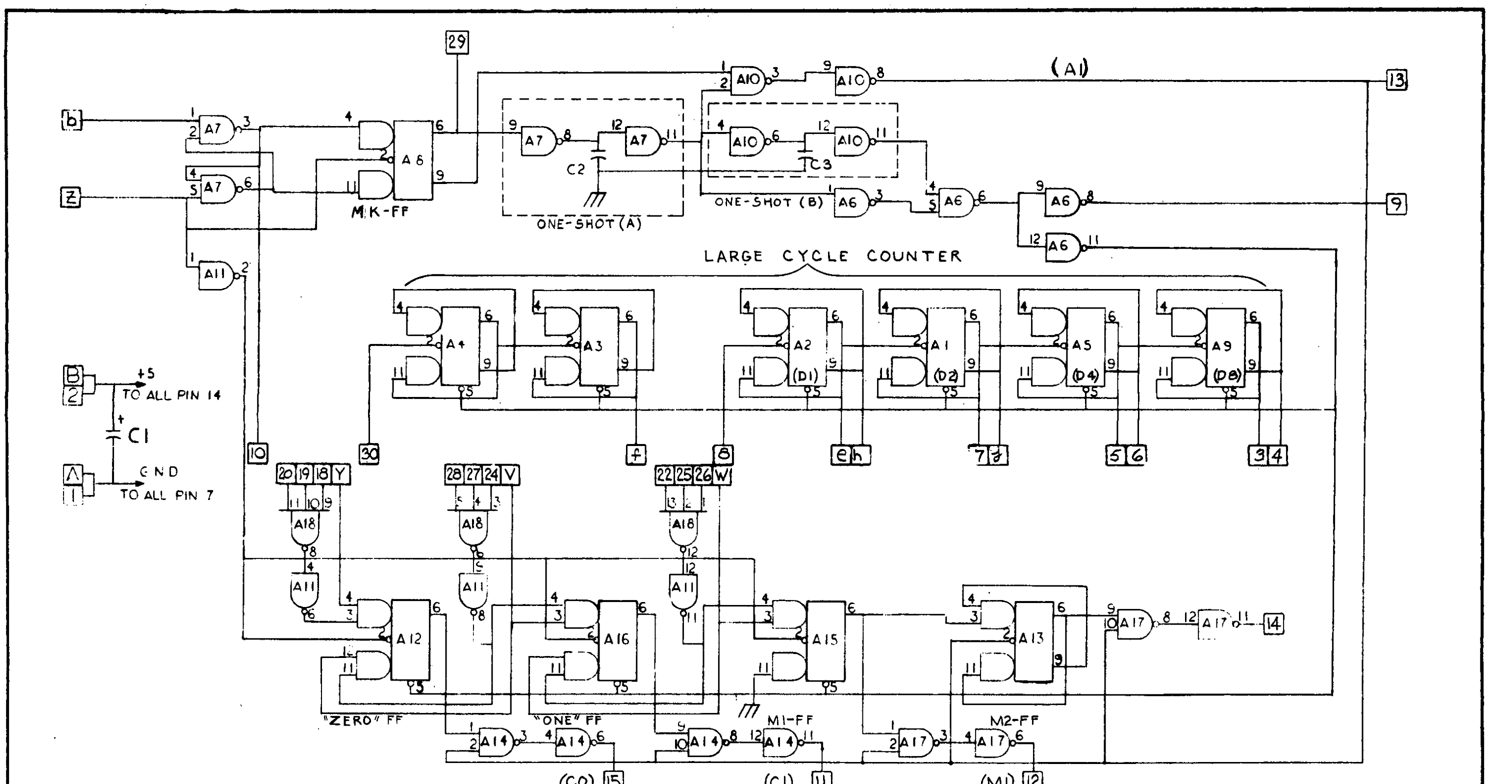
MATL.	FINISH	BY	DATE
		DK Ware	10-24-67
UNLESS OTHERWISE SPECIFIED		CHK.	
FRACTIONS ±1/64		ENG.	
DECIMALS ±.005		PROD.	
ANGLES ±30'			
BREAK SHARP EDGES			

FLOW CORPORATION
205 SIXTH STREET, CAMBRIDGE, MASS.

TITLE: A.G.C. BOARD ASSY

SCALE 4/1 | DWG. NO. D-4896-40506 | REV. A

DO NOT SCALE PRINT



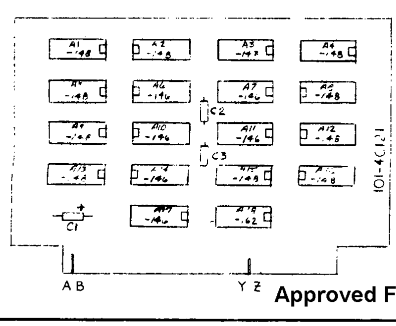


FIGURE 5.15

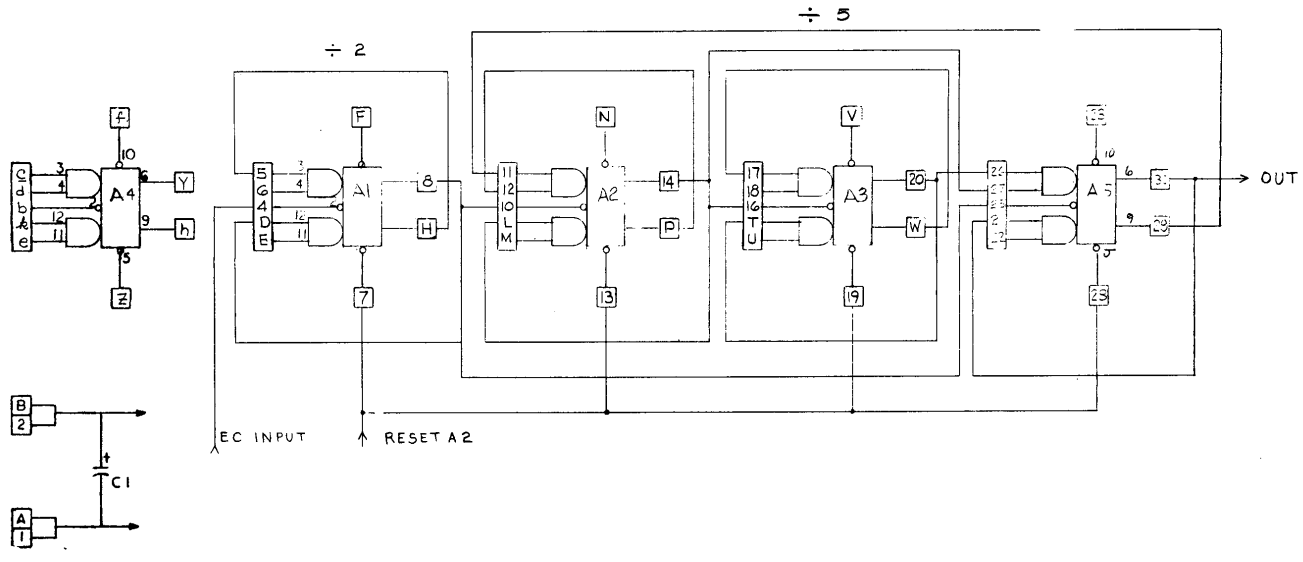
TEXAS INST. SN15862N	6	A18	1	3130-162	INTEGRATED CIRCUIT TRIPLE 3 IN GATE	DT
TEXAS INST. SN15846N	5	A6 A7 A10 A11 A14 A17	6	3130-146	" " QUAD 2 IN GATE	DT
TEXAS INST. SN15848N	4	A1 - A5 A8 A9 A12 A13 A15 A16	11	3130-148	" " FLIP-FLOP	DT
	3	C2 C3	2	MC80V202AM	CAPACITOR CERAMIC .002 MF ± 20% 100 VDC	AEROVOX
	2	C1	1	CS13-BC 336M	CAPACITOR TANT. 33 μf ± 20% 10 v	OPL
	1	~	1	101-40121	BOARD P.C.	DT
	ITEM	REF	QTY	PART NO	DESCRIPTION	MFGR

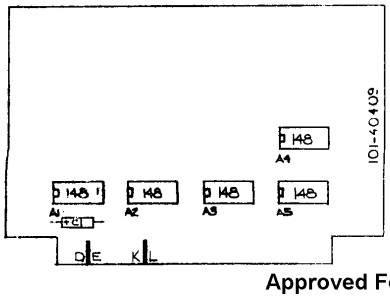
REVISIONS		
NO.	DATE	BY
1	E.C.O. 32	4-12-68 K.S.
2		
3		
4		

FLOW CORPORATION
WATERTOWN MASS

CODE STRIPPER
LOGIC & ASSY

DRAWN BY | SCALE ~ | MATERIAL
CHK'D | DATE | DRAWING NO 101-40121





6					
5					
4					
3	A1-A5	5	3130-148	INTEGRATED CIRCUIT FLIP-FLOP	DTI
2	C1	1	CS13-BC336A	CAPACITOR TANT 33uf ±20% 16V	QPL
1		1	101-40409	BOARD PC	DTI

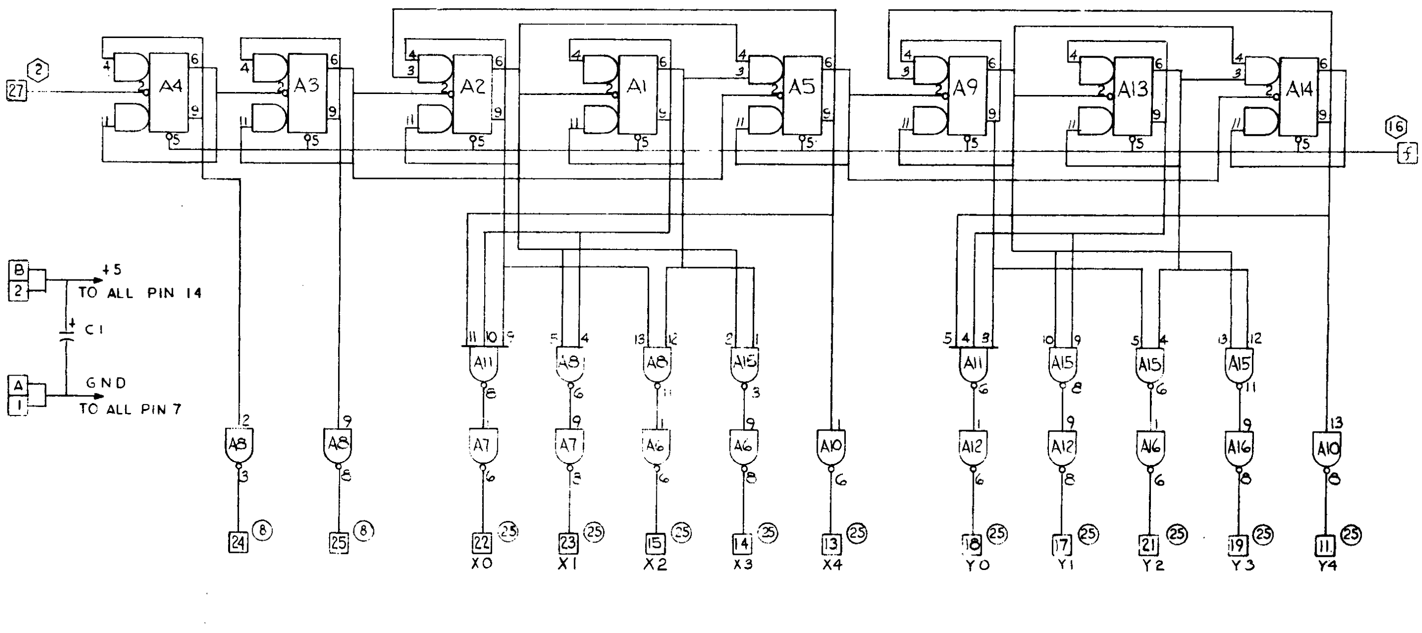
TEXAS INST. SN15848N

REVISIONS			
NO	DATE	BY	
1	E.C.O. 32	12/18/69 K.S.	
2			
3			
4			
5			

FLOW CORPORATION
WATERTOWN MASS
PENTA FLIP-FLOP BOARD
LOGIC & ASSY

DRAWN BY	SCALE	MATERIAL
CHK'D	DATE 2 JUNE 67	DRAWING NO 101-40409
TRACED	APP'D	

FIGURE 5.16



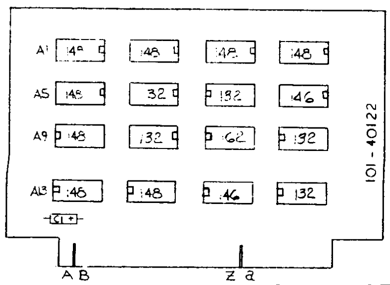


FIGURE 5-17

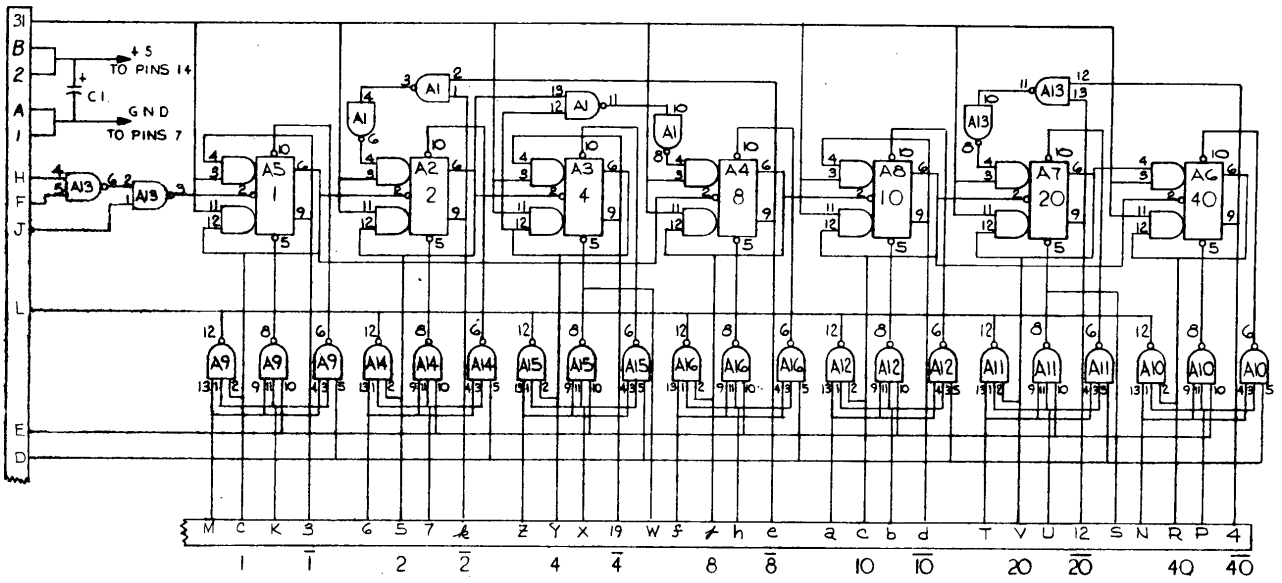
TEXAS INST. SN15862N	6	A11	1	3130-162	INTEGRATED CIRCUIT TRIPLE 3IN GATE	DTI
TEXAS INST. SN15846N	5	A8-A15	2	3130-146	INTEGRATED CIRCUIT QUAD 2IN GATE	DTI
TEXAS INST. SN15832N	4	A6, A7, A10, A12, A16	5	3130-132	INTEGRATED CIRCUIT	DTI
TEXAS INST. SN15848N	3	A1-A5, A9, A13, A14	8	3130-148	INTEGRATED CIRCUIT F.F	DTI
	2	C1	1	CS13-BC336M	CAPACITOR TANTALUM 33µf ±20% 10v	QPL
	1		1	101-40122	BOARD P.C.	D.T.I.
	ITEM	REF	QTY	PART NO	DESCRIPTION	MFGR

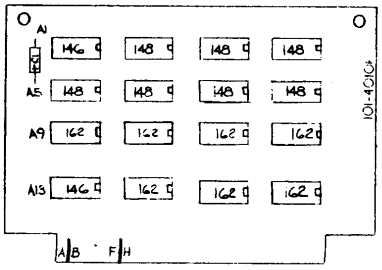
REVISIONS		
NO.	DATE	BY
1	E.C.O. #32	4-12-68 K.S.
2		
3		
4		
5		

FLOW CORPORATION
WATERTOWN MASS

DIVIDER / DECODER
LOGIC & ASSY

DRAWN BY | SCALE ~ | MATERIAL
CHK'D | DATE 12 Jun 67 | DRAWING NO. 101-40122
TRACED | APP'D





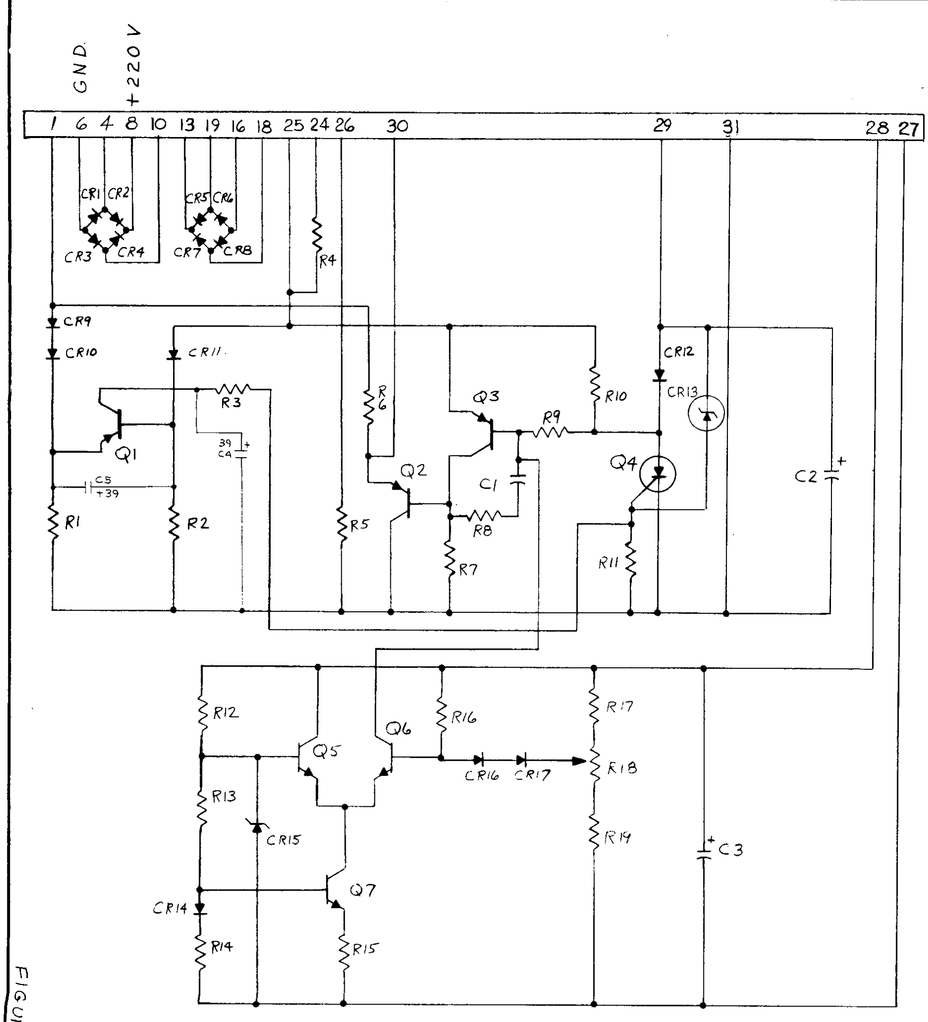
ITEM	REF	QTY	PART NO	DESCRIPTION	MFR
5	A1, A13	2	3130-146	INTEGRATED CIRCUIT QUAD 2-IN GATE	
4	A9-A12, A14-A16	7	3130-162	" " TRIPLE 3-IN GATE	DTI
3	A2-A8	7	3130-148	" " FLIP-FLOP	DTI
2	C1	1	CSB-BC336M	CAPACITOR TANT. 33uf ±20% 10V	RPL
1		1	101-30106	BOARD P.C.	DTI

REVISIONS

NO	DATE	BY
1		
2		
3		
4		
5		
6		

FLOW CORPORATION
WATERTOWN MASS
REGISTER BOARD
LOGIC ASSY
DRAWN BY
SCALE
MATERIAL
CHK'D
DATE
TRACED
SHT #
101-40106

FIGURE 5.18



ITEM	REF	QUAN	PART #	DESCRIPTION	MFGR
21	R5	1	RC07GF	RESISTOR COMP 4.7Ω 5% ¼W	QPL
20	R19	1	RC07GF	RESISTOR COMP 68Ω 5% ¼W	QPL
19	R18	1	62PA	POTENTIOMETER WW 1W 100Ω	BECKMAN
18	R15	1	RC07GF	RESISTOR COMP 82Ω 5% ¼W	QPL
17	R12	1		120Ω 5% ¼W	
16	R9, 14	2		1K 5% ¼W	
15	R8	1		470Ω 5% ¼W	
14	R6	1		6.8K 5% ¼W	
13	R4, 10, 16	3		220Ω 5% ¼W	
12	R3, 11	2		100Ω 5% ¼W	
11	R1, 2, 7 R13, 17	5	RC07GF	RESISTOR COMP 2.2K 5% ¼W	QPL
10	Q5-6-7	3	2N3704	TRANSISTOR NPN SILICON	TI
9	Q4	1	TI 145 A0	THYRISTOR	TI
8	Q1, 2, 3	3	2N4423	TRANSISTOR PNP SILICON	TI
7	CR15	1	1N4371A	DIODE ZENER (2.7V)	
6	CR13	1	1N753	DIODE ZENER (6.2V)	
5	CR9-11 CR14 CR16-17	6	1N914	DIODE SILICON	QPL
4	CR5-CR8 CR12	5	1N4001	RECTIFIER SILICON	
3	CR1-CR4	4	1N4004	RECTIFIER SILICON	
2	C2, C3, C4, C5	2	CS13BC396K	CAPACITOR, TANT 39µf 10V	QPL
1	C1	1	CTM	CAPACITOR FILM .0033µf 100V	QPL

REVISIONS		
NO.	DATE	BY
1	REVERSED POLARITY OF CR13	1/29/68 V.A.N.
2	E.C.O. #32	4-12-68 K.S.
3		
4		

FLOW CORPORATION
WATERTOWN MASS

PSIA REGULATOR SCHEMATIC

DRAWN BY: VAN | SCALE | MATERIAL
CHK'D | DATE: 3 May 67 | DRAWING: 4896-71002
TRACED | APP'D

FIGURE 5.19

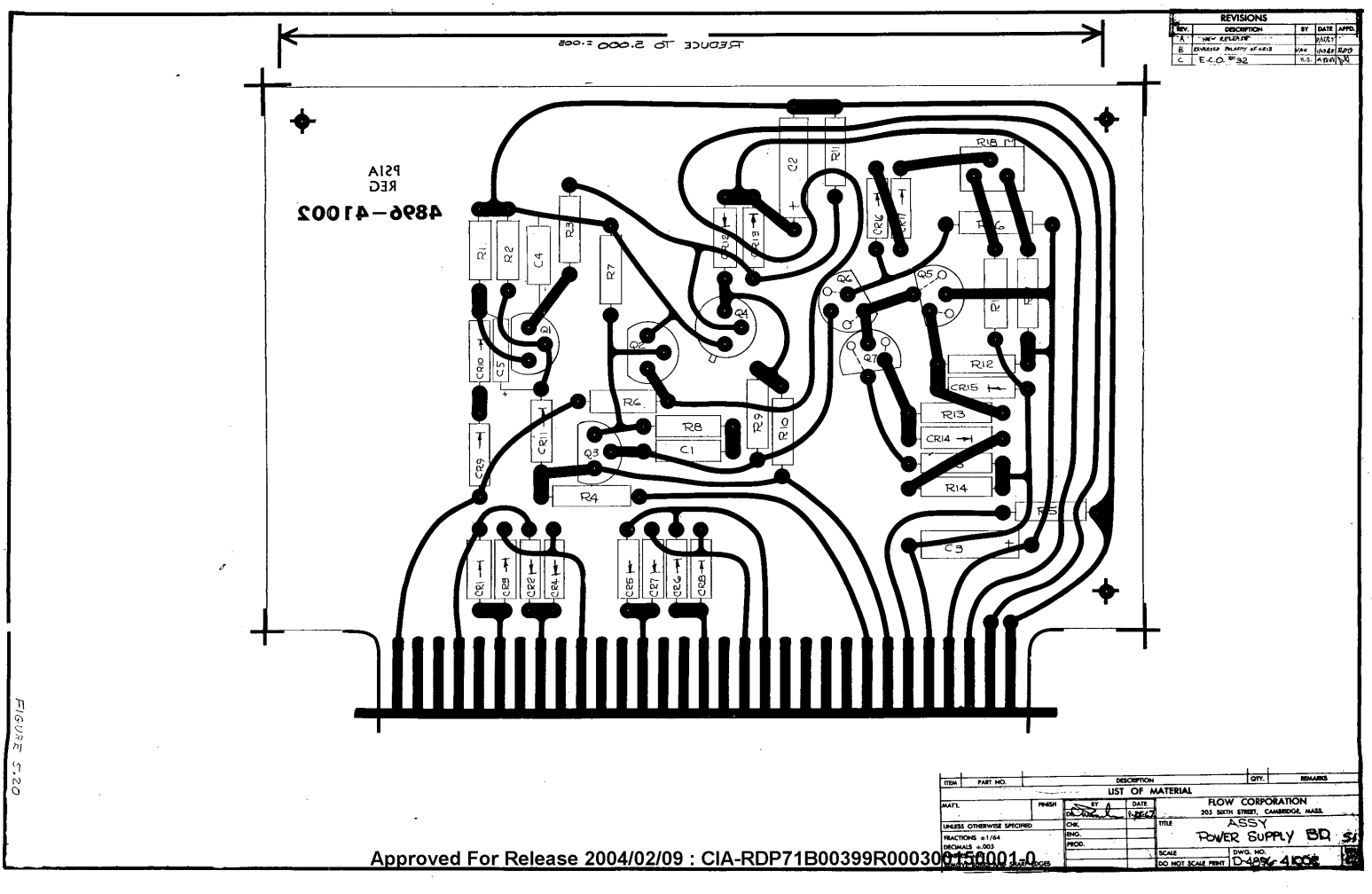
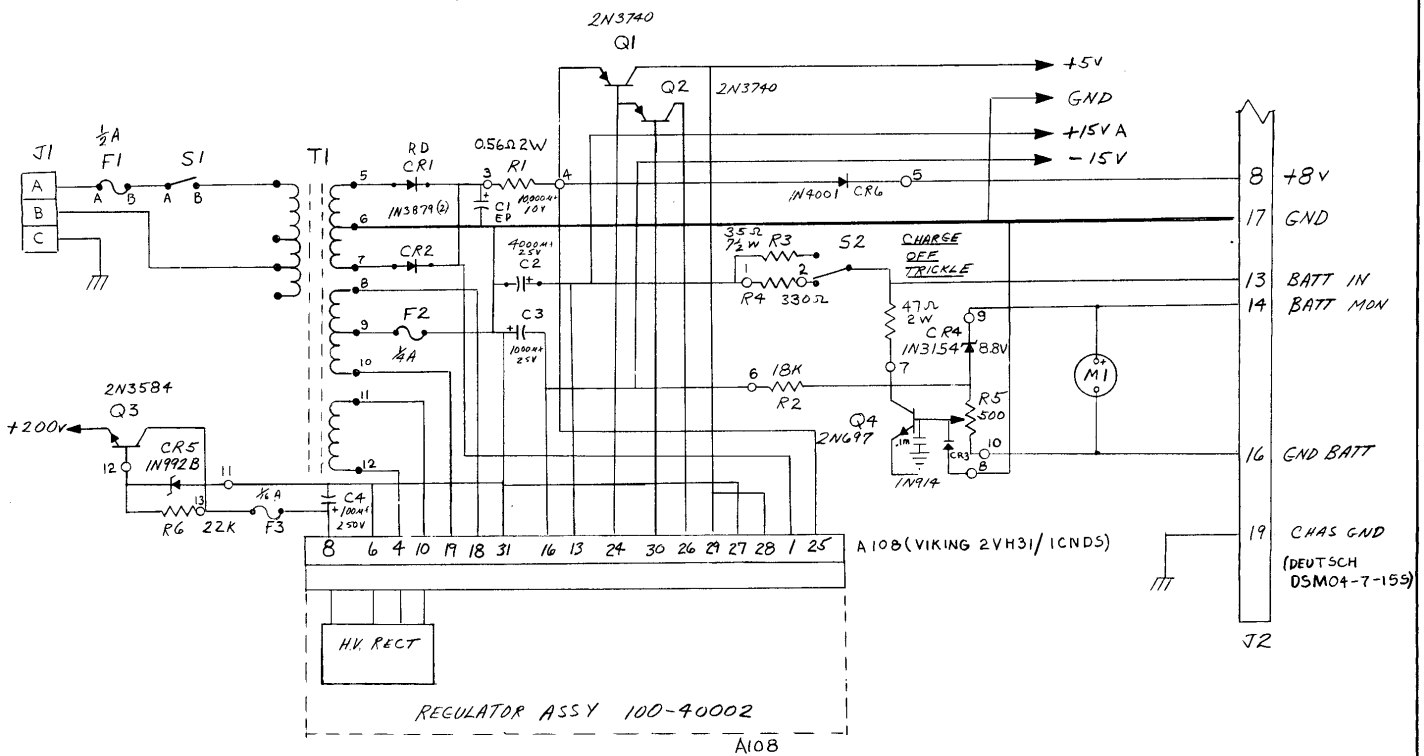


FIGURE 5120

REVISIONS				
REV.	DESCRIPTION	BY	DATE	APPD.
A	E.C.O. #32	K.S.	4/12/67	



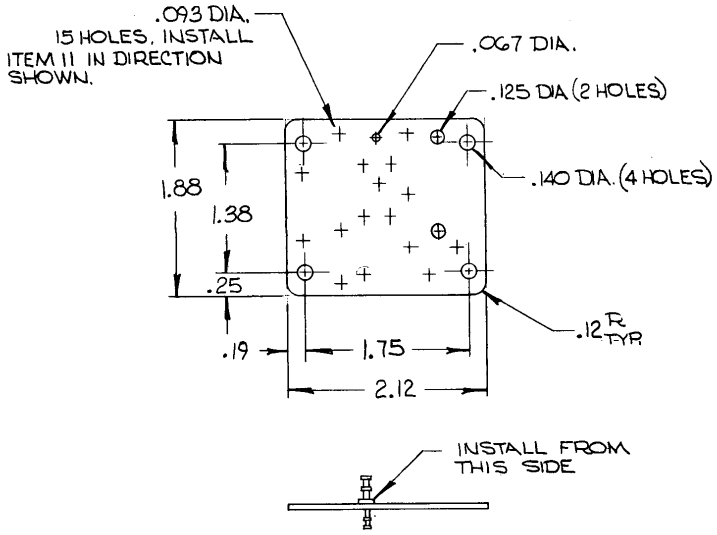
ITEM	PART NO.	DESCRIPTION	QTY.	REMARKS

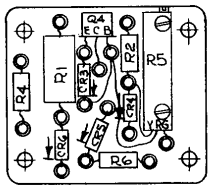
LIST OF MATERIAL

MAT'L.	FINISH	BY	DATE	FLOW CORPORATION
		DR.		205 SIXTH STREET, CAMBRIDGE, MASS.
UNLESS OTHERWISE SPECIFIED		CHK.		TITLE SCHEMATIC POWER SUPPLY S2
FRACTIONS ±1/64		ENG.		
DECIMALS ±.005		PROD.		
ANGLES ±1° REMOVE BURRS AND SHARP EDGES				SCALE DO NOT SCALE PRINT

DWG. NO. C-4896-71001 REV. A

FIGURE 5.21





ITEM	PART NO	DESCRIPTION	QTY
11	1043-2	TERMINAL FEED-THRU C.T.C.	15
10	1N4001	DIODE CR6	1
9	1N992B	DIODE CR5	1
8	1N3154	DIODE CR4	1
7	1N914	DIODE CR3	1
6	2N697	TRANSISTOR Q4	1
5	Allen Bradley	RES COMP 22K ±5% 1/4W R6	1
4	224L-1-101	RES. VAR. 100Ω (R5) BOURNS	1
3	Allen Brad.	RES COMP 330Ω ±5% 1/4W (R4)	1
2	Allen Brad	RES. COMP. 18K ±5% 1/4W (R2)	1
1	I.R.C. BWH	RES. COMP. 1Ω ±5% 2W (R1)	1

FLOW CORPORATION
205 SIXTH STREET, CAMBRIDGE, MASS.

MAT'L 1/16 THK EPOXY GLASS (G10)

FINISH

TOLERANCE UNLESS OTHERWISE SPECIFIED
FRACTIONAL DIM. ± 1/64
DECIMAL DIM. ± .005
BENDING LOCATION ± 1/64

DRAWN
CHECKED
DATE
SCALE

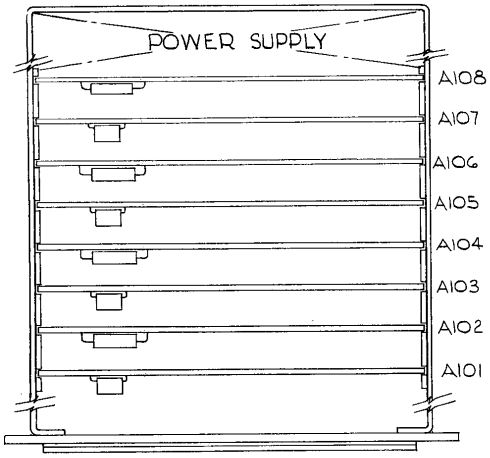
TITLE COMP. BOARD DETAIL & ASSY

DWG. NO. B-4896-11009

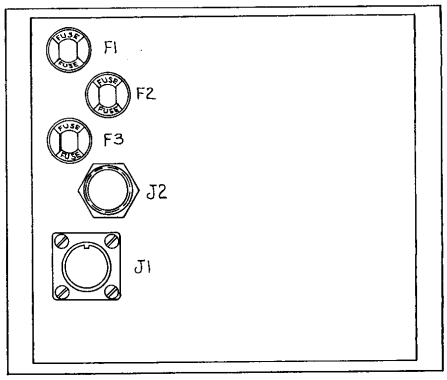
REV. A

LET'R	REVISION	DATE	BY

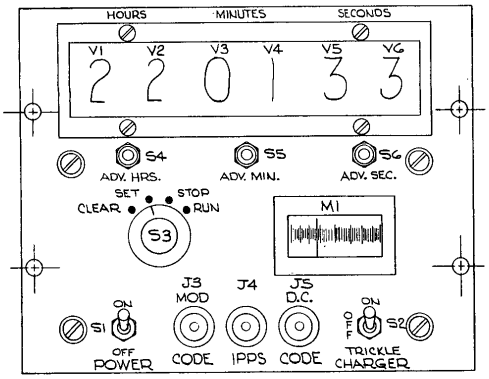
FIGURE 5.22



TOP VIEW



REAR VIEW



FRONT VIEW

FIGURE 5.23

ITEM	PART NO.	DESCRIPTION	QTY.	REMARKS
		LIST OF MATERIAL		

MAT'L.	FINISH	BY	DATE	FLOW CORPORATION
		DR.	10-6-67	205 SIXTH STREET, CAMBRIDGE, MASS.
UNLESS OTHERWISE SPECIFIED		CHK.		TITLE CHASSIS-COMPONENT LAYOUT
FRACTIONS ±1/64		ENG.		
DECIMALS ±.005		PROD.		
ANGLES ±1°				SCALE 1/4 DWG. NO. C-4896-41003 REV. A
REMOVE BURRS AND SHARP EDGES				DO NOT SCALE PRINT

REVISIONS					
E.C.O.	REV.	DESCRIPTION	BY	DATE	APPD.
11	A	MAS 4816-00002	K.S.	3-21-66	

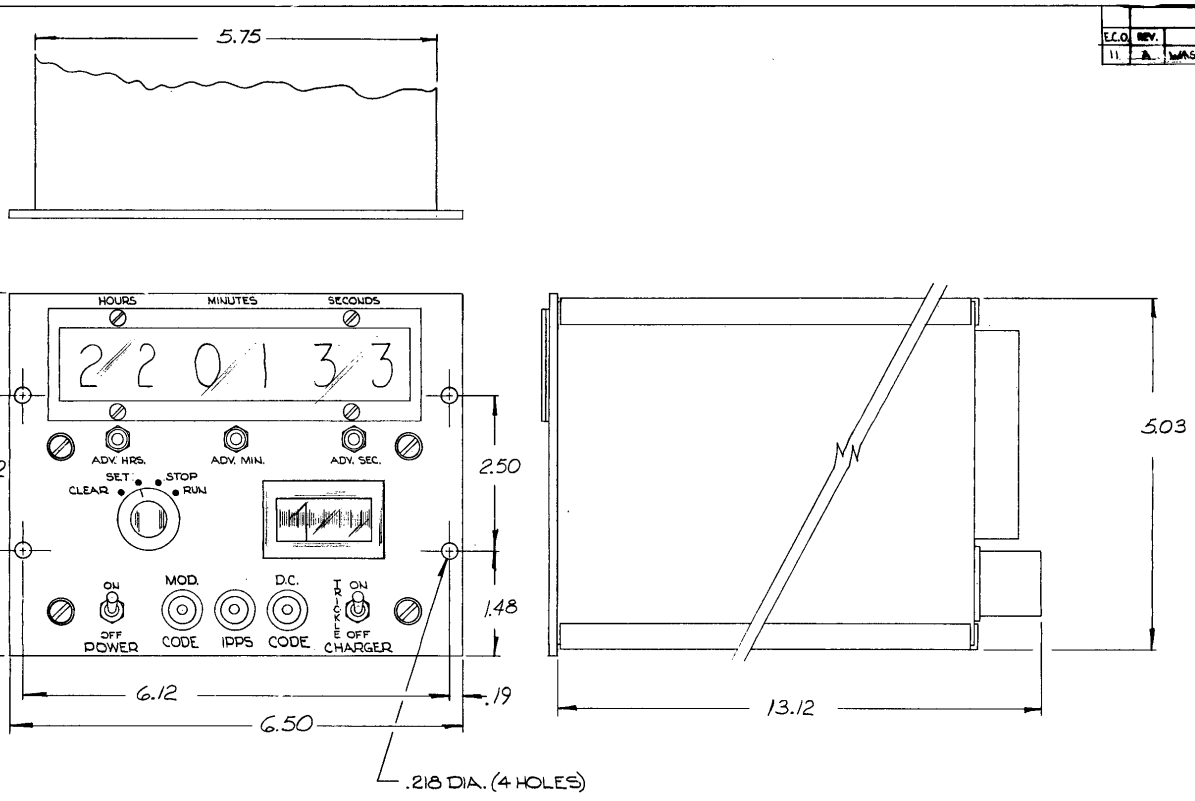


FIGURE 5.24

ITEM	PART NO.	DESCRIPTION	QTY.	REMARKS

LIST OF MATERIAL

MAT'L.	FINISH	BY	DATE
		DR.	8-4-6
UNLESS OTHERWISE SPECIFIED		CHK.	
FRACTIONS ±1/64		ENG.	
DECIMALS ±.005		PROD.	
ANGLES ±30'			
REMOVE BURRS AND SHARP EDGES			

FLOW CORPORATION
205 SIXTH STREET, CAMBRIDGE, MASS.

TITLE
OUTLINE
T.C.G. READER

SCALE
DO NOT SCALE PRINT

DWG. NO. 4896-01001 [A]

REV. A

REV				
REV.	DESCRIPTION	BY	DATE	APPD
A	INITIAL			

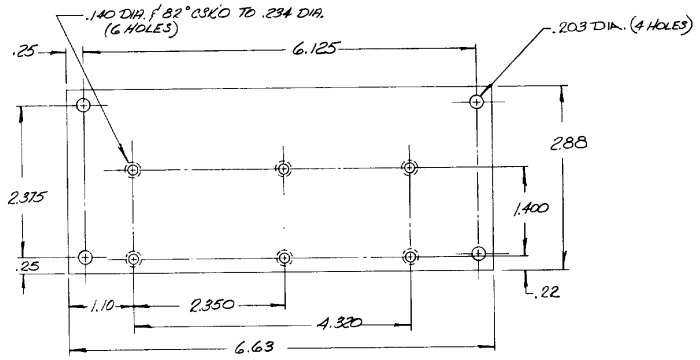


FIGURE 5.25

ITEM	PART NO.	DESCRIPTION	QTY.	REMARKS
		LIST OF MATERIAL		

MAT'L. .062THK ALUM. SH. 2024-T3 FINISH CLEAR ANODIZE

UNLESS OTHERWISE SPECIFIED
FRACTIONS ±1/64
DECIMALS ±.005(3 PLACE) ±.01(2 PLACE)
ANGLES ±30'
REMOVE BURRS AND SHARP EDGES

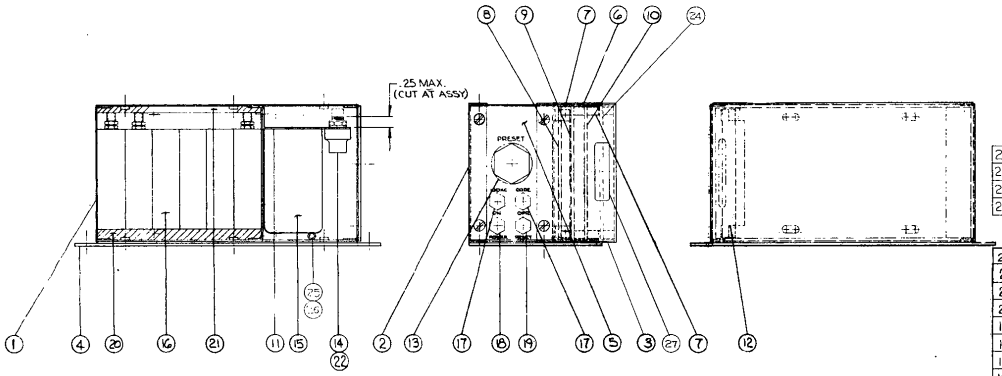
	BY	DATE
DR.		7-14-67
CHK.		
ENG.		7-14-67
PROD.		

FLOW CORPORATION
205 SIXTH STREET, CAMBRIDGE, MASS.

TITLE MOUNTING PLATE

SCALE 1-1
DO NOT SCALE PRINT
DWG. NO. 4896-1101
REV. A

REVISIONS			
REV.	DESCRIPTION	BY	DATE APPD.



NOTE:
1. INSULATE ITEM 8 FROM ITEM 1 BY CEMENTING MYLAR TO ITEM 1.

ITEM	PART NO.	DESCRIPTION	QTY.	REMARKS
27	SRE-265-J	CONNECTOR	1	WINCHESTER
26	2432-1	STANDOFF	1	R & D
25	IN914	DIODE	1	G.E.
24	4896-30005	ASS'Y PC-4 BOARD	1	FLOW
23	4896-1107	SHIELD	2	FLOW
22	2N1613	TRANSISTOR		QPL
21		NEOPRENE RUBBER 1/8" THK.	AR	GRADE [illegible]
20		" " 1/4" THK.	AR	
19	7065K20	SWITCH, TOGGLE DPST (S2)	1	CUTLER HAMMER
18	7055K20	SWITCH, TOGGLE SPST (S1)	1	" "
17	UG1468/U	CONNECTOR (J2,3)	2	AMPHENOL
16	YS-2	BATTERY (BT1-6)	6	YARDNEY
15	MOD 1650	OSCILLATOR 1MC (Y1)	1	FLOW CORP
14	254-S1	HEAT SINK	1	WAKEFIELD ENG.
13	DSM04-7155	CONNECTOR (J1)	1	DEUTSCH
12	WD-22S	CONNECTOR (P1)	1	WINCHESTER
11	4896-1102	MTG. BRACKET OSCILLATOR	1	FLOW
10	4896-40004	ASSY PC-3 BOARD	1	FLOW
9	4896-40003	" PC-2 "	1	FLOW
8	4896-40002	" PC-1 "	1	FLOW
7	4896-1106-P2	SPACER	4	FLOW
6	4896-1106-P1	"	12	FLOW
5	4896-1103	PANEL FRONT SILK SCREEN	1	FLOW
4	4896-1101	MOUNTING PLATE	1	FLOW
3	[illegible]	COVER, RIGHT	1	FLOW
2	[illegible]	COVER, LEFT	1	FLOW
1	4896-1105	CHASSIS	1	FLOW

LIST OF MATERIAL

MAT'L	FINISH	BY	DATE
		DR.	
UNLESS OTHERWISE SPECIFIED		CH.	
FRACTIONS ±1/64		ENG. [illegible]	5-21-8
DECIMALS ±.005		PROD.	
ANGLES ±30'			
REMOVE BURRS AND SHARP EDGES			

FLOW CORPORATION
205 SIXTH STREET, CAMBRIDGE, MASS.

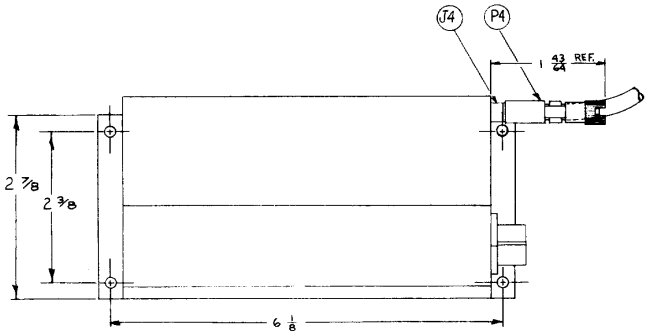
TITLE: MAIN ASSEMBLY
MINIATURE TIME CODE GENERATOR

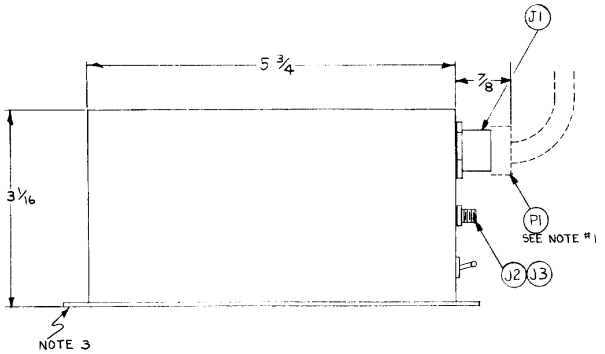
SCALE 1:1 — DWG. NO. 4896-40010

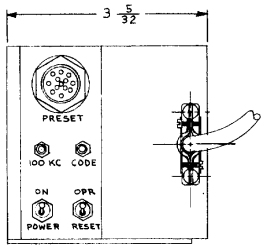
DO NOT SCALE PRINT

FLOW

REVISIONS					
E.C.O.	REV.	DESCRIPTION	BY	DATE	APPD.
12	A	WAS 4896-00002	KS	3-21-68	







NOTE 1 *P1 NOT USED DURING OPERATION - PRESET ONLY
2 WEIGHT APPROX. 35 OZ.
3 MOUNTING PLATE REMOVED WHEN OVEN IS USED

ITEM	PART NO.	DESCRIPTION	QTY.	REMARKS
J4	SRE-246-3	CONNECTOR CHASSIS	1	WINCHESTER
P4	SRE-24P-JTCH	CONNECTOR CABLE	1	WINCHESTER
P2,P3	UG 1465/U	COAX CONNECTOR (USE UG188A COAX)	2	GPL
J2,J3	UG 1468/U	COAX-CHASSIS CONNECTOR	2	GPL
P1	DSM07-7-15P	EXTERNAL CONNECTOR-PRESET ONLY	1	DEUTSCH CO.
J1	DSM04-7-15S	PRESET CHASSIS CONNECTOR	1	DEUTSCH CO.

LIST OF MATERIAL

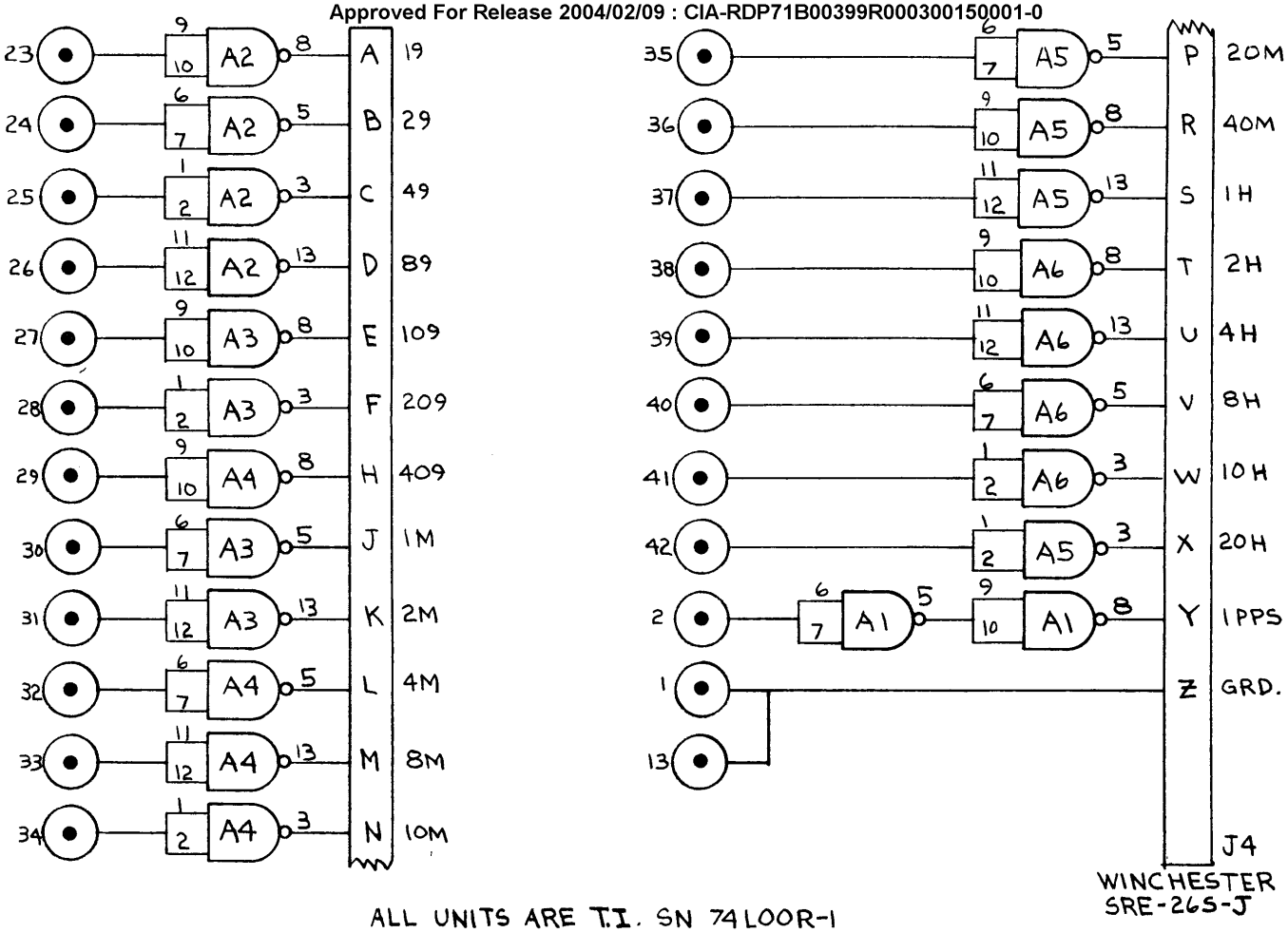
MAT'L	FINISH	BY	DATE
COVER-STAINLESS STEEL	PASSIVATE	DR. [illegible]	11 MAR 68
UNLESS OTHERWISE SPECIFIED		CHK. [illegible]	3-15-68
FRACTIONS ±1/64		ENG. [illegible]	3-15-68
DECIMALS ±.005		PROD.	
ANGLES ±30'			
REMOVE BURRS AND SHARP EDGES			

FLOW CORPORATION
127 COOLIDGE HILL ROAD, WATERTOWN, MASS.

TITLE: MINIATURE TIME CODE GENERATOR

SCALE 1:1 | DWG. NO. C4896-00004 A | REV. A
DO NOT SCALE PRINT

FIGURE AIII-2



ALL UNITS ARE T.I. SN 74LOOR-1

FIGURE AIII-3

PC-4 BOARD SCHEMATIC		FLOW CORPORATION
MAT'L	DWN BY K.S.	127 COOLIDGE HILL RD. WATERTOWN. MASS.
FINISH	SCALE	
(EXCEPT AS NOTED)	DATE 5-31-68	DWG. NO. SHT. 4 A4896-70001

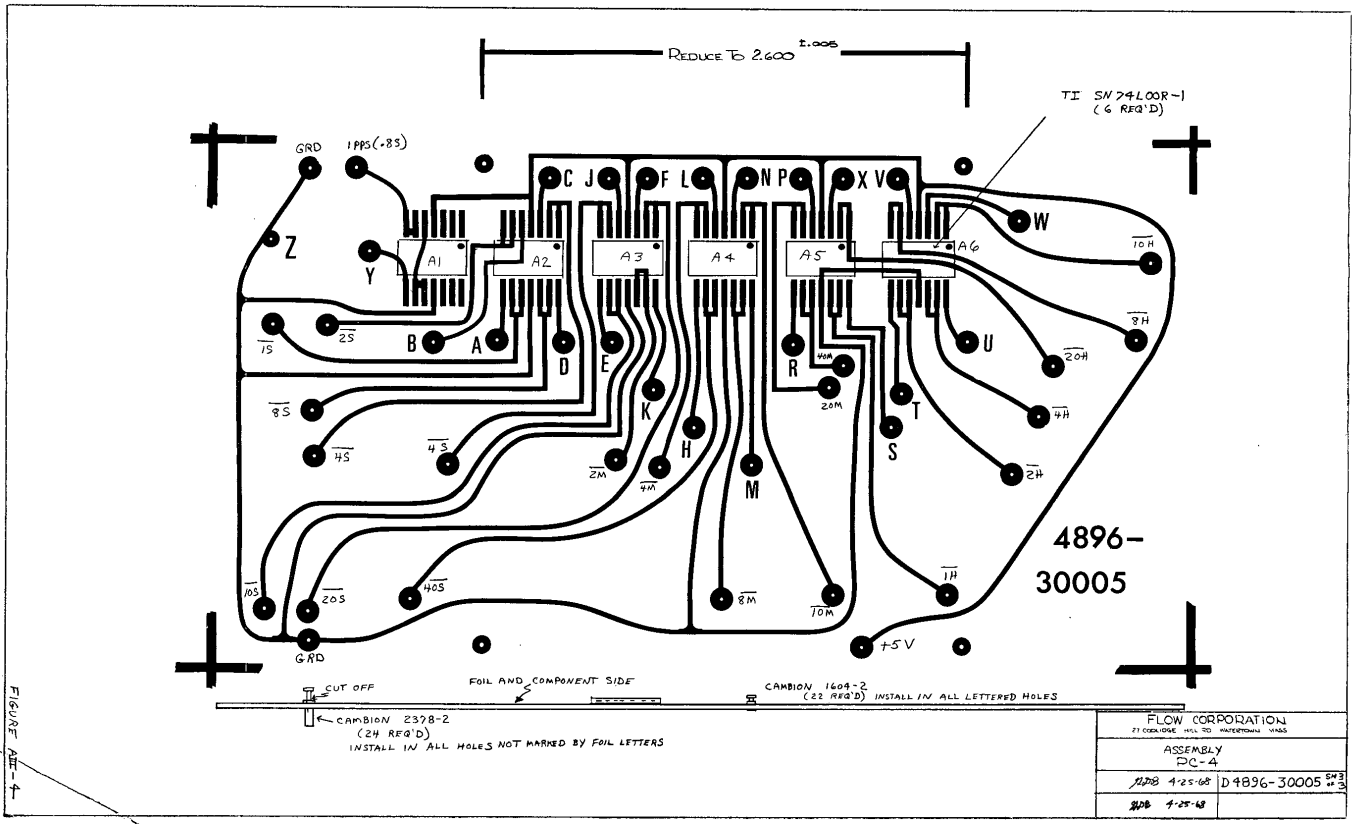


FIGURE AH-4